DIRECT MODEL PREDICTIVE CONTROL OF NON INVERTING BUCK-BOOST DC-DC CONVERTER

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***Abstract*— Direct model predictive control (DMPC) of the non-inverting buck-boost DC-DC converter with magnetic coupling between input and output is proposed. In this paper, direct model predictive control (DMPC) of the noninverting buck-boost DC-DC converter with magnetic coupling between input and output is proposed. Unlike most of the other converters, the subject converter has the advantage of exhibiting minimum phase behavior in the boost mode. However, a major issue that arises in the classical control of the converter is the dead zone near the transition of the buck and boost mode. The reason for the dead zone is practically unrealizable duty cycles, which are close to zero or unity, of pulse width modulation (PWM) near the transition region. To overcome this issue, we propose to use DMPC with the PID controller. In DMPC with the PID controller, the switches are manipulated directly by the controller without the need for PWM. Thereby, avoiding the dead zone altogether. DMPC and PID also offer several other advantages over classical techniques that include optimality and explicit current constraints. Moreover, simulations show that the DMPC technique results in a significantly improved performance as compared to the classical control techniques in terms of response time, reference tracking, and overshoot.**

***Keywords*— Direct model predictive control (DMPC), DC-DC converter, pulse width modulation (PWM), current constraints.**

1. INTRODUCTION

Switched-mode DC-DC power converters are very attractive, since their wide range of applicability in energy conversion, distribution generation, and integration of renewable energy sources into the DC grid (Hossain and Rahim (2018)). Depending on the applications, various DC-DC converters have been utilized to step up/down the regulated DC voltage from the unregulated DC voltage. In practice, buck and synchronous buck converters are the most commonly used step-down DC-DC converters (Erickson and Maksimovic (2007)).On the contrary, many industrial applications prefer conventional PID controller theory due to its simple structure and low-cost implementation (Garg et al. (2015)). In the PID controller, the tuning parameters are calculated using a trial-and-error method that requires considerable time to design and may sometimes fail to improve the performance. In numerous applications, like battery charging/discharging, fuel-cell regulation systems, power factor correction, and MPPT of solar panels, a dc-dc converter is used to obtain a controlled output from a varying input source. A non-inverting buck-boost converter is preferred in applications requiring buck-boost properties and having low current/voltage ripples. Their beneficial aspects incorporate high power transfer efficiency, small voltage ripples, and small stresses on active and passive components. Majority of the converters that operate in boost mode exhibit right half plane (RHP) zeros in continuous-conduction mode. The existence of these RHP zeros, which makes the system non-minimum phase, has the tendency to make the controller design difficult, limit the loop bandwidth, penalize output capacitor

size, and make the converter susceptible to oscillations. The combination of magnetic coupling between input and output inductors and a series resistor-capacitor network depicted in Fig. 1, has successfully eliminated RHP zeros. Thus, the system can easily achieve wide control bandwidth. Other advantages include the prospect of regulating input/output currents or voltages with quick response.

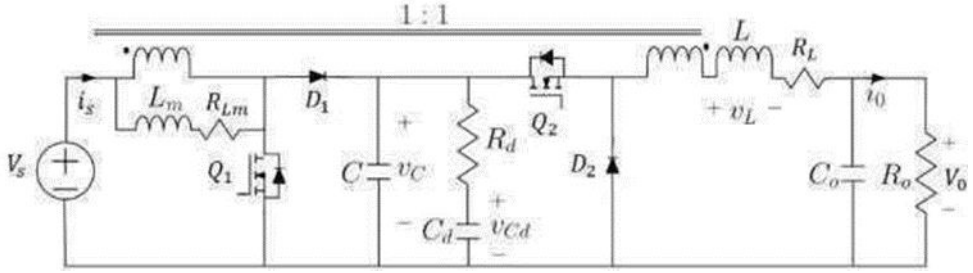

Fig 1. Circuit diagram of non-inverting Buck-Boost converter.

Transistor-diode symbols are used to form circuit schematic of the converter in Figure 1. Also, two operational modes are introduced based on u that is the switching function. Two different modes are classified by this topology for buck and boost mode. Overall, to present a functional state, the controller must operate such that the level of the output voltage on the load is lower than supply voltage. Consequently, to satisfy this condition, Q1 switch will be fired while Q2 is off. However, when the higher output voltage is produced compared to input voltage, the converter works in boost mode (Q2 starts to fire when Q1 stays constantly on). Linearizing the state-space averaging model around the operating point is used to get the system's small signal transfer function. The transfer functions for buck and boost modes are driven based on output voltage ($\hat{C}$) and control input.

Where D1 and D2 show the duty cycles of switches. Also, the superscript “” illustrates a minimal AC variation around the steady-state operating point. Considering the transfer function of the converter, the impact of capacitor resistance (RC) among the parasitic elements is the only effective factor providing a zero in the transfer function. It should be noted that the series diodes have a small range threshold voltage and it is possible to be ignored; also, the on-resistance of switches can be estimated about 0.8 ohm that can be ignored since it has a small amount. Thus, one can omit other parasitic elements from small-signal analysis of the circuit; However, their influence is applied in both experimental and simulation results. The relation between the capacitor voltage and the output voltage is shown in Equation

In order to overcome this, many PID tuning algorithms such as Zeigler-Nicholas (Z-N) (Skogestad (2003)), stability boundary locus (SBL) (Tan et al. (2006)), IMC (Rivera et al. (1986); Wei et al. (2009)) and various evolutionary tuning methods are reported. But there are limitations in using these; for example, Z-N technique can only give a range of tuning values, the SBL method provides a region of stabilizing PI parameters, evolutionary techniques require some assumptions and involves complex iterative analysis. However, in comparison to other methods, IMC based PID tuning is model-based, simple, robust and sub-optimal technique which requires only a single tuning parameter. It is observed that this tuning parameter is generally evaluated on the basis of trial and error method or approximation of plants time constants or optimizing some desired parameters (such as integral square error) or solving nonlinear equation with

constraints on gain and phase margins, maximum sensitivity, etc (Laughlin et al. (1986)). This is the motivation for present work to tune single IMC parameter without using trial and error approach.

Majority of the converters that operate in boost mode exhibit right half plane (RHP) zeros in continuous-conduction-mode. The existence of these RHP zeros, which makes the system non-minimum phase, has the tendency to make the controller design difficult, limit the loop bandwidth, penalize output capacitor size, and make the converter susceptible to oscillations[1], [7]. The combination of magnetic coupling between input and output inductors [8] and a series resistor-capacitor network [9]. As a result, a so-called dead zone appears close to the transition region. The appeared dead zone denotes the discontinuity in the converter conversion ratio (1) defined in a single duty ratio control variable u which takes values between 0 and 2 [2]. The dead zone causes excessive ripples in the output voltage and potential disorder of the converter [12]. The vanishing of dead zone is of great importance because we want soft transition between buck and the boost mode in several applications [13]-[15].
However, the topology in Fig. 1 also possesses an extensive downside. The switching pulses generated near the vicinity of transition between buck and the boost mode are so short that a practical circuit cannot catch it. As a result, a so-called dead zone appears close to the transition region. The appeared dead zone denotes the discontinuity in the converter conversion ratio (1) defined in a single duty ratio control variable u which takes values between 0 and 2 [2] as shown in Fig. 2. The dead zone causes excessive ripples in the output voltage and potential disorder of the converter. The vanishing of the dead zone is of great importance because we want soft transition between buck and the boost mode in several applications.

$$M(u)=\frac{\min(1,u)}{1-\max(0,u-1)}$$

$$\begin{cases} s_1=\max(0,u-1) \\ s_2=\min(1,u) \end{cases}$$

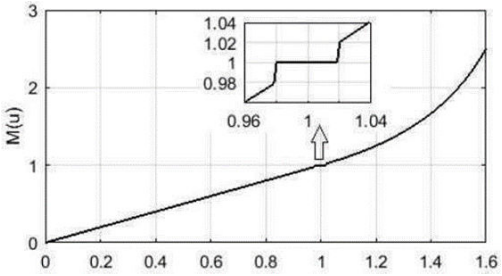

Fig. 2. Dead zone at the transition of buck and boost mode: M(u) is the conversion ratio where u is the duty ratio control variable.

Numerous dead zone minimization methods have been used in the literature. A Well-known technique is focused on the overlap of buck and the boost operation modes at the buck-boost transitions. Its principal disadvantages are: ripples in output voltage are poorly minimized, there are substantial subharmonics and the switching losses are almost twice. Much better results were obtained regarding dead-zone minimization, in which the overlapping of buck and boost mode is merged and fixed with the duty cycle of buck mode to its optimum attainable value. But the main drawback of this technique is that the ripples are improved at the cost of efficiency in the boost mode another strategy was proposed. The principle concept of this technique is the addition of the dead zone avoidance and minimization (DZAM) machine in the control loop that will vanish the dead zone. Unfortunately, this technique is difficult to actualize in analogue control systems. In the literature, some other methods are used for attaining soft transitions, which can't be readily employed to the converter topology examined in this paper. They either rely on sliding mode control or adjust

each duty cycle to exactly half. The main contribution of this paper is to use direct model predictive control (DMPC) for the aforementioned topology that can completely avoid the dead zone. DMPC is one of the emerging control techniques for power electronics converters. Key advantages of DMPC are: it can deal with plant nonlinearities, multiple inputs, multiple control objectives, and any constraints on inputs/states while ensuring optimal control. Another advantage of DMPC is that unlike PWM control, the switch can be directly controlled without a demodulator. Avoiding the demodulator allows the use an accurate model of the converter that incorporates switching nonlinearities as compared to an averaged model. The use of an accurate model along with optimal control allows DMPC to exhibit superior performance for some power converters as compared to most other control techniques. In DMPC switch transitions are only done at a fixed sampling time, thus limiting the minimum width of the switching pulses. This completely wipes out the dead zone to attain smooth transitions between buckbuck and boost mode. A disadvantage of DMPC is its high computational complexity. However, it has been mitigated by some efficient techniques and the availability of fast speed microprocessors. Another key point is that the converter in Fig. 1 is the minimum phase. Therefore, we can have a small value of prediction horizon to reduce the computational complexity.

Proposed Finite Control Set Model Predictive Control

Proposed Finite Control Set Model Predictive Control based on NSS tracking

The design of the FCS-MPC relies on three key features: the predictive model, a cost function representing the feature to be minimized and constraints on input variables used for the control. Equations (2-5) and (2-6) are used as the predictive model in the proposed FCS-MPC. Section 2.5.1 describes the cost function designed for time optimal control while section 2.5.2 presents the constraint on the output voltage deviation.

8.1 NSS Tracking Cost Function for Time Optimal Control

Figure introduces vectors V1 and V2, useful for the cost function design, along with the expected time optimal time optimal trajectories.

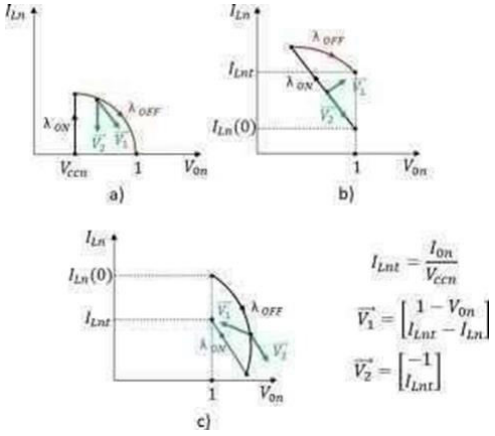

Figure 3: Ideal trajectories for MTC in state-plane domain for (a) start-up transient, (b) loading transient and (c) unloading transient

From this figure, two situations are considered. One scenario is illustrated in (a) and (b) where the state trajectory ends with an OFF NSS in red whereas the other scenario is illustrated by (c) where the state trajectory ends with an ON NSS in blue. Since the system offers only two possible switching positions, the first situation can be translated into tracking the OFF NSS containing the target point (1,ILnt) while the other situation is equivalent to tracking the ON NSS including the target point (1, ILnt).

The OFF NSS tracking is translated into a cost function term in (2-23), decreasing when the converters states evolve along the ideal trajectory of (a) under start-up conditions or (b) for loading transient, where $R2 = (ILnt(k) - Ion(k))2 + (1 - Vccn)2$ and can be verified from the diagrams in figure.

$$J_{ref_{OFF}}(I_{Ln}(k+1), V_{on}(k+1)) = \|\|\overrightarrow{V_1}\|\|\overrightarrow{V_2}\| - \overrightarrow{V_1}.\overrightarrow{V_2}| + \left|(I_{Ln}(k+1) - I_{on}(k))^2 + (V_{on}(k+1)\right.$$

Similarly, the ON NSS tracking is expressed in (2-24) as a decreasing term when the converter states evolve along the trajectory in (c) for an unloading transient.

$$J_{ref_{ON}}(I_{Ln}(k+1), V_{on}(k+1)) = \|\|\overrightarrow{V_1}\|\|\overrightarrow{V_2}\| + \overrightarrow{V_1}.\overrightarrow{V_2}| + |1 + I_{Lnt}(k)^2 - I_{Ln}(k+1)I_{Lnt}(k) - V_{on}(k+1)|$$

The second term of the addition in (2-23) compares the square of the distance from the DC operating point and the current position with the distance from the DC operating point and the target point. Similarly, the second term in (2-24) refers to the distance between the x-intercept of the ON NSS tied to the current position and the x-intercept of the ON NSS tied to the target point

To create the cost function (2-25), (2-23) and (2-24) are combined using a factor λ equal to 1 if the

ON NSS tracking is enabled and 0 if OFF NSS tracking is enabled.

$$J = \lambda JrefON + (1 - \lambda)\, JrefOFF$$

Figure 8 illustrates the mapping of the state plane domain with λ values. Lambda is equal to 1 if the converter states are located above the current target ON NSS on the state plane and 0 otherwise.

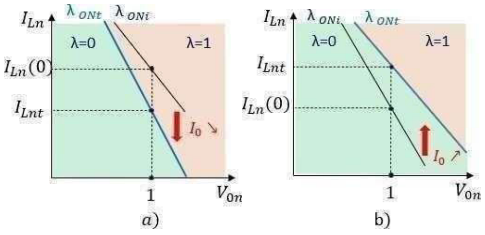

Figure 4: Lambda mapping when Io increases (a) or decreases (b) att=0

In (a), the load current I0 decreases at time t=0 when the normalized converter state is (1, ILn(0)) and is assumed to be the objective point before I0 changes. Before this change, the current target ON NSS tracked by the control scheme is λONi.

The decrease in load current induces a decrease in the objective inductor current ILnt and the new ON NSS to be tracked becomes λONt in light blue in figure 12a. The consequence is also a change in the mapping of λ values that corresponds at this instant to Figure 12a. At t=0, the λ value is initially equal to 1, enabling the tracking of the target ON NSS to reach the reference voltage and current. Similarly, figure 12b presents the situation where the load current increases. In that case, ILnt increases and λ is initially equal to 0 at t=0.

Constraints of the proposed FCS-MPC

As the cost function reduction is made to ensure Time-Optimal Control regardless of the voltage deviation, constraints on the maximum output voltage of the converter are set to limit this deviation. If the predicted output voltage for one switching structure leads to a voltage deviation greater than the maximum allowed by the constraint, then J is equal to infinity forcing the control to choose the other switching possibility. If both switching structures lead to an infinite cost function, the OFF-switching structure is chosen by default. However, the voltage needs to achieve a minimum deviation given by (2-10) and (2-11) to reach the target during a loading or an unloading transient, respectively. An important thing to consider for the constraint, in addition to the minimum deviation, is the voltage ripple. Equations (2-26) and (2-27) estimate this voltage ripple at the point of minimum voltage deviation for loading and unloading transients, respectively. From figure 9b and 9c, the voltages corresponding to the minimum deviation for loading transient ($1 - \Delta vMDLn$) and unloading transient ($1 + \Delta vMDUn$) are located on the load line (LL). Therefore, the inductor current can be deduced from these points. Using the inductor current, (2-5) can be used to

estimate the maximum voltage ripple between ON and OFF switching decision for both loading transient in (2-26) and unloading transient in (2-27).

$$\delta_{Ln} = 2\pi T_{sn} \times \max\left(\left|I_{on} - \frac{I_{on}}{V_{ccn}}(1 - \Delta v_{MDLn})\right|\right.$$

$$\delta_{Un} = 2\pi T_{sn} \times \max\left(\left|I_{on} - \frac{I_{on}}{V_{ccn}}(1 + \Delta v_{MDUn})\right.\right.$$

The constraint applied is given in (2-28). It is expressed proportionally to the highest minimum voltage deviation, with the expected voltage ripple, between the loading and unloading transient case to ensure stable regulation in both transient scenarios. In (2-28), p is the variable set by the designer to adjust the voltage deviation proportionally to the maximum of the minimum voltage deviation with its associated voltage ripple and must be greater or equal to 1.05.

$$|V_{0n} - 1| < p \times \max\left(\Delta v_{MDLn} + \delta_{Ln}, \Delta v_{MDUn} + \delta_{Un}\right)$$

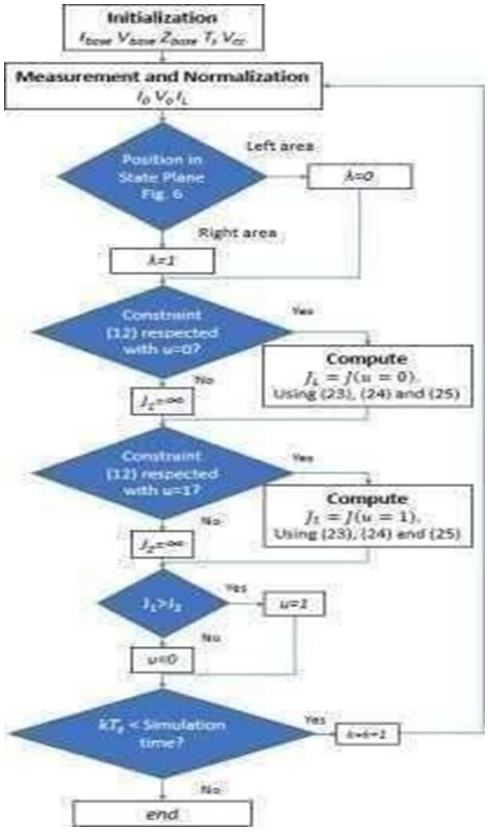

Fig5. Proposed FCS-MPC Flowchart

The initialization step consists of offline calculations of base values essential for normalization. Then, Io, Vo and IL are measured at a sampling frequency of Ts and normalized. The first "if" condition attributes a value to λ based on the location of the converter states on the state plane. The second "if" condition uses the prediction from (2-5) and (2-6), when u=0, to determine if the constraint in (2-28) is respected for the OFF-switching decision. If this constraint is respected, the associated cost function $J1$ is computed using (2-23), (2-24), (2-25) and set to infinity otherwise. The third "if" condition repeats this process for u=1 with its associated cost function $J2$.In the fourth "if", the switching decision u is set to 1 if $J2$is inferior to $J1$and to 0 otherwise. Finally, the last "if" condition checks for the end of simulation and loops back to the measurement and normalization step. It is important to note that during start-up transients, the constraints are disabled and the second and third "if" conditions are forced to the "yes" path.

Generalized Predictive Model and Natural Switching Surfaces

All three of the DC-DC converters from figure 20 can be modeled using generalized differential equations given in (3-1) and (3-2) where kω, m1 and m2 are different depending on the converter type (see Table I). In Table I, u is set to 0 or 1 if the MOSFET Q1 is OFF or ON respectively. The MOSFET Q2 is OFF when u=1 and ON when u=0.

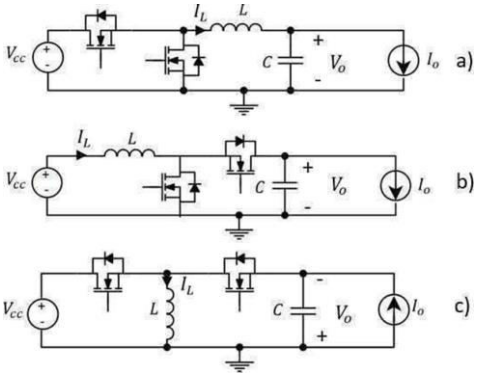

Figure 6: DC-DC buck (a), boost (b), and buck-boost (c) converter

For all three converters, the following base values are used to obtain

normalized expressions (subscription) in Table I and the system of differential equations to obtain (3-3) and (3-4). Vr represents the desired output voltage set point.

PROPOSED CONTROL SCHEME

The control technique used in this paper is direct model predictive control (DMPC). In DMPC the control law is based on an optimization problem. The optimization problem minimizes an objective function, which penalizes deviation from the control goals. The optimization problem finds the optimal switching sequence for the next N time samples, where N is the prediction horizon. In DMPC only the first switch positions in the optimal switching sequence are applied to the circuit and the optimization problem is solved again in the next time sample to incorporate.

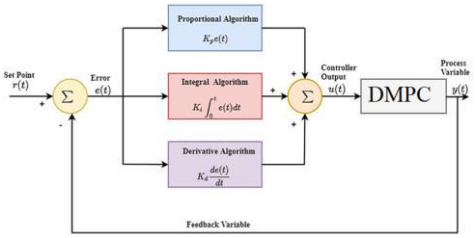

Figure 7. Prposed Controller Block diagram.

In DMPC the control mechanism is carried out by the direct manipulation of switch states for the complete sampling interval. Consequently, this technique never demands a modulator. In our case, we have two control goals. The first is to regulate the output voltage and the second is to improve efficiency by limiting excessive switching transitions. The objective function is designed such that it calculates the sum of output voltage error and the difference between two successive switching states over the finite prediction horizon N. The latter term is designed to reduce the switching frequency and avoid unnecessary switching. The objective function at time instant k is as follows:

$$J_n = \sum_{l=1}^{N} \left(\left| v_{0err}[n+l] \right| + \lambda \left(\left| \Delta s_1[n+l] + \Delta s_2[n+l] \right| \right) \right)$$

Where the error in output voltage, vref is is the reference output voltage.

$$v_{0err}[n+l] := v_{ref} - v_0[n+l]$$

$$\Delta s_1[n+l] := s_1[n+l] - s_1[n+l-1]$$

The validation of controller performance is observed from the transient response of the overall system and with three different conditions such as sudden changes in input and reference voltages and load.

- Transient Comparison
- The transient response of the complete system was observed respectively. The performance of the proposed controller is also observed at different crossover frequencies.
- Sudden Change in Input Voltage
- The overall system performance is monitored for sudden changes in input voltage while other all conditions are kept constant. Sudden Change in Reference Voltage
- The performance of the complete system for change in set point voltage, i.e., output voltage.
- Sudden Load Change

The overall system performance is monitored for sudden changes in load resistance while other all conditions are kept constant. The control technique used in this paper is direct model predictive control (DMPC). In DMPC the control law is based on an optimization problem. The optimization problem minimizes an objective function, which penalizes deviation from the control goals. The optimization problem finds the optimal switching sequence for the next N time samples, where N is the prediction horizon. In DMPC only the first switch positions in the optimal switching sequence are applied to the circuit and the optimization problem is solved again at the next time sample to incorporate feedback [39]. In DMPC the control mechanism is carried out by the direct manipulation of switch states for the complete sampling interval. Consequently, this technique never

demands a modulator [40]. In our case we have two control goals. The first is to regulate the output voltage and the second is to improve efficiency by limiting excessive switching transitions. The objective function is designed such that it calculates the sum of output voltage error and the difference between two successive switching states over the finite prediction horizon N. The latter term is designed to reduce the switching frequency and avoid unnecessary switching.

The constraint Equation above ensures that only the feasible input combination shown in Table I are allowed. Solving the optimization problem results in optimal inputs for time instant n and future inputs for the remainder of prediction horizon. In DMPC, only the first element of the computed optimal sequences is applied to the system. At the next time sample, the state is measured or estimated and the optimization problem is solved again. This mechanism allows feedback in DMPC. The optimization problem Equation has an exponential computational complexity with the prediction horizon. Since there are three members in the set, there is a possibility of 3 N distinct sequence. In enumeration based techniques of DMPC the objective function Equation has to be evaluated for each possible sequence. Moreover, based on the model the future states also have to be predicted for each possible sequence. These calculations lead to increase in the total computational complexity.

However, in our case we can keep a short horizon since the converter is minimum phase. An advantage of DMPC is that the control inputs s1 and s1 can only be changed after the sampling interval. Therefore, unlike PWM, the transistor gate pulses are never smaller the sampling time, which may have issues in realizing practically. Moreover, in DMPC the converter doesn't exclusively operate in either the buck mode or boost mode. DMPC chooses the best feasible inputs in that could meet the control goals. Another advantage of DMPC is that we can put other constraints in the optimization problem Equation. For example, a constraint on the maximum inductor currents can be used to avoid a current control loop used in classical control techniques. The concept of proposed DMPC is summarized in algorithm 1, in which function f represents the state space model in Equation. Flow chart is abridged.

Initially the best-known optimal cost J is initialized by a big number and all the possible 3 N sequences of inputs are generated. For each sequence the states and output are predicted that are used. Evaluate the objective function. If the objective function is smaller than J, then the best known cost J and best-known input sequence are updated. The block diagram of the converter along with the proposed controller is depicted

Algorithm DMPC algorithm

An advantage of DMPC is that the control inputs s1 and s1 can only be changed after the sampling interval. Therefore, unlike PWM, the transistor gate pulses are never smaller in the sampling time, which may have issues in realizing practically. Moreover, in DMPC the converter doesn't exclusively operate in either the buck mode or boost mode. DMPC chooses the best feasible inputs in J that could meet the control goals. Another advantage of DMPC is that we can put other constraints in the optimization problem Equation (6). For example, a constraint on the maximum inductor currents can be used to avoid a current control loop used in classical control techniques. The concept of the proposed DMPC is summarized in algorithm 1, in which function f represents the state space model in Equation (4). The flow chart is abridged.

Initially the best-known optimal cost * J is initialized by a big number and all the possible 3 N sequences of inputs are

generated. For each sequence, the states and output are predicted that are used to

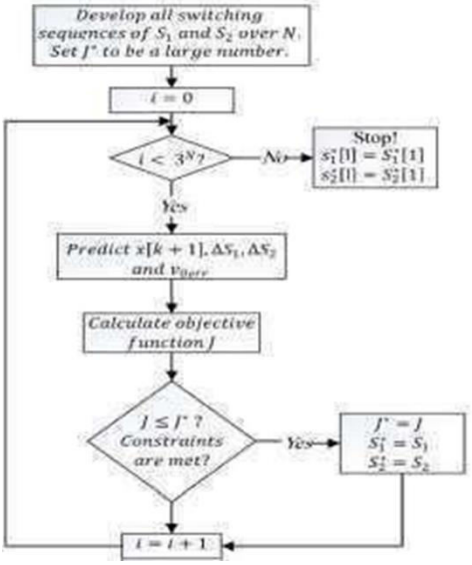

Fig.9. Flowchart of the DMPC algorithm

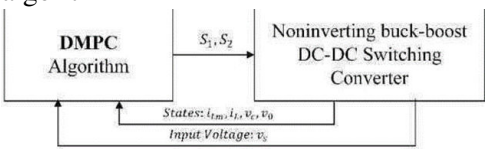

Fig10. Block diagram of the DMPC Algorithm.

Algorithm 1 DMPC algorithm

Function $s_1^*(n),\ s_2^*(n)$=**DMPC** $\left(\hat{x}(n), s_1(n-1)\right), s_2(n-2)$

$J^*(n) = \infty; s_1^*(n) = \phi; s_2^* = \phi$

For all S_1, S_2 *over* N **do**

J=0

For n=1 to N **do**

If $s_1(n) = 1$ & $s_2(n) = 1$ **then**

$x(n+1) = f_1\left(x(n), s_1(n), s_2(n)\right)$

else if $s_1(n) = 0$ & $s_2(n) = 1$ **then**

$x(n+1) = f_2\left(x(n), s_1(n), s_2(n)\right)$

else

$x(n+1) = f_3\left(x(n), s_1(n), s_2(n)\right)$

end if

$v_{0err}[n+1] = v_{ref} - v_0[n+1]$

$\Delta s_1[n] := s_1[n] - s_1[n-1]$

$\Delta s_2[n] := s_2[n] - s_2[n-1]$

$J = J + v_{0err}[n+1] + \lambda\left|\Delta s_1[n] + \Delta s_2[n]\right|$

end for

if $J < J^*(n)$ **then**

$J^*(n) = \mathrm{J}, s_1^*(n) = S_1(1), s_2^*(n) = S_2(1)$

end function

SIMULATION RESULTS AND COMPARISON

Fig11. Inductor Current output wave from.

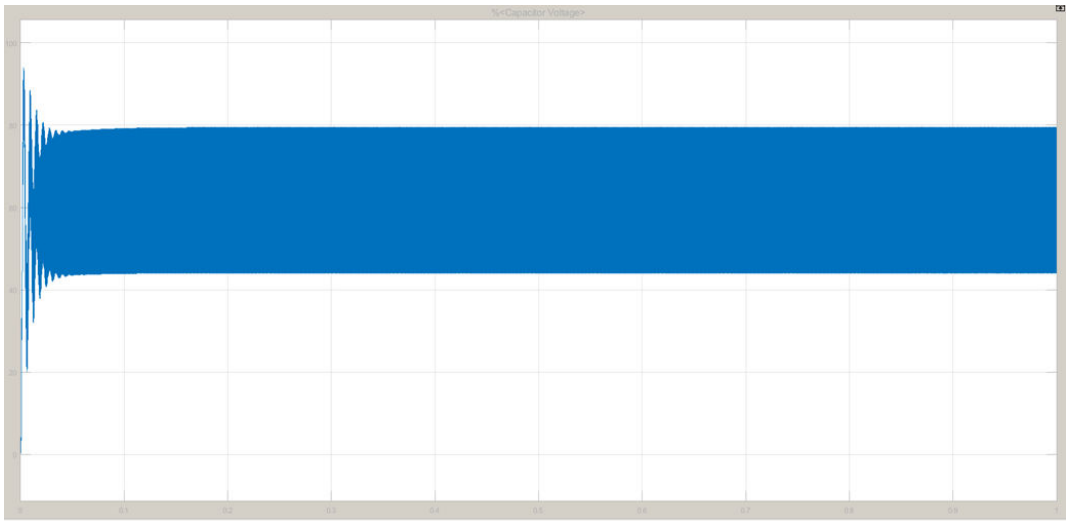

Fig12. Capacitor Voltage output wave from.

In this case the input voltage was first stepped up from 39V to 80V at t=0.05ms. Response of both the DMPC_PID controller is depicted. At the changes in input voltage, the DMPC_PID controller keeps the converter output at the required reference without any significant deviation.

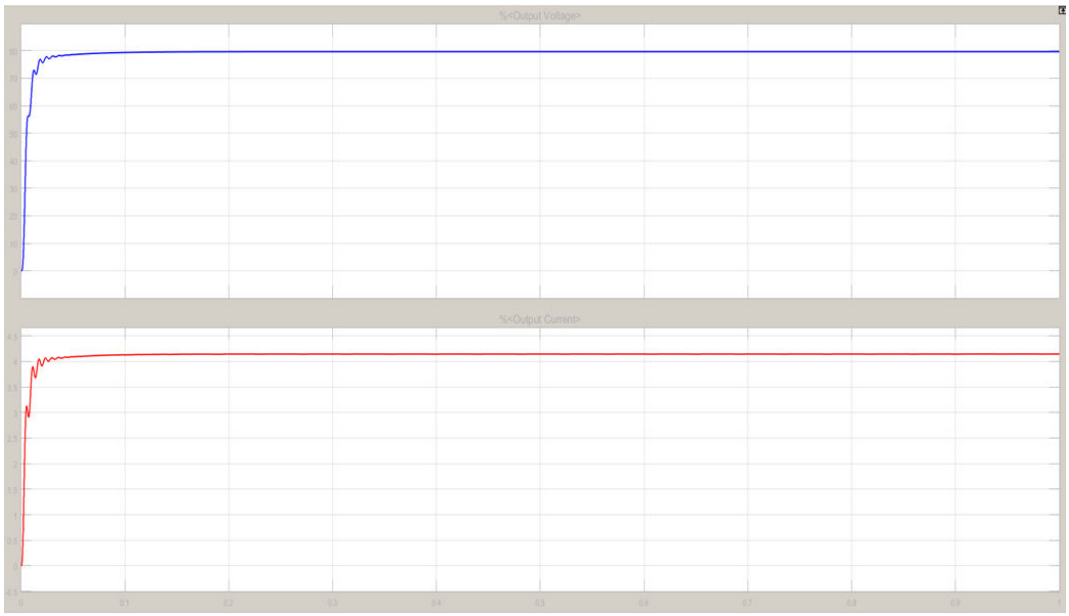

Fig 13. Output Voltage and current wave from.

In this case a linearly varying source is applied as an output voltage to the converter operating at steady state operating conditions with output voltage reference of 80V and current 4A. Response of both DMPC_PI controllers is depicted view of output voltage and respective duty cycles of transition region around 80V and current 4A in DMPC_PID the smallest width of switching signals is 1µs.

The converter depicted in Fig. 13 is simulated with the proposed control and the obtained results are presented here. Five different cases are considered. In case 1 the converter start-up is observed. In case 2, step down variations are made in reference voltage. In step up/down variations are made in the input voltage and the dynamic response of the converter is examined. In case 4, step down change is made in load resistor and response of controllers is observed. In ramp change in input is made to examine the controller's response close to buck/boost transition region. The values of the parameters used are: 14

LμmH, 0.5RLm, LRCμFR, 30μH, 0.3Ω, 1.5 LΩ, 0.22CμF, 110 CμF and 9.6Ω. 9.6Ω. Input voltage Vs varies in the range of 39V to 55V. The control goal is to regulate the output voltage V0 to 48V. The weighting factor λ is kept 0.1, while the prediction horizon N is taken as 6. The sampling time 1Tμs and the sampling frequency 1MHzs. We have been able to use such a small N because the system is minimum phase. A small value of N helps to reduce the computational complexity of the algorithm. The results of the proposed DMPC are compared with PI controller. The PI controller has a proportional gain of 1/25 and integral gain.

Simulation Results Inductor Current

The start-up of the converter with a constant input voltage of 39V is simulated with both PI controller and the proposed DMPC. The inductor currents rise sharply to a peak of more than 14A in DMPC_PID. On the other hand, the inductor currents in DMPC_PID stay within the specified constraint of 14A. The settling time of DMPC is approximately 0.2ms

CONCLUSION

Direct model predictive control of non-inverting buck-boost DC-DC converter. A key advantage of DMPC is that it directly manipulates the switches without the need for any modulator. Thereby, eliminating the dead zone in the transition between buck and boost mode, which is of major concern in the control of the subject converter. Another advantage of DMPC includes the inclusion of current constraints that avoids the use of an extra current loop. Other beneficial aspects of the proposed DPMC are lesser overshoot/undershoot quicker response time, and inherent feed forward. A usual drawback of DMPC is its computational complexity. However, the converter is a minimum phase which makes it possible to use a small value of prediction horizon that reduces the computational complexity.

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