AN ADVANCED HIGH GAIN AND INVERTING CAPABILITY NON-ISOLATED DC-DC POWER CONVERTER

[1]MR. K. GIRINATH BABU, [2]P. RAHUL ,[3]V. NITHIN

[1](Assistant professor), EEE. Guru Nanak Institutions Technical Campus, Hyderabad.

[23]B.Tech Scholars, EEE. Guru Nanak Institutions Technical Campus, Hyderabad.

ABSTRACT

The current gain of the converter grows along with the voltage gain at the same ratio, and this increase in current gains will have an impact on the capacitance of the input and output capacitors. Using an interleaved front-end structure and a Cockcroft Walton (CW)-Voltage Multiplier (VM), a new current-fed interleaved high gain converter is suggested that simultaneously reduces the input current ripple. The phrase "current fed" is used because, in the circuitry that is suggested, a current channel via the interleaved structure's inductors energizes each and every capacitor in the CW-VM. The suggested converter may be used as an input booster to advance DC-AC applications based on fuel cells (FC), photovoltaic (PV), and low voltage battery energy storage systems. The two low voltage rating switches make up the expected topology. The continuous (ripple-free) input current, high voltage gain, low switch rating, high reliability, simple control structure, and high efficiency % are the key advantages of the projected converter architecture. The comprehensive component design, mathematically based steady state analysis, and operating principle of the proposed converter are explained. The research has taken into account the parasitic nature of the components in order to illustrate how they deviate from ideal scenarios. A thorough comparison of the alternative converters on the market is provided. The 300W prototype's testing findings are designed to validate the expected DC-DC converter's operation and performance.

INDEX TERMS: voltage multiplier, renewable energy, non-isolated, inverting, interleaved, high gain.

1.INTRODUCTION

As high-frequency components continue to advance in technology, switching power converters are becoming more and more common. Reduced size and weight of the converter are made possible by high frequency. Furthermore, both inverting and non-inverting outputs may be achievable depending on the DC-DC converters used. One may produce both inverting and non-inverting voltage at the output depending on the DC-DC converters they use.

Inverting DC-DC converters find use in a variety of applications, including solar PV systems, OLED micro display boards, data acquisition systems (DAS), telecommunications modules, and random access memory (RAM) [1-4]. Moreover, independent inverter-load applications and utility grid-DC bus applications need high gain DC-DC converters. Conventional negative output converters are unsuitable for achieving the necessary high gain because they must run at higher duty ratios, which raises the semiconductors' high losses. Many high step-up converters are suggested to handle this, including switched capacitor, cascaded and quadratic, inductor connected, transformer isolated, Z or qZ source, and switch inductor converters. Greater benefits of Z and qZ source converters [5] include fewer semiconductors needed in the step-up stage, a practically constant input current throughout, and excellent reliability due to their resistance to shoot-through stages. The primary disadvantages of these topologies are the very high voltage stress on the semiconductors. Typically, linked inductors and transformers are used to create isolated, higher gain DC-DC converters, as suggested in references [6]–[8].

The MOSFETs' voltage and current spikes are caused by their leakage inductances and the capacitances of their different windings, even though they provide galvanic isolation between the two ports (input and output) at higher switching frequencies. Because of this, this arrangement needed more clamping circuits and filters in addition to components with greater ratings. Several zero voltage switching (ZVS) and zero current switching (ZCS) based soft switched (resonant) converters are presented in [9]–[11]. Selecting MOSFETs with lower ON resistance may assist reduce converter losses and ultimately boost efficiency when the voltage stress on the semiconductors is minimal. In this case, the output diodes may be protected without the need for a snubber circuit or soft switching to lower the voltage stress. However, in [11], the energy stored in the leaking inductance is the only source of energy needed to perform ZVS central MOSFET switching.

Therefore, extra leakage inductance, capacitance, or an additional inductor is required to accomplish ZVS of the primary MOSFET. This reduces gain (duty cycle loss) and increases the number of components. The converter must operate at a higher duty cycle to make up for these problems, which raises the devices' RMS currents and increases losses. The power electronic technology based on the concept of Switched Capacitor (SC) has gained popularity recently due to its ability to achieve greater power densities with a complete monolithic structure and lack of inductive components [12]. The primary disadvantages, however, are the massive active switches and capacitors, the pulsing input current, and the intricate capacitor current regulation. A proposal to include the coupled inductor with SC was made in [13].

Although the SC's issues were resolved by this arrangement, semiconductors still experience spikes in voltage and current. A combination of the basic single inductor (buck, boost, buckboost, sepic, and cuk) and switched inductor (SL) topologies has been presented in [14]–[16]. These converters reduce the MOSFETs' voltage stress and boost gain. They also have a modular design. Recently, a system based on capacitor diode-voltage multipliers (CD-VM) [17]–[19] has been developed to produce a larger output voltage. Due to their simple structure, multiple output capacitor stages, uniform voltage stress across all semiconductor devices and capacitors, higher voltage gain without extreme duty cycle, suitability to feed multilevel inverters, and ease of adding or removing stages without interfering with the main boosting circuitry, these topologies can be a good solution for high voltage conversion. In order to get a high voltage conversion ratio, the interleaved converter is suggested in [19] by mixing positive and negative multipliers. Nevertheless, the circuitry may be obtained by simply replicating the multiplier's constituent parts. As a result, the circuitry needed a lot of diodes and capacitors. Additionally, energy is transferred from capacitor to capacitor in converters [17]–[19], which causes an abrupt transient in the current. Thus, with a greater number of VM stages, the primary issues related to CDVMs are voltage ripple and current-dependent voltage droop. In order to overcome these shortcomings and the quantity of steps, a novel interleaved converter is

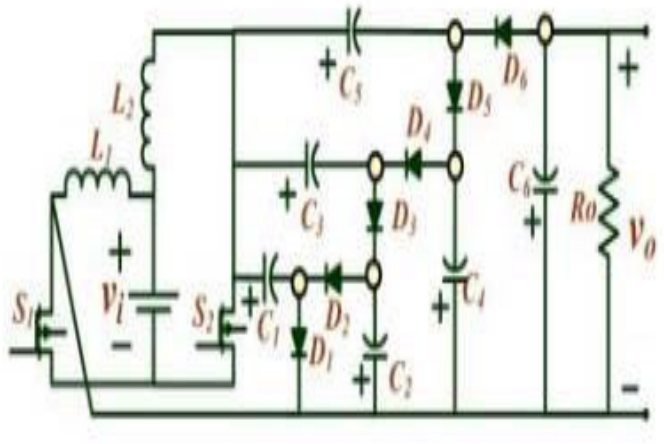

FIGURE 1. Proposed inverting High gain DC-DC converter

suggested for significant profit. The extra characteristic of this setup is that each capacitor is charged by the inductor current. It is noted that for power electronic interfaces in renewable applications, current fed CDVMs are the suitable option. The recommended design, however, called for an extra high voltage diode-capacitor filter step on the output side. Two input boost stages are also used. A novel interleaved converter using a Dickson voltage multiplier is suggested [21]–[30] in order to reduce the VM stages. These DC-DC converter topologies do have several drawbacks, however, including circuit complexity, a greater number of virtual machine stages, an inability to get high gain without inverting, larger input ripples, etc. This

study presents a novel non-isolated current fed interleaved multilevel interleaved boost converter that uses a minimal amount of components and stages to achieve low current ripple at the input side, high voltage gain, and current fed configuration. Potential advantages of the suggested converter include: • High voltage gain with few circuit components; • Inverting voltage capabilities; • Ripple-free input current profile to reduce input side filter needs and passive elements in the circuit.

• Easy control over the charging and discharging of capacitors in VM cells; • Low converter switch ratings; • Extremely efficient.

This work is structured as follows: Section II covers the suggested converter setup, operating principle, steady state analysis for CCM and DCM, and voltage gain analysis. Section III presents the investigation and comparative analysis of the high gain DC-DC converters. In Section IV, the experimental validation and corresponding findings are provided along with a commentary. This paper's final remarks are provided at the conclusion.

2.CONVERTERS

2.1 DC-DC CONVERTER BASICS

An apparatus that takes a DC input voltage and outputs a DC voltage is called a DC-to-DC converter. The voltage levels of the input and the output are often different. DC-to-DC converters are also used for power bus control, noise isolation, and other purposes.

2.2 BUCK CONVERTER STEP-DOWN CONVERTER

When the transistor in this circuit turns ON, voltage Vin is applied to one end of the inductor. The inductor current tends to increase at this voltage. The current will still flow through the inductor and now pass through the diode while the transistor is off. The voltage at Vx will now just be the voltage across the conducting diode for the duration of the complete OFF period as we originally believe that the current through the inductor does not reach zero. If the inductor current is constant, the average voltage at Vx will be determined by the transistor's average ON time.

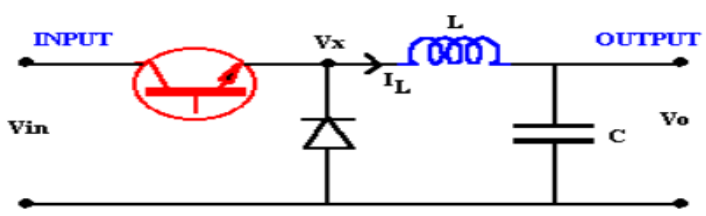

Fig 2.1 Buck Converter

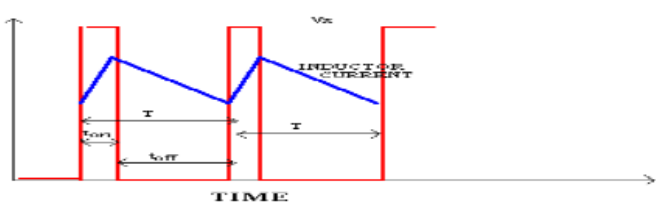

Fig 2.2 Voltage and current changes

3.PROPOSED TOPOLOGY OF INTERLEAVED STRUCTURED CURRENT FED HIGH GAIN CONVERTER

The power circuitry for the three stages of the VMs in the new interleaved high gain converter architecture is shown in Fig. 1. To get the highest voltage gain feasible, the inverting VM cells are coupled to the basic interleaved boost converter. Unlike half-wave VM cells, which have two diodes and one capacitor apiece, each VM cell (stage) has only one diode and one capacitor. This contributes to increasing the fever number gain.

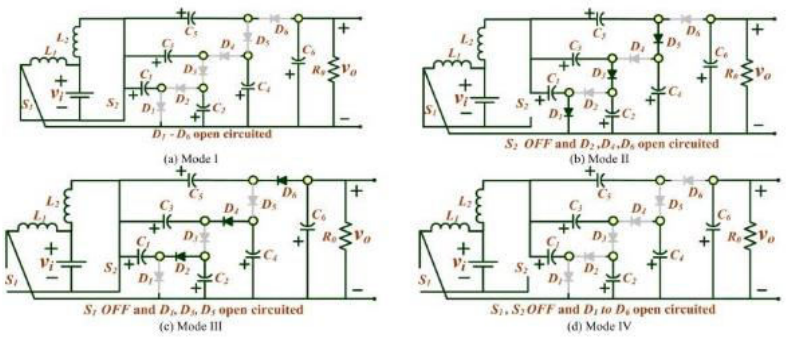

FIGURE 3.1. Operating modes of the proposed DC-DC converter topology. of components.

For the MOSFET to have the most operational levels possible, its switches are phase-shifted by 180 degrees. The voltage gains and all operational stages are derived in the next sections.

A. OPERATING MODES

Mode I: during Mode I, MOSFET's S1 and S2 are ON and the corresponding circuitry is shown in Fig. 2(a). During this Mode I, both the inductors(L1 & L2) are charged from the input voltage vi . The capacitor C6 is discharged via the resistance (Ro-load). The respective mathematical representation for this mode is shown below,

$$\left.\frac{di_{L1}}{dt}=\frac{v_i}{L_1}=\frac{V_i+\Delta v_i}{L_1}\approx\frac{V_i}{L_1},\ \frac{di_{L2}}{dt}=\frac{v_i}{L_2}=\frac{V_i+\Delta v_i}{L_2}\approx\frac{V_i}{L_2}\right\}$$

The diode D1 to D6 are blocked & the C6 is supplying the load.

Mode II: During Mode II, the MOSFETs S1 & S2 are turned ON and OFF, respectively. Fig. 2(b) shows the equivalent circuitry for Mode II. The L1 is energized from the supply voltage through S1. The supply voltage vi and the inductor L2 form boost stage & energized the C1 via D1 and S1. The capacitor C2, supply voltage vi , and inductor L2 energized the C3 via D3 and S1. The capacitor C4, supply voltage vi , and inductor L2 energized the C5 via D5 and S1. The slope of the inductor L1 and L2 currents be able to represented as below,

$$\left.\frac{di_{L1}}{dt}=\frac{v_i}{L_1}=\frac{V_i+\Delta v_i}{L_1}\approx\frac{V_i}{L_1},\quad\frac{di_{L2}}{dt}\approx\frac{V_i-V_{C1}}{L_2}\right\}$$

D1, D3, & D5 are forward biased & simultaneously D2, D4, & D6 are reverse biased. All the capacitors with odd numbers (C1, C3, and C5) are charged through the combination of the input voltage vi , inductor L2, and the even number capacitors

(C2, and C4), respectively. The capacitor C6 is de-energized via load.

Mode III: during Mode III, the S1 and S2 are made OFF & ON, respectively. Fig. 2(c) shows the equivalent circuitry. The L2 is energized from the supply voltage vi via S2. The capacitor C1, supply voltage, and inductor L1 are together energized the capacitor C2 via D2 & S2. The capacitor C3, supply voltage vi , and inductor L1 energized the C4 via D4 & S2. The capacitor C5, input voltage vi , and inductor L1 delivers power to load and at the same time also charged the capacitor C6 through diode D6 and switch S2. During this mode, D2, D4, and D6 are forward biased and the diodes D1, D3, and D5 are reverse biased. All the capacitors with odd numbers (C2, C4, and C6) are charged through by the combination of the input voltage vi , inductor L2, and the even number capacitors (C1, C3, and C5), respectively. The slope of the inductor L1 & L2 currents be able to represented as follows,

$$\left.\frac{di_{L2}}{dt}=\frac{V_i}{L_2},\quad\frac{di_{L1}}{dt}=\frac{v_i-v_{C2}+v_{C1}}{L_1}=\frac{V_i-V_{C1}}{L_1}\right\}$$

Mode IV: In this mode, both MOSFETs S1 & S2 are made OFF and corresponding circuitry is presented in Fig. 2(d). During this mode, the current flowing via inductors L1 and L2 become zero because all the D1-D6 are reversed biased. Generally, this mode is avoided in order to operate converter in CCM. Therefore, both switches are operated with duty cycles greater than the 50% to avoid this mode.

B. CCM ANALYSIS

Figure 3 illustrates a power converter's steady-state functioning. The converter's semiconductor MOSFETs are activated such that Mode I occurs precisely in the center of Modes II and III. Illusions in semiconductor technology

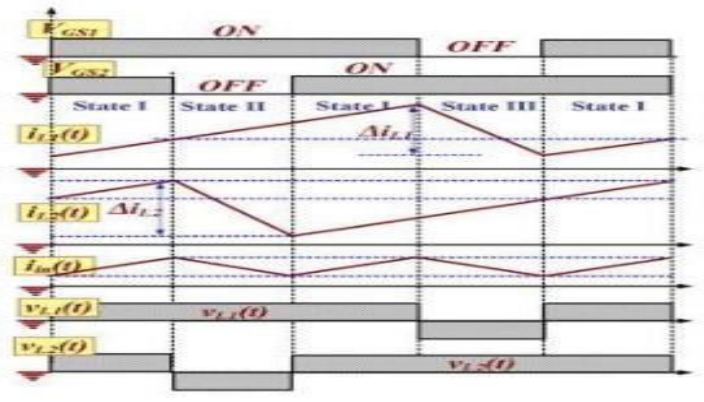

FIGURE 3.2. Steady state operation and respective waveforms of proposed high gain converter in different modes of operation.

PROPOSED CONVERTER CONTROL STATES

By varying duty ratios of switches S1(d1) and S2(d2), the desired voltage across the load can be achieved. The primary condition for the operation is that the gate pulses for both switches should be phase shifted by the 180o . In Table-1, the details about the voltage stress across the switches, capacitor voltages, operating modes and their states and type of the inductor current is given. If d1 < d2 then the summation of voltages of C2, C4, & C6; lesser than the summation of voltages of C1, C3, & C5, else summation of voltages of the C2, C4, & C6 higher than the summation of voltages of C1, C3, & C5. Also, if d1 < d2 then switch voltage stress VS1 < VS2. In order to operate in CCM steady state mode, d1 >= 0.5 & d2 >= 0.5 has to be satisfied.

III. COMPONENT DESIGN AND COMPARISON

The critical inductances L1 and L2 is calculated as follows,

$$\left.\begin{aligned} L_{1,crit.} &= \frac{V_i \times d_1 \times T_S}{\Delta i_{L1}}; \quad L_{2,crit.} = \frac{V_i \times d_2 \times T_S}{\Delta i_{L2}} \end{aligned}\right\}$$

The average inductor current rating must satisfy the following,

$$IL_1 > \frac{3Io}{(1-d_1)}, \quad IL_2 > \frac{3Io}{(1-d_2)}$$

The voltage stresses of switches is obtained as below,

$$\left.\begin{aligned} V_{S1} &= \frac{V_i}{1-d_1}; \quad V_{S2} = \frac{V_i}{1-d_2} \end{aligned}\right\}$$

The blocking voltages across the diodes for all the modes are given as follows,

$$\left.\begin{aligned} mode{-}I, \quad & V_{Dodd} = \frac{-V_i}{1-d_1}; \; V_{Deven} = \frac{-V_i}{1-d_2} \\ mode{-}II, \quad & V_{Dodd} = \frac{-V_i}{1-d_1} + \frac{-V_i}{1-d_2}; \; V_{Deven} = 0 \\ mode{-}III, \quad & V_{Dodd} = 0; \; V_{Deven} = \frac{-V_i}{1-d_1} + \frac{-V_i}{1-d_2} \\ mode{-}III, \quad & V_{Dodd} = \frac{-V_i}{1-d_1}; \; V_{Deven} = \frac{-V_i}{1-d_2} \\ & \left(_{PIV} = \frac{-V_i}{1-d_1} + \frac{-V_i}{1-d_2}\right) \end{aligned}\right\}$$

The critical capacitance values are calculated as follows,

$$\left.\begin{aligned} C_{odd} &= \frac{V_o T_S}{R_o \Delta V_{Codd}} d_1, \quad C_{even} = \frac{V_o T_S}{R_o \Delta V_{Codd}} d_2 \end{aligned}\right\}$$

The detailed comparison of the recently proposed high gain converters with the presented converter is reported in Table 2. In this table, gain, number of components (diodes, switches, inductors, capacitors) and stress across components and efficiency details are discussed. It is notable that compared to the existing converter, the proposed converter configuration required fewer components to attain the desired voltage gain for a given input. Furthermore, voltage stress across the switches, diodes is low compared to the other converters presented in Table. 2.

TABLE 1. All possible operating conditions at different duty cycle ranges.

Operation Modes			States	Inductor Current	Voltage stress across switch	Capacitor Voltage For even number of levels
$d_1+d_2>1$	$d_1<d_2$	$d_1<0.5, d_2>0.5$	I, II, III, IV	*Discontinuous	$V_{S2}>V_{S1}$	$\sum_{i=1,3,5} V_{Ci} < \sum_{i=2,4,6} V_{Ci}$
		$d_1>0.5, d_2>0.5$	I, II, III	Continuous		
		$d_1=0.5, d_2>0.5$	I, II, III	Continuous		
	$d_1>d_2$	$d_1>0.5, d_2>0.5$	I, II, III	Continuous	$V_{S2}<V_{S1}$	$\sum_{i=1,3,5} V_{Ci} > \sum_{i=2,4,6} V_{Ci}$
		$d_1>0.5, d_2<0.5$	I, II, III, IV	*Discontinuous		
		$d_1>0.5, d_2=0.5$	I, II, III	Continuous		
	$d_1=d_2$	$d_1>0.5, d_2>0.5$	I, II, III	Continuous	$V_{S2}=V_{S1}$	$\sum_{i=1,3,5} V_{Ci} = \sum_{i=2,4,6} V_{Ci}$
$d_1+d_2=1$	$d_1<0.5, d_2>0.5$		I, II, III, IV	*Discontinuous	$V_{S2}>V_{S1}$	$\sum_{i=1,3,5} V_{Ci} < \sum_{i=2,4,6} V_{Ci}$
	$d_1>0.5, d_2<0.5$	$d_1<0.75, d_2>0.25$	I, II, III, IV	*Discontinuous	$V_{S2}<V_{S1}$	$\sum_{i=1,3,5} V_{Ci} > \sum_{i=2,4,6} V_{Ci}$
		$d_1>0.75, d_2<0.25$	I, II, IV			
		$d_1=0.75, d_2=0.25$	I, II, IV			
	$d_1=d_2=0.5$		I, II	Continuous	$V_{S2}=V_{S1}$	$\sum_{i=1,3,5} V_{Ci} = \sum_{i=2,4,6} V_{Ci}$

TABLE 2. Comparison of proposed converter with existing converter

Converter	Gain ($G=V_0/V_i$)	Inductors	Capacitors		Switches		Diodes		Efficiency
			Count	VS	Count	VS	Count	VS	
[12]	2/(1-d)	1	3	GV_i	1	$GV_i/2$	3	$GV_i/2$	94%
[13]	(3+d)/(1-d)	2	3	$(G+1)V_i/4$	2	$(G+1)V_i/4$	3	$(G+1)V_i/2$	92.5%
[16]	(3-d)/(1-d)	1	4	$(G-1)V_i/2$	1	$(G-1)V_i/2$	4	$(G-1)V_i/2$	94%
[18]	N/(1-d)	1	2N-1	GV_i/N	1	GV_i/N	2N-1	GV_i/N	89%
[19]	1/d(1-d)	2	3	$C_1=GV_i(1-d), C_2=GV_i d$	2	$S_1=GV_i(1-d), S_2=GV_i d$	3	$GV_i(1-d)$	91.5%
[21]	4/(1-d)	2	5	GV_i	2	$GV_i/2$	4	$GV_i/2$	91.4%
[20]	(N+1)/(1-d)	2	N+1	GV_i	2	$GV_i/5$	N+1	GV_i	92%
Proposed	N/(1-d)	2	N	$C_X=XGV_i/N$ where X=1,2,3..6	2	GV_i/N	N	$2GV_i/N$	94%

4.PULSE WIDTH MODULATION

The best way to switch the power devices of the solar system controller and ensure consistent voltage battery charging is to use pulse width modulation, or PWM. When using PWM regulation, the solar array's current tapers based on the state of the battery and the necessity for recharging. Take a look at a waveform like this one, which shows a voltage transitioning between 0 and 12 volts. It should be very evident that a "suitable device" attached to its output would observe the average voltage and believe it is being fed 6v, or precisely half of 12v, as the voltage is at 12v for exactly the same amount of time as it is at 0v. Therefore, we may adjust the 'average' voltage by changing the positive pulse's width.

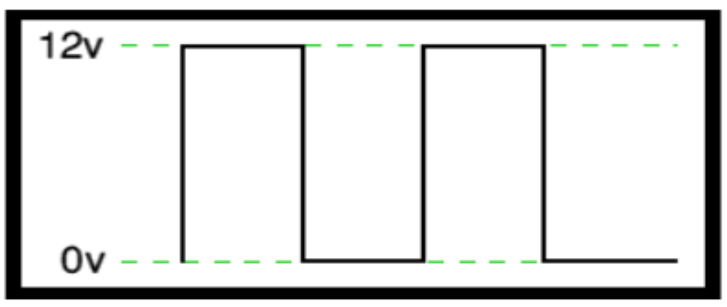

Fig.4.1 Average voltage exactly half of 12v

In a similar vein, the average voltage will be 3/4 of 12v, or 9v, as seen below, provided the switches maintain the voltage at 12 for three times as long as at 0v.

4.1.1 Pulse Width modulator

So, how can a PWM waveform be created? Actually, it's pretty simple; the TEC website has circuits accessible. To begin, create a triangular waveform, as the picture below illustrates. This is contrasted with a d.c. voltage that you may modify to get the desired on/off time ratio. The output rises as the triangle crosses the "demand" voltage. when the voltage of the demand is below the triangle.

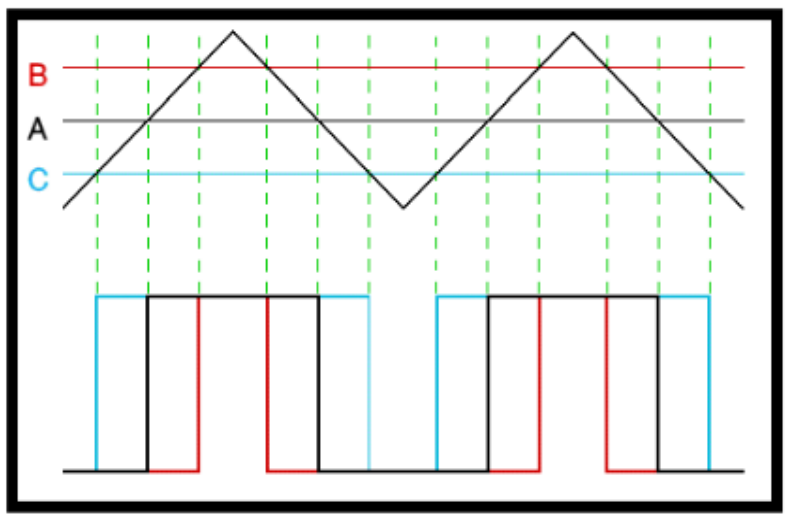

Fig 4.2 Pulse Width modulator Wave form

5.MATLAB DESIGNS AND RESULTS

5.1 SIMULATION CIRCUIT

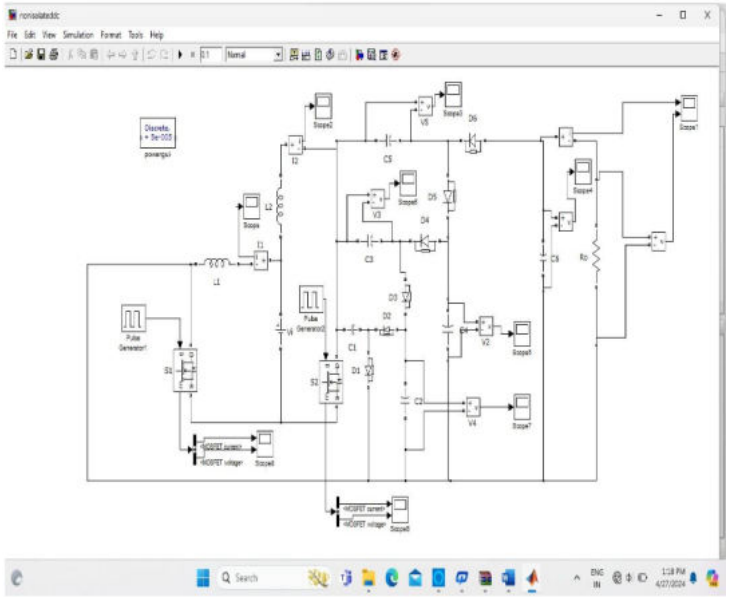

Fig 5.1.1 Simulink Model

5.2 RESULT

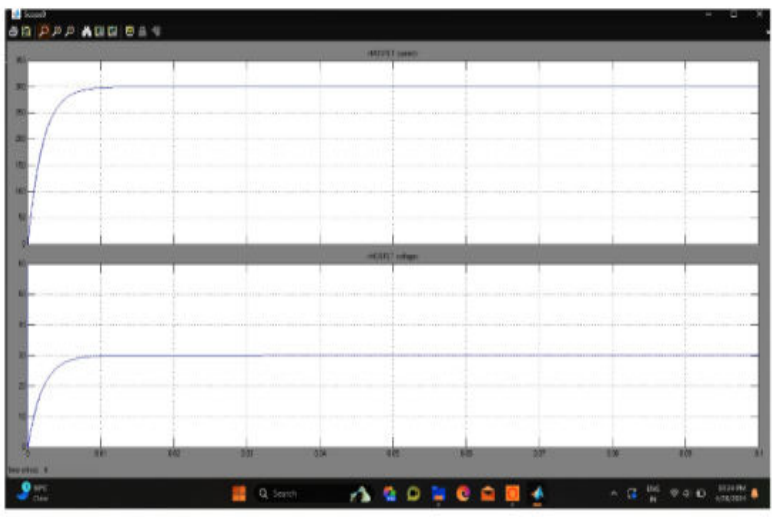

Fig 5.2.1 Switch 1 Output voltage and Output current Waveforms

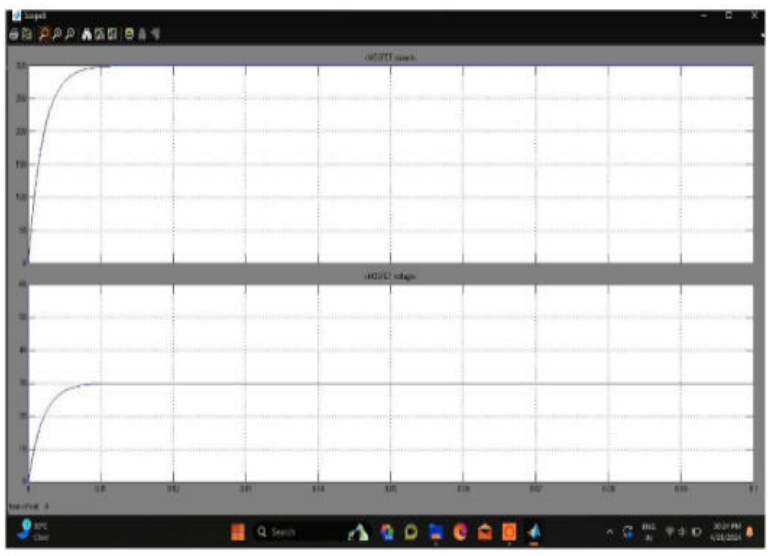

Fig 5.2.2 Switch 2 Output voltage and Output current Waveform

6.CONCLUSION

For use in renewable energy applications, a unique non-isolated current fed interleaved inverting high gain DC-DC power converter is proposed. The converter under study integrates the functionality of diode capacitor stages and interleaved fundamental boost converter. To increase the voltage gain with the least amount of devices, the full-wave voltage multiplier arrangement is included. By adding only one diode and one capacitor for each VM stage increment, the suggested converter may be readily expanded to a larger number of stages to enhance the gain at the same duty cycle. With the use of useful design criteria, the detailed operating modes for CCM and DCM are examined. It has been confirmed that the theoretical and actual voltage improvements at the same duty ratios are about comparable. The predicted converter is even better than the current converter topologies, according on a thorough comparison with the newly suggested alternative converter. Tested at 300W, the constructed prototype's efficiency was found to be 93.07%. The experimental findings were then given to validate the theoretical analysis and performance. The future responsibilities of the proposed converter include closed-loop control, integration with renewable energy systems, gentle switching of semiconductor devices, and voltage stress reduction of semiconductor devices.

7.REFERENCES

[1]Received March 27, 2021,accepeted April 16,2021,date of publication April 20,2021,date of current version April 29,2021.Digital Object Identifier 10.1109/ACCESS.2021.3074459 Non-Isolated Dc-Dc Power Converter With Gain and Inverting capability

[2]B.-C. Kwak and O.-K. Kwon, ‘‘A 2822-ppi resolution pixel circuit with high luminance uniformity for OLED micro displays,’’ J. Display Technol., vol. 12, no. 10, pp. 1083–1088, Oct. 2016.

[3] Texas Instruments. TPS63700 Datasheet. (Jun. 2013). [Online]. Available: http://www.ti.com-/lit/ds/symlink/tps-63700.pdf

[4] S.-W. Hong, S.-H. Park, T.-H. Kong, and G.-H. Cho, ‘‘Inverting buck-boost DC-DC converter for mobile AMOLED display using real-time self-tuned minimum power-loss tracking (MPLT) scheme with lossless soft-switching for discontinuous conduction mode,’’ IEEE J. Solid-State Circuits, vol. 50, no. 10, pp. 2380–2393, Oct. 2015.

[5] M. Jabbari, ‘‘Resonant inverting-buck converter,’’ IET Power Electron., vol. 3, no. 4, pp. 571–577, Jul. 2010.

[6] Y. P. Siwakoti, F. Z. Peng, F. Blaabjerg, P. C. Loh, and G. E. Town, ‘‘Impedance-source networks for electric power conversion Part I: A topological review,’’ IEEE Trans. Power Electron., vol. 30, no. 2, pp. 699–716, Feb. 2015.

[7] T.-J. Liang, J.-H. Lee, S.-M. Chen, J.-F. Chen, and L.-S. Yang, ‘‘Novel isolated high-step-up DC–DC converter with voltage lift,’’ IEEE Trans. Ind. Electron., vol. 60, no. 4, pp. 1483–1491, Apr. 2013.

[8] S. A. Gorji, M. Ektesabi, and J. Zheng, ‘‘Isolated switched-boost push–pull DC–DC converter for step-up applications,’’ Electron. Lett., vol. 53, no. 3, pp. 177–179, Feb. 2017.

[9] F. Evran and M. T. Aydemir, ‘‘Isolated high step-up DC–DC converter with low voltage stress,’’ IEEE Trans. Power Electron., vol. 29, no. 7, pp. 3591–3603, Jul. 2014.

[10] S. Sathyan, H. M. Suryawanshi, A. B. Shitole, M. S. Ballal, and V. B. Borghate, ‘‘Soft-switched interleaved DC/DC converter as front-end of multi-inverter structure for micro grid applications,’’ IEEE Trans. Power Electron., vol. 33, no. 9, pp. 7645–7655, Sep. 2018.

[11] B. R. Lin, ‘‘Modular soft-switching converter in DC micro-grid system applications,’’ Electron. Lett., vol. 54, no. 10, pp. 649–651, May 2018