A HIGH PERFORMANCE LOW POWER 2-4 DECODER DESIGN WITH MIXED LOGIC

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ABSTRACT- This brief introduces a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic, and static complementary metal-oxide semiconductor (CMOS). Two novel topologies are presented for the 2-4 decoder: a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power-delay performance. Both normal and inverting decoders are implemented in each case, yielding a total of four new designs. All IMPLEMENTED decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative DSCH and Micro wind simulation s at 90nm shows that the IMPLEMENTED circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.

I. INTRODUCTION

Static CMOS circuits are used for the vast majority of logic gates in integrated circuits. They consist of complementary nMOS pulldown and pMOS pullup networks and present good performance as well as resistance to noise and device variation. Therefore, CMOS logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes [2]. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design. Pass-transistor logic was mainly developed in the 1990s, when various design styles were introduced [3-6], aiming to provide a viable alternative to CMOS logic and improve speed, power and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual nMOS/pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates. This work develops a mixed-logic design methodology for line decoders, combining gates of different logic to the same circuit, in an effort to obtain improved performance compared to single-style design. Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g. SRAM), multiplexing structures, implementation of boolean logic functions and other applications. Despite their importance, a relatively small amount of literature is dedicated to their optimization, with some recent work including [7-9].

A. CMOS LOGIC

Complementary metal–oxide–semiconductor, abbreviated as CMOS is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. In 1963, while working for Fairchild Semiconductor, Frank Wanlass patented CMOS. CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor (or COS-MOS). The words "complementary-symmetry" refer to the typical design style with CMOS using complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions. Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or N-type metal-oxide-semiconductor logic (NMOS) logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in very-large-scale integration (VLSI) chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminium was once used

but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-κ dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and smaller sizes.

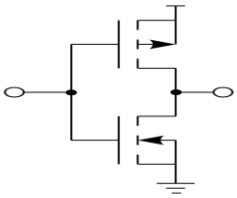
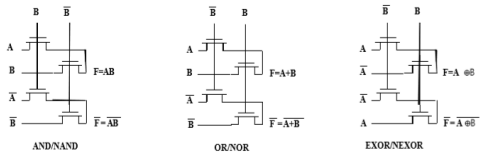


Fig.1. CMOS inverter

B. PTL LOGIC

In electronics, pass transistor logic (PTL) describes several logic families used in the design of integrated circuits. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input. If several devices are chained in series in a logic path, a conventionally constructed gate may be required to restore the signal voltage to the full value. By contrast, conventional CMOS logic switches transistors so the output connects to one of the power supply rails, so logic voltage levels in a sequential chain do not decrease. Simulation of circuits may be required to ensure adequate performance.



PTL performance improvement as alternative low power high speed logic over CMOS logic Pass Transistor Logic (PTL). It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. The layout of 2-bit comparator is developed using automatic and semi-custom techniques. Both the layouts are compared and analyzed in terms of their area consumption. Automatic layout is generated from its equivalent schematic whereas semi-custom layout is optimized manually. The result shows that semicustom layout of PTL logic consumes 35% less area as compared to CMOS logic design to provide area efficient solution.

II. EXITSING LINE DECODERS

A. INTRODUCTION TO LINE DECODERS

In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2^n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines or fewer, if the n-bit coded information has unused combinations. The circuits examined in this work are called n-to-m line decoders, and their purpose is to generate the m = 2^n minterms of n input variables.

B. 2-4 LINE DECODER

A 2-4 line decoder generates the 4 minterms D_{0-3} of 2 input variables A and B. Its logic operation is summarized in Tables. Depending on the input combination, one of the 4 outputs is selected and set to 1 while the others are set to 0. An inverting 2-4 decoder generates the complementary minterms I_{0-3}, thus the selected output is set to 0 and the rest are set to 1, as shown in Table II.

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency. A 2-4 decoder can be implemented with 20 transistors using 2 inverters and 4 NOR gates, as shown in Fig. 2(a). The corresponding inverting decoder can also be implemented with 20 transistors using 2 inverters and 4 NAND gates, as shown in Fig. 2(b).

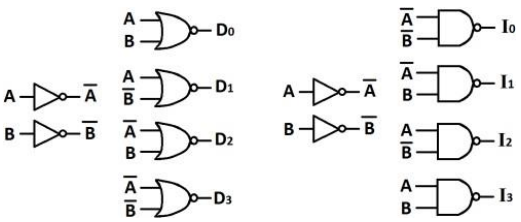


Fig.2. 20-transistor 2-4 line decoders implemented with CMOS logic: (a) Non-inverting NOR-based decoder, (b) Inverting NAND-based decoder.

C. APPLICATIONS OF LINE DECODER

- Memory arrays(eg.SRAM)
- Multiplexing structures
- Implementation of Boolean logic functions.

The process of taking some type of code and determining what it represents in terms of a recognizable number or character is called decoding. Decoder is a combinational circuit that converts binary information into unique output(i,e N inputs to 2**n unique outputs). A common type of decoder is the line decoder which take an n-digit binary number to 2^n data line.

III. IMPLEMENTED MIXED LOGIC LINE DECODERS

A. INTRODUCTION TO NEW MIXED LOGIC LINE DECODERS

In combinational logic, transmission gates have mostly been used in XOR-based circuits such as full adders and as the basic switch element in multiplexers. However, we consider their use in the implementation of AND/OR logic, as demonstrated in [5], which can be efficiently applied in line decoders. The 2-input TGL AND/OR gates are shown in Fig. 3(a) and 3(b), respectively. They are full-swinging, but not restoring for all input combinations. Regarding pass-transistor logic, there are two main circuit styles: those that use nMOS only pass-transistor circuits, like CPL [3] and those that use both nMOS and pMOS pass-transistors, like DPL [4] and DVL [6]. The style we consider in this work is DVL, which offers an improvement on DPL, preserving its full swing operation with reduced transistor count [10]. The 2-input DVL AND/OR gates are shown in Fig. 3(c) and 3(d), respectively. Similar to the TGL gates, they are full-swinging but non-restoring. Assuming that complementary inputs are available, the TGL/DVL gates require only 3 transistors, as opposed to the 4 required in CMOS NAND/NOR gates. Decoders are high fan- out circuits, where few inverters can be used by multiple gates, thus using the TGL/DVL gates can result to reduced transistor count.

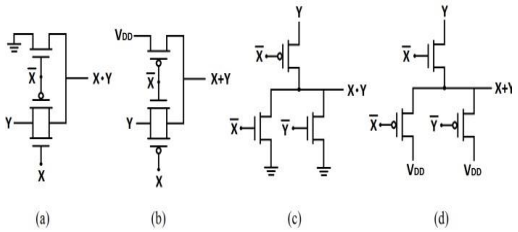


Fig.3. The 3-transistor AND/OR gates considered in this work (a) TGL AND gate, (b) TGL OR gate, (c) DVL AND gate, (d) DVL OR gate.

An important common characteristic of these gates is their asymmetric nature, ie the fact that they do not have balanced input loads. As shown in Fig. 3, we labeled the 2 gate inputs X and Y. In TGL gates, input X controls the gate terminals of all 3 transistors, while input Y propagates to the output node through the transmission gate. In DVL gates, input X controls2 transistor gate terminals, while input Y controls 1 gate terminal and propagates through a pass transistor to the output. We will refer to X and Y inputs as the control signal and the propagate signal of the gate, respectively. This asymmetric feature gives a designer the flexibility to perform signal arrangement, ie choosing which input is used as control and which as propagate signal in each gate. Having a complementary input as propagate signal is not a good practice, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the inhibition (A'B) or implication (A'+B) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND (AB) or OR (A+B) function, either choice is equally efficient. Finally, when implementing the NAND (A'+B') or NOR (A'B') function, either choice results to a complementary propagate signal, perforce.

B. THE 14-TRANSISTOR 2-4 LOW-POWER TOPOLOGY

Designing a 2-4 line decoder with either TGL or DVL gates would require a total of 16 transistors (12 for AND/OR gates and 4 for inverters). However, by mixing both AND gate types into the same topology and using proper signal arrangement, it is possible to eliminate one of the two inverters, therefore reducing the total transistor count to 14. Let us assume that, out of the two inputs, namely A and B, we aim to eliminate the B inverter from the circuit. The D_0 minterm (A'B') is implemented with a DVL gate, where A is used as propagate signal. The D_1 minterm (AB') is implemented with a TGL gate, where B is used as propagate signal. The D2 minterm (A'B) is implemented with a DVL gate, where A is used as propagate signal. Finally, The D_3 minterm (AB) is implemented with a TGL gate, where B is used as propagate signal. These particular choices completely avert the use of the complementary B signal, therefore the B inverter can be eliminated from the circuit resulting in a 14- transistor topology (9 nMOS, 5 pMOS).

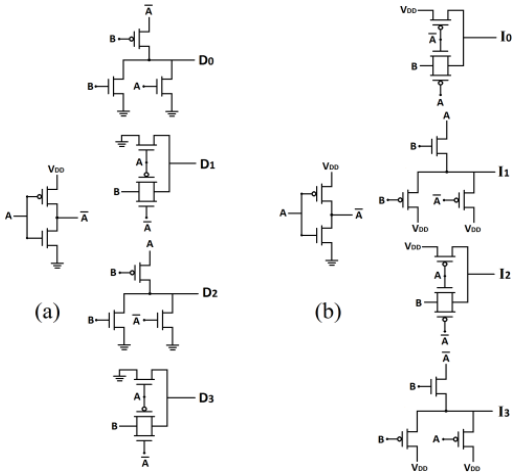


Fig.4. New 14-transistor 2-4 line decoders: (a) 2-4LP (b) 2-4LPI.

Following a similar procedure with OR gates, a 2-4 inverting line decoder can be implemented with 14 transistors (5 nMOS, 9 pMOS), as well: I_0, I_2 are implemented with TGL (using B as propagate signal) and I_1, I_3 are implemented with DVL (using A as propagate signal). The B inverter can once again be elided. The inverter elimination reduces transistor count, logical effort and overall switching activity of the circuits, thereby minimizing power dissipation. As far as the authors are concerned, 14 is the minimum number of transistors required to realize a full-swinging 2-4 line decoder with static (non- clocked) logic. The two new topologies are named '2-4LP' and '2-4LPI', where 'LP' stands for 'low power' and 'I' for 'inverting'. Their schematics are shown in Fig. 4(a) and Fig. 4(b), respectively.

C. THE 15-TRANSISTOR 2-4 HIGH-PERFORMANCE TOPOLOGY

The low-power topologies presented above have a drawback regarding worst case delay, which comes from the use of complementary A as the propagate signal in the case of D_0 and I_3. However, realizing D_0 and I_3 can be implemented more efficiently by using standard CMOS gates, since there is no need for complementary signals. Specifically, D_0 can be implemented with a CMOS NOR gate and I_3 with a CMOS NAND gate, adding one transistor to each topology. The new designs resulting from this modification mix 3 different types of logic into the same circuit and present a significant improvement in delay while only slightly increasing power dissipation. They are named '2-4HP' (9 nMOS, 6 pMOS) and '2-4HPI' (6 nMOS, 9 pMOS), where 'HP' stands for 'high performance' and 'I' for 'inverting'. The reasoning behind the 'HP' designation is that these decoders present both low power and low delay characteristics, therefore achieving an overall good performance. The 2-4HP and 2-4HPI schematics are shown in Fig. 5(a) and Fig. 5(b), respectively, where the additional transistors are highlighted for easier distinction.

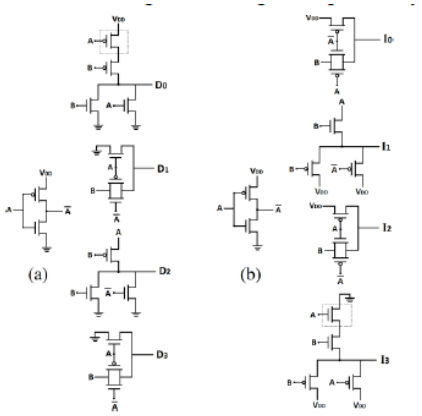


Fig. 5. New 15-transistor 2-4 line decoders: (a) 2-4HP (b) 2-4HPI.

IV. SIMULATION RESULTS

The simulations were done using DSCH and microwind with a power supply of 1V. Simulation result and digital schematic of some of the operation using full swing GDI technique are given below using DSCH 3.5 tool.

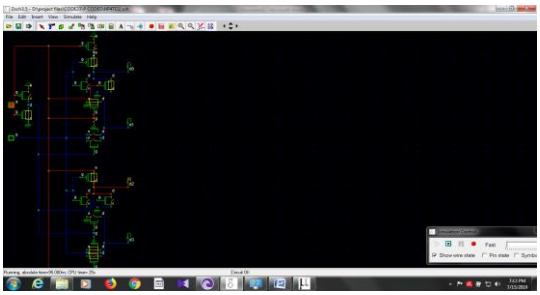


Fig.6. 2-4 HP decoder function

The above Figure shows the schematic circuit of Implemented 2-4 HP of low power, high performance line decoder circuits were designed using 90nm CMOS process in Microwind, the size of PMOS is triple that of the NMOS transistor size to achieve the best power and delay performance.

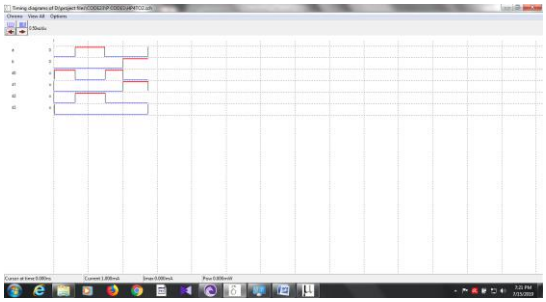


Fig.7 HP2-4 decoder Timing diagram

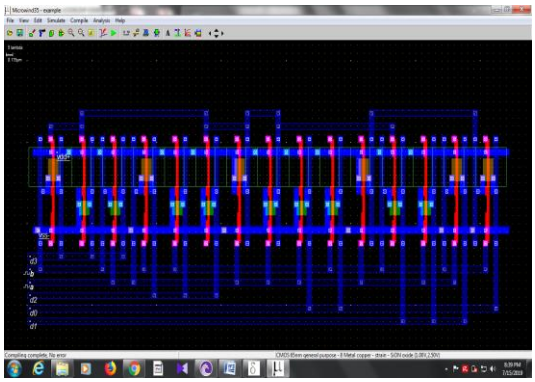


Fig.8 HP 2-4 decoder verilog compilation

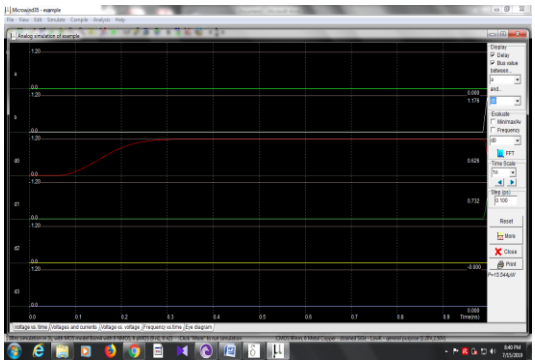


Fig.9 HP2-4 decoder simulation output

The above Figures shows the2-4 HP decoder circuit layouts are generated in DSCH will complied and simulation results performed by the showing their full swinging capability despite using pass-transistor gates.

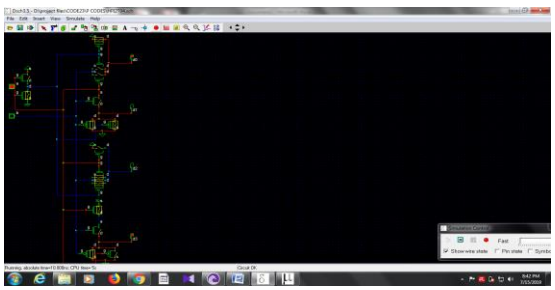


Fig.10 HPI 2-4 decoder function

The above Figure shows the schematic circuit of Implemented 2-4 HPI of low power, high performance line decoder circuits were designed using 90nm CMOS process in Microwind, the size of PMOS is triple that of the NMOS transistor size to achieve the best power and delay performance.

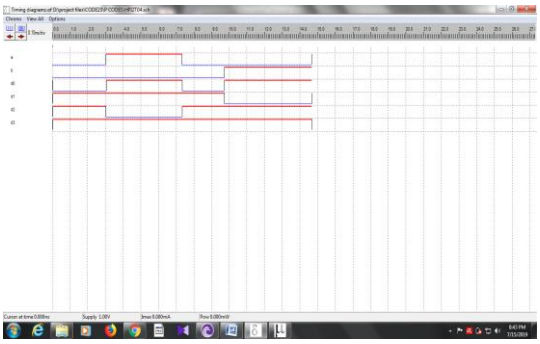


Fig.11 HPI 2-4 decoder Timing Diagram

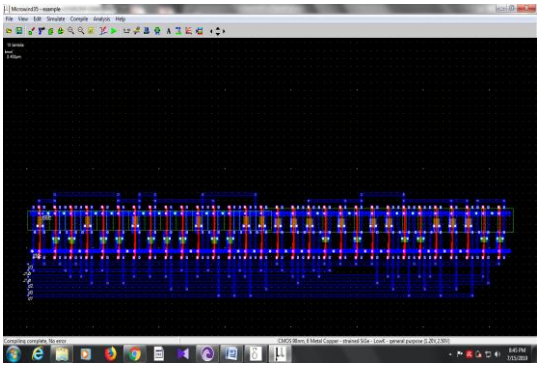


Fig.12 HPI 2-4 Decoder verilog compilation

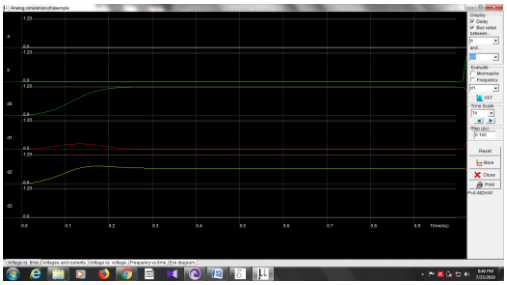


Fig.13 HPI 2-4 Decoder simulation output

The above Figures shows the2-4 HPI decoder circuit layouts are generated in DSCH will complied and simulation results performed by the showing their full swinging capability despite using pass-transistor gates.

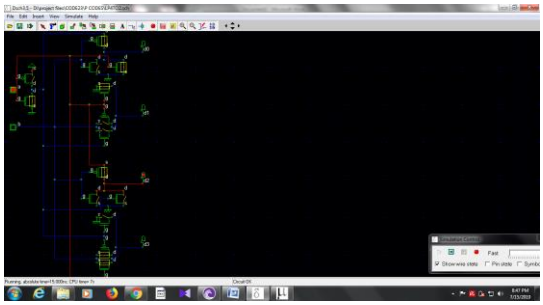


Fig.14 LP 2-4 Decoder function

The above Figure shows the schematic circuit of Implemented 2-4 LP of low power, high performance line decoder circuits were designed using 90nm CMOS process in Microwind, the size of PMOS is triple that of the NMOS transistor size to achieve the best power and delay performance.

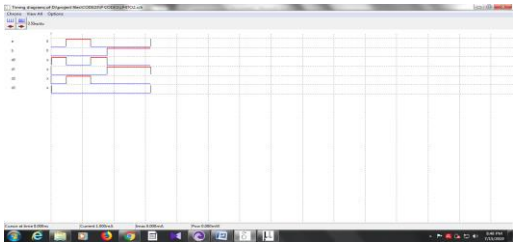


Fig.15 LP 2-4 Decoder Timing Diagram

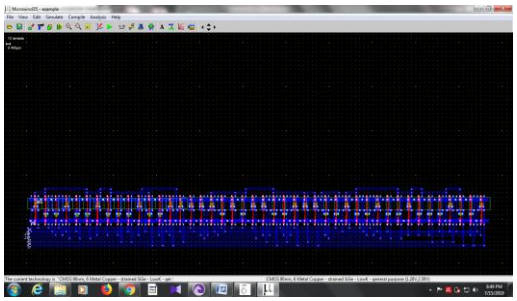


Fig.16 LP 2-4 Decoder verilog compilation

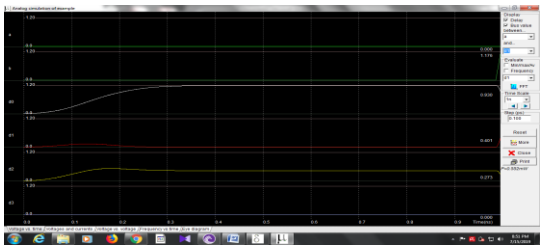


Fig.17 LP 2-4 Decoder simulation output

The above Figures shows the2-4 LP decoder circuit layouts are generated in DSCH will complied and simulation results performed by the showing their full swinging capability despite using pass-transistor gates.

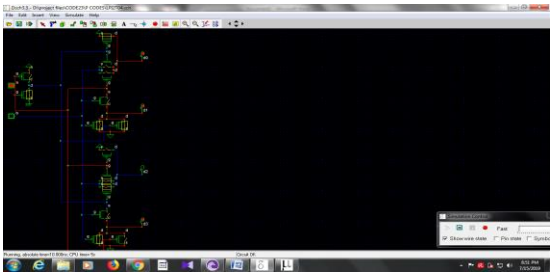


Fig.18 LPI 2-4 Decoder function

The above Figure shows the schematic circuit of Implemented 2-4 LPI of low power, high performance line decoder circuits were designed using 90nm CMOS process in Microwind, the size of PMOS is triple that of the NMOS transistor size to achieve the best power and delay performance.

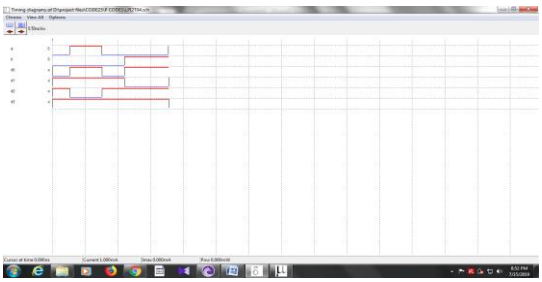


Fig.19 LPI 2-4 Decoder Timing Diagram

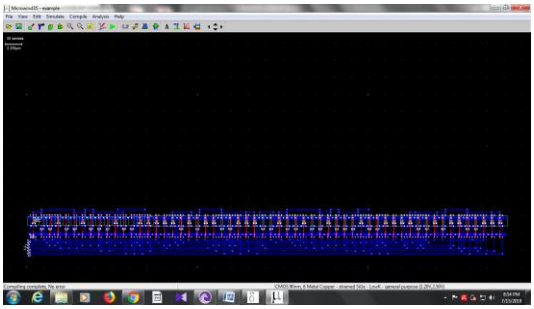


Fig.20 LPI 2-4 Decoder verilog compilation

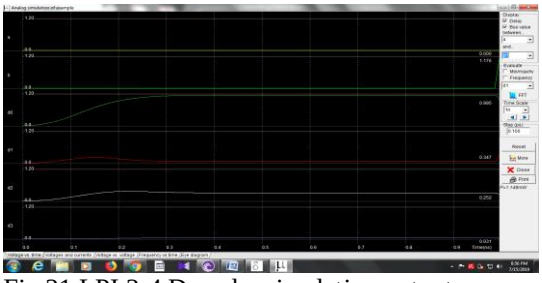


Fig.21 LPI 2-4 Decoder simulation output

The above Figures shows the 2-4 LPI decoder circuit layouts are generated in DSCH will complied and simulation results performed by the showing their full swinging capability despite using pass-transistor gates.

Synthesis Results Table:(2-4 Decoder)

System	Design	No of transistors	Power(mw)
Existing	CMOS	20	0.0316
	CMOS INV	20	0.0346
Proposed (Implemented)	2-4LP	14	0.0140
	2-4LP INV	14	0.0279
	2-4HP	15	0.0155
	2-4HP INV	15	0.0273

V. CONCLUSION

An efficient mixed-logic design for decoder circuits, combining TGL, DVL and static CMOS. By using this methodology, we developed four new 2-4 line decoder topologies, namely 2-4LP, 2-4LPI, 2-4HP and 2- 4HPI, which offer reduced transistor count (therefore potentially smaller layout area) and improved power-delay performance in relation to conventional CMOS decoders. These designs combine the improved performance characteristics of pass transistor logic with the restoring capability of static CMOS. A variety of comparative spice simulations was performed at the 90 nm, verifying, in most cases, a definite advantage in favor of the IMPLEMENTED designs. The 2-4LP topologies are mostly suitable for applications where area and power minimization is of primary concern. The 2-4LPI, 2-4HP and 2-4HPI, proved to be viable and all-around efficient designs, thus they can effectively be used as building blocks in the design of larger decoders, multiplexers and other combinational circuits of varying performance requirements. Moreover, the presented reduced transistor count and low power characteristics can benefit both bulk CMOS and SOI design as well. The obtained circuits are to be implemented on layout level, making them suitable for standard cell libraries and RTL design.

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