IMPROVEMENT OF POWER QUALITY IN DISTRIBUTION NETWORK BY USING DSTATCOM

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ABSTRACT- To maintain the easy installation feature and reasonable costs, it is convenient to set the PCC voltage, in which the processed power is minimal, without monitoring any load or grid information and using only internal signals of the DSTATCOM, such as the PCC voltages and DSTATCOM output currents. Voltage-controlled DSTATCOM can maintain the PCC voltages balanced even under grid or load unbalances. It proposes the concept of minimum power point tracking (mPPT) and the frequency loop combination of both loops, providing to the power company a solution for the poor voltage regulation in real distribution grids with superior PCC voltage quality. The mPPT avoids unnecessary reactive compensation, increasing the compensation capability. The frequency loop overcomes the practical difficulty of synchronization by correcting the frequency of the voltage reference. The control strategy aims to synthesize the balanced voltage waveforms at PCC with adequate amplitude and also regulate the voltage of the dc bus capacitors. Further to improving the voltage stability in the distribution grids by using PR control strategy. MATLAB/SIMULINK Simulation results showed the validity and efficiently of the proposed control approach in different conditions.

I. INTRODUCTION

In power system analysis, load behaviour has not attained the same attention from researchers as generation and transmission studies. However, there are cases when unexpected load properties are known to have caused large problems, for example in the Swedish blackout in December 1983 where the loads made the system unstable. In the simulation following the blackout, the first calculations showed that the system should have stayed stable but it was later understood that after the initial drop in power demand, due to the voltage drop, the loads recovered due to the voltage restoration by the on-load tap changers in transformers. Many studies have highlighted this behaviour, among them, which performed measurements in the power system and tried to determine the parameters of the load recovery in the range of minutes. Among the first to study the dynamic performance of systems with a time scale of less than a second. However, the dynamic properties and the time scale in focus in this thesis are determined by power electronic based loads which can react to changes in the range of milliseconds.

The power electronics considered is mainly self-commutated semiconductor switches like the IGBT. In distributed DC systems, often used on ships or aircraft, power electronic based loads with fast dynamics is a well studied topic, known to cause operation problems. With the increasing number of power electronic loads in AC systems, caution has to be taken to ensure satisfying safety margins also in AC distribution and transmission systems. So far, stability criteria studies similar to those for DC systems have not been common for AC systems. In AC systems, the impact of load dynamics on system performance in systems with or without voltage compensators is gaining increasing attention from researchers, although the dynamic loads mostly considered are induction machines. Power electronic based loads have different dynamic properties than induction machines and it is therefore important to investigate the impact from these types of loads.

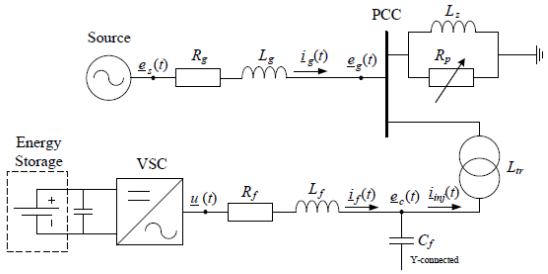

Fig:1. Grid model with supply, line impedance, constant power load and D-STATCOM connected through a LCL-filter.

Connecting a D-STATCOM to the PCC through a LCL-filter gives a grid model which can be seen in Figure 1. This grid model is very simplified compared to a real grid. Furthermore, both the load and the compensator are connected right at the PCC which means that there is nothing that can decouple the controllers. In fact, this is the worst condition since there are nothing to slow down the changes, hence the risk for interaction is increased. The converter-side filter inductance is denoted Lf , the filter capacitance is denoted Cf

while the grid-side filter inductance, constituted by the leakage inductance of the injection transformer, is denoted Ltr. Voltages and currents are denoted and directed according to Figure 1, i.e. a positive current (power) is hence obtained when injected into the PCC.

II. SYSTEM MODELING

To meet the voltage regulation requirement, a voltage-controlled DSTATCOM-based voltage regulator is proposed with shunt connection to PCC, as shown in Fig. 2. The shunt connection avoids power supply interruption while the voltage regulator is installed or disconnected. The proposed DSTATCOM allows the power company to postpone investments and enhances the flexibility of grid management. Voltage-controlled DSTATCOM can maintain the PCC voltages balanced even under grid or load unbalances. The PCC voltage is directly controlled by the DSTATCOM and sudden load changes have no significant impact in the PCC voltage waveforms. Moreover, the voltage-controlled DSTATCOM decouples the grid and the loads, serving as a low impedance path for harmonic distortions due the voltage source behavior. Current harmonic distortions from the loads have small impact in the grid and vice versa. The grid current quality, therefore, is exclusively given by the grid voltage quality.

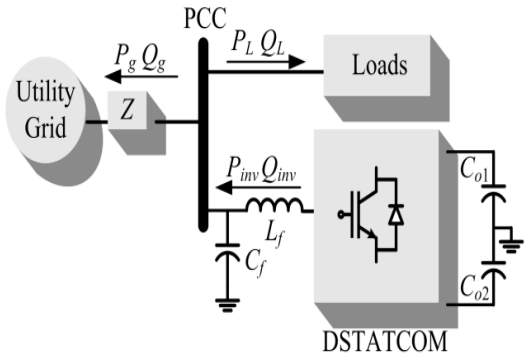

Fig:2. Low voltage distribution grid under analysis with the voltage regulator

According to angular position reference is required for the voltage-controlled DSTATCOM to work properly. Before the DSTATCOM starts its operation, synchronization circuits generate the angular position to the voltage regulator. Once the operation begins, the voltage-controlled voltage regulator replaces the PCC voltage and the grid voltage frequency and angle are no longer available. PCC voltage frequency and angle are then determined by the voltage regulator. For a real application, due to the distance between the transformer and the PCC, only the PCC voltage should be measured to compose the voltage reference of the DSTATCOM. In past years, the PCC voltage amplitude (VPCC) for reactive compensation methods was usually adopted as the nominal grid voltage, i.e. 1.00 p.u. However, Brazilian grid code determines a maximum (1.05 p.u.) and a minimum (0.92 p.u.) voltage amplitude for low voltage distribution grids. The PCC amplitude can be viewed as a degree of freedom and the processed power can be reduced with a suitable control loop. In this effort, proposes a new method to determine the suitable PCC terminal voltage for reduction of the DSTATCOM power rating. The method is formulated according to the desired source current, aiming to achieve the unity power factor at the grid. However, this method requires information about the source current, grid resistance and reactance. In the authors propose another method to determine suitable VPCC using the positive sequence components of the load current to compute the PCC voltage. In both cases, additional information is required, increasing the process complexity, number of sensors and the cost of the solution. To maintain the easy installation feature and reasonable costs, it is convenient to set the PCC voltage, in which the processed power is minimal, without monitoring any load or grid information and using only internal signals of the DSTATCOM, such as the PCC voltages and DSTATCOM output currents.

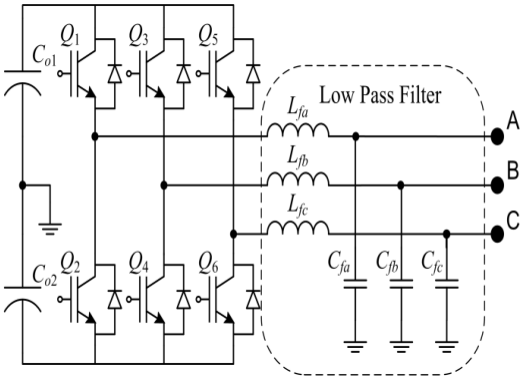

Fig:3. Three-phase four-wire VSI with LC low-pass filter

This project presents a voltage-controlled DSTATCOM-based voltage regulator for low voltage distribution grids, using a three-phase four-wire VSI with an LC low-pass output filter, as shown in Fig. 3. Operation principles of the voltage-controlled DSTATCOM and the control strategy are presented. Additionally, two loops are included to the proposed control strategy: the concept of minimum power point tracking (mPPT) and the frequency loop. The mPPT avoids unnecessary reactive compensation, increasing the

compensation capability. The frequency loop overcomes the practical difficulty of synchronization by correcting the frequency of the voltage reference. This project proposes the combination of both loops, providing to the power company a solution for the poor voltage regulation in real distribution grids with superior PCC voltage quality. Simulation results confirm the effectiveness of the voltage regulator and the features of both loops, separately and simultaneously.

Voltage-controlled DSTATCOMs replace the PCC with three balanced voltage waveforms, adjusting their phase as the load and the dc bus require. The numerical solution of helps in the power rating design of the voltage regulator. For this paper, the DSTATCOM power rating was chosen as 1.0 p.u., the nominal load power. Taking into account the PCC voltage reduction performed by the mPPT algorithm, shows the DSTATCOM is able to compensate 1.0 p.u. load power with PCC voltage equal to 0.93 p.u.

A. MINIMUMPOWER POINT TRACKER

The voltage amplitude to be regulated at PCC changes the power flow between the grid, load and DSTATCOM. Suitable VPCC makes the processed apparent power be minimal. When the VPCC is between the desired voltage limits, the mPPT minimizes the converter apparent power and no reactive power at the grid frequency is processed. Apparent power minimization means current minimization, which lower the losses and extends the equipment life cycle. For the mPPT analysis, apparent power is chosen to be minimized instead of reactive power due to: (i) active power in DSTATCOMs is a small fraction of the apparent power; (ii) the harmonic currents from the grid and load are also processed; (iii) the converter power rating and the losses are given by the apparent power; and (iv) apparent power is easier to calculate in comparison to extracting the reactive power at the grid frequency from distorted current waveforms.

1. The P&O-based mPPT Algorithm

The reduction of voltage regulator apparent power can be performed by tracking algorithms. An example of tracking algorithm is the Maximum Power Point Tracker (MPPT), which is widely used in PV systems. Among several MPPT algorithms, the Perturb & Observe (P&O) method was chosen to compose the mPPT algorithm due to its simplicity, low computational effort and a small number of sensors, although it has slow transient response and operates around a Maximum Power Point (MPP), which can be a local or a global MPP.

Two parameters must be set to the P&O algorithm: perturbation amplitude and sample time. The perturbation amplitude defines the convergence time to reach the MPP and the amplitude of the oscillations in steady state. The sample period must be greater than the response time of the system to avoid instabilities. One interesting feature of the P&O method is its independency of PV arrays parameters. This feature makes the P&O not restricted to PV systems. The P&O-based mPPT algorithm presents the same features of the P&O algorithm applied to MPPT, but is designed to achieve the Minimum Power Point (mPP) instead of MPP. The mPPT can be derived analyzing. The marker 1 represents an increase of *VPCC* and the marker 4 represents a decrease of *VPCC* which leads to reduction of the *Sinv*. In these cases, the next perturbation will conserve the perturbation signal (positive for marker 1 and negative for marker 4) and the mPPT will converge to the mPP. On the other hand, the marker 2 represents a decrease of *VPCC* and the marker 3 represents an increase of *VPCC* diverging from mPP. Therefore, the direction of the next perturbation must be positive for marker 2 and negative for marker 3. Comparing the perturbation logic of the P&O mPPT with the conventional P&O MPPT algorithm, one can conclude that the P&O-based mPPT can be obtained by simply changing the perturbation signal of the conventional P&O MPPT. The processed power at the mPP was intentionally considered as *Smin*, the minimal power to be processed. DSTATCOM losses and harmonic distortions contributions to the apparent power cannot be minimized to zero.

2. The Amplitude Loop

The amplitude loop is composed of the P&O-based mPPT algorithm and has voltage constraints to meet, which are imposed by the Brazilian grid code. The voltage constraints are not considered and directly affect the apparent processed power. There are three different cases when voltage constraints are present as depicted. In case 1, *Smin* requires a *VPCC* below the minimum allowable PCC voltage (*Vmin*). The mPPT goes toward the mPP, but *VPCC* cannot be lower than *Vmin*. *VPCC* is kept at *Vmin* and the voltage regulator supplies reactive power to maintain the *VPCC* regulated. Therefore, the mPP in case 1 will be at mPPL and the processed power is represented by *SminL*. The Case 3 shows a similar outcome to case 1 with *VPCC* kept at the maximum allowable PCC voltage (Vmax). The converter operates at mPPH and process reactive power equal to *SminH*.

In case 2, the mPP occurs with *VPCC* between *Vmax* and *Vmin*. The mPPT tracks the mPP and the converter process *Smin*, the active power to compensate the losses and the harmonic distortion from the grid and load.

B. FREQUENCY LOOP

The grid frequency has small frequencies deviations around the nominal value and many loads can operate under such deviations. However, voltage-controlled DSTATCOM synthesizes the PCC voltage with a constant frequency. Large differences between the grid and PCC frequencies, associated with long frequency deviations, may lead to disconnection of the DSTATCOM. Differences between *fg* and *fPCC* have two impacts on the voltage regulator: dc bus voltage steady state error and nonconstant total dc bus voltage controller output. The steady state error depends on the total dc bus controller design and frequency perturbation magnitude. If the steady state error is positive, dc bus overvoltage can be higher than the capacitors' rated voltage. If negative, the modulation index can be close the unity, reducing the PCC voltage quality. When the controller is implemented in analog circuits, the non constant control output must be constrained to the analog voltage limits. Once the compensation angle (θ) reaches the constraints, the angle is kept to the limit value.

C. CONTROL STRATEGY

The control strategy aims to synthesize three balanced voltage waveforms at PCC with adequate amplitude, low THD and also regulate the voltage of the dc bus capacitors. Therefore, the control strategy has three output voltage loops, one total and one differential dc bus voltage loop. The aforementioned controllers were designed with the parameters presented and evaluated for a range of the grid impedance (0.1 to 10 of *Rg* and *Lg*) through frequency response analysis. In this range the designed controllers work properly. Additionally, this paper includes two loops: a loop responsible for the PCC voltage amplitude and another one responsible for mitigating the grid frequency effect on the voltage regulator. Fig. 4 shows the complete control block diagram with the amplitude and frequency loops.

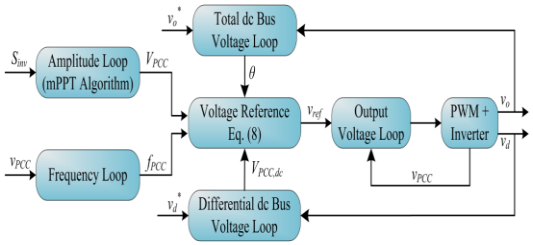

Fig:4. Proposed control strategy including amplitude and frequency loops.

1. Output Voltage Loop

The inputs of the output voltage loop are three voltage references (*vref*). The voltage references are composed of the dc bus controllers output, the mPPT and the frequency loop, as depicted in Fig.4. To achieve adequate synthesis of the voltage references, the output voltage loop must have fast dynamic response. The output controller is a PID controller. The simplified output voltage loop block diagram can be seen in Fig. 5. The output voltage loop has active damping controllers to enhance the stability of the voltage regulator against grid impedance variations.

2. Grid Frequency Variation and the Total dc Bus Controller

The DSTATCOM operation causes power losses in the power converter as a result of semiconductor switching. The losses diminish the total dc bus voltage (*vo*). As the displacement angle θ determines the active power flow at the PCC. Therefore, the total dc bus loop compares *vo* to the reference *vo** and, through a PI plus pole controller, set a suitable θ to drain active power from the grid and reestablish the power balance between the grid, the loads and the DSTATCOM. The DSTATCOM is composed of three-phase four-wire VSI and the voltage balance at the split capacitors is required. The difference between the split capacitor voltages (*vd*) is compared to the reference (*vd**) and a PI plus pole contributes to the reference generator with a small dc component (*VPCC,dc*). This dc component charges one capacitor more than the other and the voltage balance can be achieved.

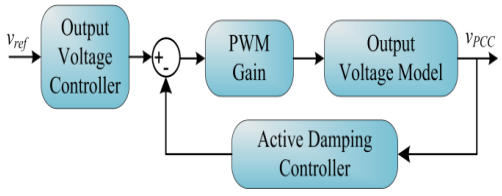

Fig:5. Output voltage loop block diagram

III. SIMULATION RESULTS

Case:1- Grid Frequency Variation Impacts

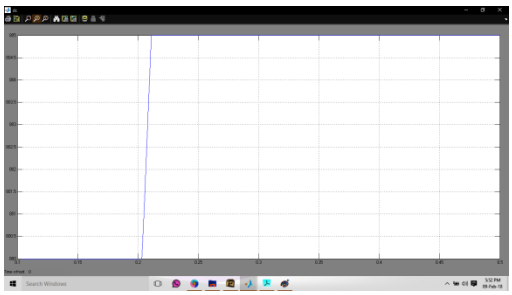

Fig:6(a)

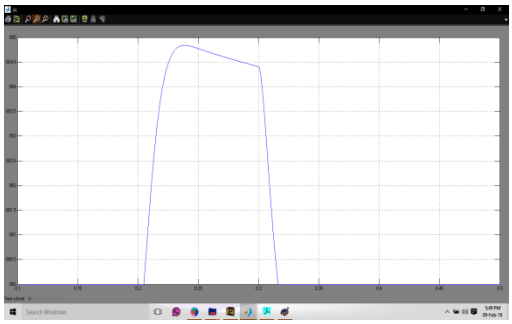

Fig:6(b)

Fig:6. Total dc bus voltage during the grid frequency variation: (a) without and (b) with the frequency compensation

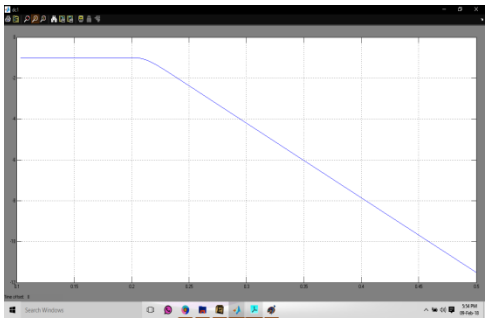

Fig:7(a)

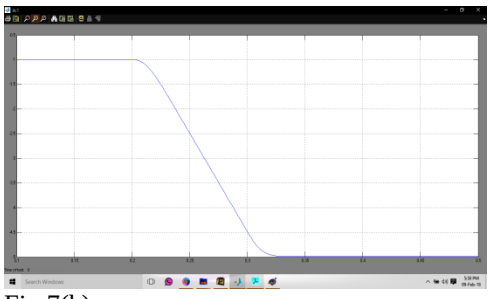

Fig:7(b)

Fig:7. Compensation angle during the grid frequency variation: (a) without and (b) with the frequency compensation

The effect of the grid frequency step on the total dc bus voltage can be seen in Fig. 7 (a). The dc bus voltage has low steady state error (around 6 V) because of a large total dc bus voltage controller bandwidth. With the *fref* update, Fig. 7 (b), the total voltage returns to nominal voltage. After the frequency step, the total voltage controller has a slope output. Without *fref* update, Fig. 7 (a), the compensation angle decreases indefinitely, whereas with the frequency loop the compensation angle is constant, as shown in Fig. 7 (b). However, the compensation angle does not return to the previous value. Errors between *fref* and *fPCC* are accumulated in the compensation angle and the controller output may reach its limits. If imminent, a protective routine is activated, which adds a constant factor to *fref*, bringing the compensation angle back to 0 radians. After that, the frequency loop returns to normal operation.

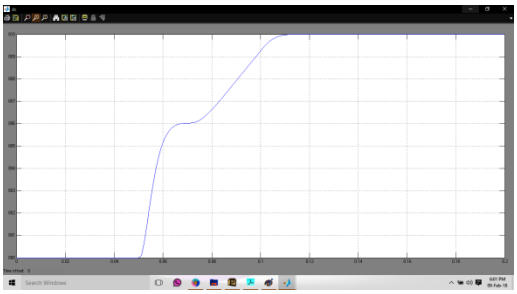

Fig:8 Dc bus voltages during the DSTATCOM initialization

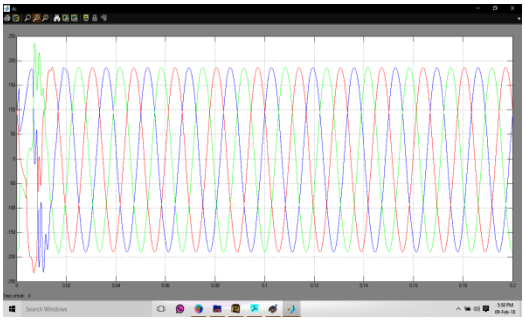

Fig:9. PCC voltages without compensation for linear loads

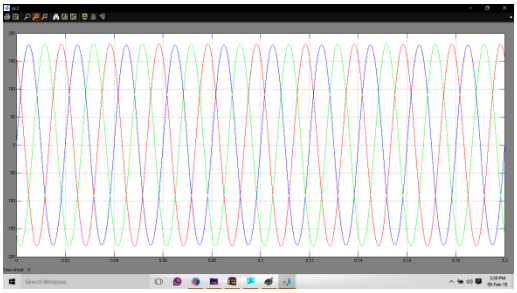

Fig:10. PCC voltages with compensation for linear loads

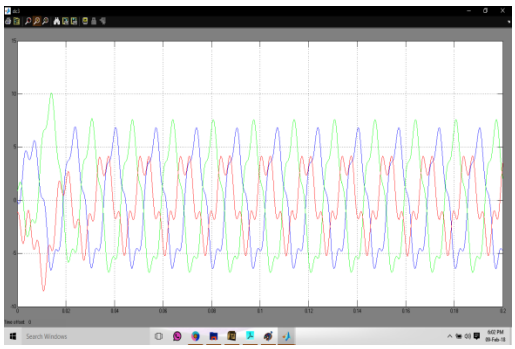

Fig:11. Voltage regulator currents for linear loads

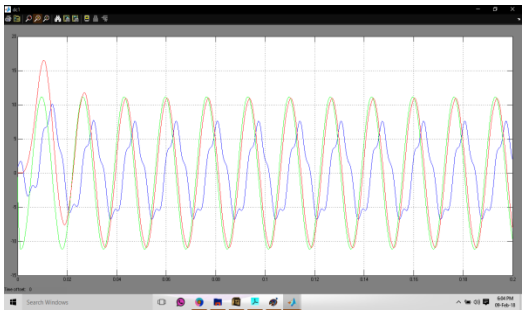

Fig:12. Grid, load and voltage regulator currents for linear loads

At the time *t*0 the auxiliary contactor (AC) closes and inserts the pre-charge resistors (PCR) in series with the DSTATCOM while the PWM is maintained disabled. The dc bus charges through the switches diodes, as shown in Fig. 8. Meanwhile, the PLL circuit synchronizes the voltage references with the PCC voltages. The PCC voltage amplitude without compensation is 212 V according to Fig. 9. One can see that the PCC voltages contain some harmonic distortion inherent to low voltage distribution grids. The compensated PCC voltage was arbitrarily chosen as 220 V. The PCC voltages are regulated with low THD (0.2%), as shown in Fig. 10. The compensation currents have different rms values for each phase, highlighting the natural unbalance of the low voltage grids. The harmonic distortion present in the grid voltage is compensated by the regulator. Fig. 11 presents the compensation current waveforms. The quality of the *b*-phase grid current (*igb*) for linear loads is shown in Fig. 12. The voltage regulator supplies the load with low THD voltages, as seen by the load current (*iLb*). The harmonic content in *igb* is given by the grid voltage distortions.

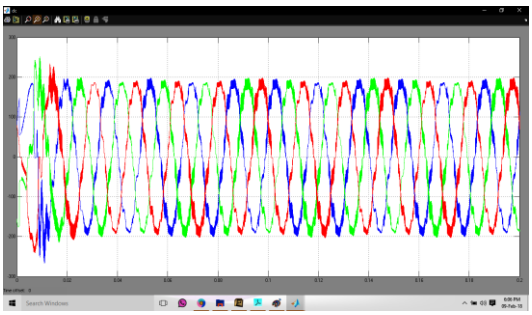

Fig:13. PCC voltages without compensation for nonlinear loads

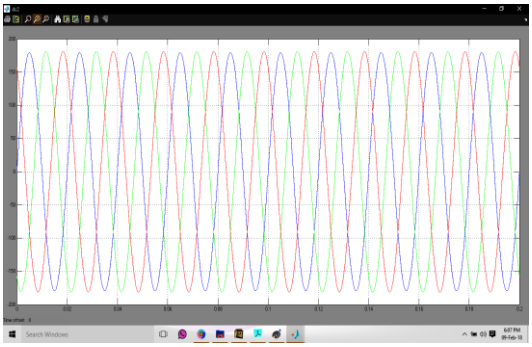

Fig:14. PCC voltages with compensation for nonlinear loads

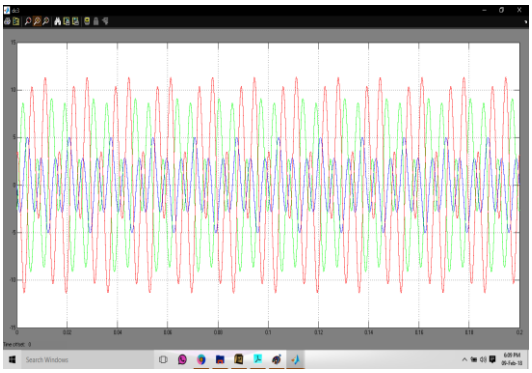

Fig:15. Voltage regulator currents for nonlinear loads

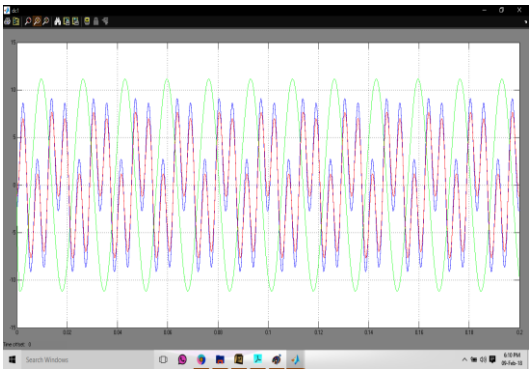

Fig:16. Grid, load and voltage regulator currents for nonlinear loads

The considered nonlinear loads are three 2 kVA single-phase rectifiers with a capacitive filter, one in each phase added to 5.2 kW three-phase resistive loads. The PCC voltage amplitude without compensation is 203 V with 6.4% THD. The compensated PCC voltage is depicted having three regulated and sinusoidal waveforms with 0.6% THD. The compensation currents contain the fundamental frequency for the reactive compensation and all the harmonic distortion from the nonlinear loads. The *b*-phase grid current (*igb*) waveform for nonlinear load. The voltage regulator absorbs the harmonic content from the load current (*iLb*) leaving *igb* free of load harmonic distortions. Comparing *igb*, one can notice the grid current waveforms present similar distortions from the grid voltage.

IV. CONCLUSION

A three phase DSTATCOM as a voltage regulator and its control strategy, composed of the conventional loops, output voltage and dc bus regulation loops, including the voltage amplitude and the frequency loops. Simulation results demonstrate the voltage regulation capability, supplying three balanced voltages at the PCC, even under nonlinear loads. The proposed amplitude loop was able to reduce the voltage regulator processed apparent power about 51 % with nonlinear load and even more with linear load (80%). The mPPT algorithm tracked the minimum power point within the allowable voltage range when reactive power compensation is not necessary. With grid voltage sag and swell, the amplitude loop meets the grid code. The mPPT can also be implemented in current-controlled DSTATCOMs, achieving similar results. The frequency loop kept the compensation angle within the analog limits, increasing the autonomy of the voltage regulator, and the dc bus voltage regulated at nominal value, thus minimizing the dc bus voltage steady state error. Simultaneous operation of the mPPT and the frequency loop was verified. The proposed voltage regulator is a shunt connected solution, which is tied to low voltage distribution grids without any power interruption to the loads, without any grid voltage and impedance information, and provides balanced and low-THD voltages to the customers.

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