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IMPACT OF HIGH-K SPACER ON DEVICE PERFORMANCE OF A JUNCTION LESS TRANSISTOR

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ABSTRACT

In this paper, radio frequency (RF) stability performance of double gate junction less transistor for different spacer material, the width of spacer, and bias conditions is reported. The impact of gate oxide thickness and gate work function on RF performance of double gate junction less transistor is also presented. The analog and RF figure of merit, namely, intrinsic gain, unity gain cut-off frequency, stern's stability factor, critical frequency, maximum attainable gain, and maximum stable gain, are investigated with the help of numerical simulation. The result shows that the fringing fields of high *k* spacers have a major impact on the gate to source and gate to drain capacitance. The device design guideline along with bias and geometrical parameters are reported for the optimized structure. The optimized device structure exhibits better RF stability.

1.0 INTRODUCTION

In 22nd century, Silicon on Insulator was known as Integrated Circuit Technology. According to International Technological road map MOSFET channel length should reduce. Short channel effect has problems such as increase in subthreshold swing, decrease in Ion/Ioff ratio, drain induced barrier lowering, and trans conductance etc. These short channel effect problems can be overcome by different types of transistors. At the time of formation of source and drain junction while using doping profile [3], thermal budget poses [16] big challenge. However, junction less transistor is best candidate for improving short channel effect problem because of very low thermal budget. This was reviewed in the literature. Junctionless transistor is simpler compared to inversion model MOSFET because of junction less fabrication procedure. Double gate junction less transistor is best candidate for CMOS technology [2]. However, junction less

transistor suffers from less drain current and transconductance due to high doping concentration in the channel region.

Dual material gate (DMG) junction less transistor improves transconductance and carrier transport efficiency. Peak electric field [14] at source side accelerates more electrons due to DMG structure due to which current driving capability increases. designed two dimensional analytical model for channel potential of DMG SOI Transistor [11] in order to improve short channel effect problem. Hougin demonstrated dual material gate junction less nanowire transistor which showed significant improvement in transconductance, output conductance and cut off frequency in comparison with single material gate junction less nanowire transistor [7].

2.0 EXISTING SYSTEM

The scaling of gate length in the bulk MOSFETs, then efficiency of the gate control decreases in the channel. In order to overcome this limitation, various device structures such as fully depleted SOI FETs as well double gate and multiple gates FET have been proposed, due to ability to suppress short channel effects. In such devices, however ultra-shallow source/drain junction fabrication is becoming one of the main in view of the required process steps and related thermal budget [8]. However, the formation of ultra-sharp junctions between source drain and channel becomes complex when the channel length of classical multi gate MOS transistors is scaled down to extreme dimensions. Existing transistors are supported the employment of semiconductor junctions[3]. due to the laws of diffusion [7] and therefore the applied mathematics nature of the distribution of the doping atoms within the semiconductor, the formation of extremist shallow junctions with high doping concentration gradients [3] has become associate more and more troublesome challenge for the semiconductor business. A solution to this problem in the form of novel structure called ―Junctionless multi gate transistor.

3.0 PROPOSED SYSTEM

Recently, the concept of the junction less (JL) nanowire transistor, which contains a single doping species[8] at the same level in its source, drain, and channel, is investigate. The JL device is basically a gated resistor, that is, it is a resistor with a gate that controls the carrier density and hence the current flow. Normally, the JL device works like a low-resistance resistor [3], and the application of a gate voltage allows the semiconductor film of carriers to be depleted, thereby modulating its conductivity. Ideally, it should be possible to completely deplete the

semiconductor film of carriers, in which case the resistance of the device approaches to infinite. The advantages of JL devices include:

1) avoidance of the use of an ultra-shallow source/drain junction [12], which greatly simplifies the process flow;

2) low thermal budgets owing to implant activation [14] anneal after gate-stack formation is eliminated; and

3) the current transport is in the bulk of the semiconductor, which reduces the impact of imperfect semiconductor/insulator interfaces. Although a JL device with bulk substrate, which provides the absence of an SOI wafer to lower the cost, and improves scalability and full compatibility with the industry standard bulk CMOS process flow[5], is also proposed, there still lacks a comprehensive study of both n-type and p-type Si bulk substrate JL devices [12] in performance estimating and device design [6]. Additionally, most of the studies focused on the device performance estimation of JL transistors, but few addressed the circuit application of such device

4.0 TECHNIQUES USED

Drain induced barrier lowering

Ideally, we want to work the MOSFET in 1-D mode, i.e., solely gate voltage dominant this of the device. But, because the channel lengths area unit going tiny, the drain starts to behave as a second gate, i.e., ID isn't solely controlled by the gate voltage however is additionally controlled by the drain voltage. This is often known as because the 2- D behavior [12] of the semiconductor. During a long channel device any increase in VDS [15], is accounted by lowering the band solely within the drain facet. Because the channel length is minimized this increase in VDS account in lowering the supply to channel barrier (which ought to be truly controlled by the gate).

Solely the physical phenomenon band edge is shown on the supply channel drain for 32nm and 250nm length devices[13]. It may be discovered that the source-channel barrier is down considerably for a 32nm device compared to a 250nm MOSFET [14]. Impact of DIBL is detected within the transfer characteristics as a decrease in threshold voltage. This additionally leads to the no saturation behavior of the semiconductor (ID keeps on increasing with VDS). Low American state once more ends up in a rise of OFF current [16]. However, there'll be a rise

in ON current of the semiconductor unit, however the rise in ON current isn't as high because the increase in OFF current, thence degrading the ON/OFF current quantitative relation of the device. There area unit many ways that to deal with DIBL like

(a) Increase the gate management by decreasing the compound thickness, that successively will increase the direct tunneling current through the gate compound [13]. And

(b) by increasing the substrate doping, that successively keeps the supply and drain apart (with less coupling [12]) by decreasing the depletion

5.0 IMPLEMENTING METHODS

The JLT device has no PN junction because source, channel, and drain regions[2] are doped uniformly with a phosphorous concentration of 1.5 × 1019 cm−3 . HfO2 as the gate dielectric and equivalent oxide thickness (EOT) of the gate dielectric is 1 nm. The source and drain extension region length [14] (Ls and Ld) of the structure is 20 nm with silicon body thickness of 10 nm. Al2O3 (k = 9.3), HfO2 (k = 22), and TiO2 (k = 80) are the dielectric materials [8] used as a spacer. For simulation, we have used Lombardi constant voltage and temperature model to capture the impact of the scattering mechanisms, doping, and transverse-field dependence [7] on carrier mobility. Schottky-Read-Hall is included to account for generation-recombination in the device.

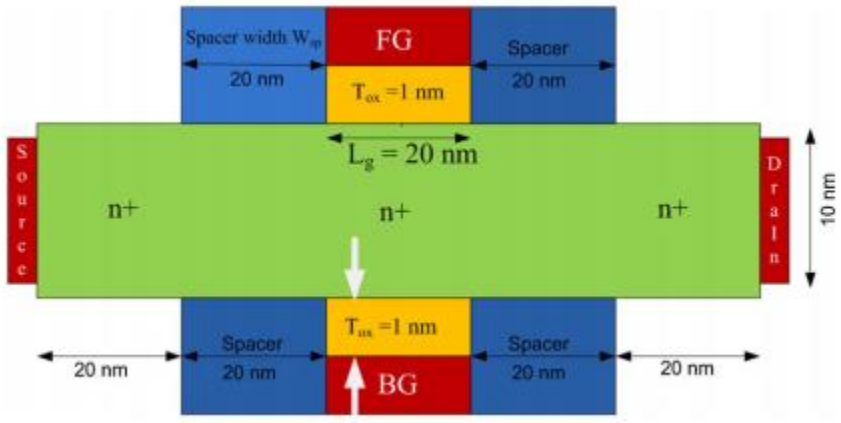

Figure Schematic view of double gate junction less transistor

Fermi-Dirac statistics model is activated to characterize carrier distribution, and band gap narrowing model is used to capture the effect of band gap narrowing in heavily doped regions of the device. Simulations are carried out using 2D device simulator [9] SILVACO ATLAS.22 For a fair comparison of RF performances of the DGJLT [7] for different spacers [11], the threshold voltage device is fixed for 0.25 V corresponding to drain current 10−7 A/um at a drain voltage of

50 mV (Vth extraction was done using constant current method). This Vth is obtained by adjusting the gate work function, which is 5.36, 5.38, and 5.42 eV for Al2O3, HfO2, and TiO2 spacers [3], respectively. Moreover, the JLT device threshold voltage is more sensitive to the gate work function.

6.0 METHODOLOGY

IMPACT OF THE HIGH *K* SPACER ON DC AND RF PERFORMANCE OF DGJLT

Fig. shows the schematic of the DGJL-TFET. The device is heavily n-type doped 20nm long Si-channel with Source/Drain extension[7] of 20nm. The gate oxide thickness (tox) is 2nm and device doping profile is maintained at 1x1019 cm-3 for silicon body thickness [8] of 5nm. The device is operated with two gates with different work functions: one gate called control-gate (CG) which is used to control the charge flow in the channel (ON and OFF of the device) by sweeping a control-gate voltage (VCG) [11] from 0V to VDD and another one is P-gate (PG), used to convert the N + source of DGJL-TFET[3] to P-type by using gate work function engineering for tunneling operation. The spacer width, which isolates the CG and PG of the device, is 5nm. All the simulations are performed using a 5.15.32.R version of Silvaco Atlas .

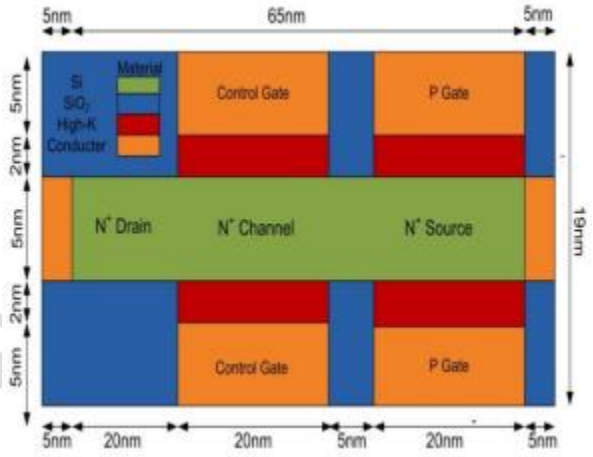

Figure Schematic Representation of DGJL-TFET Considered for Simulation

A non-local band to band (BTBT) tunnelling model is used to estimate the TFET device performance by considering the tunnelling along the lateral direction between source and drain. Due to heavy doping of the channel, the band gap narrowing (BGN) [16] model is considered and because of the high impurity atom present in the channel, the Shockley-Read-Hall (SRH) recombination model is enabled. Both quantum confinement effect, as well as interface trap effects in TFETs on the non-local band to band tunnelling [15], is considered by including

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quantum confinement (QC) model developed by Hansch and Schenk trap-assisted tunnelling (TAT) model. The work function of Control Gate is taken as 4.3eV for switching the layer under it as intrinsic and platinum metal [16] with a work function of 5.93eV is considered for P-Gate to make the layer under it as P-type region.

RF performance of DGJLT

The stability of factor (K) defines whether a system is conditionally or unconditionally stable for the RF range frequency. The stability factor described in Y parameters is explained,

$$K = \frac{2\,\mathrm{Re}(Y_{11})\,\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12}Y_{21})}{|Y_{12}Y_{21}|}$$

Where Y11 and Y22 are driving-point admittance at ports 1 and 2. Y12 and Y21 are known as transfer admittance. The symmetric DGJLT has 3 terminals, source, drain, and gate. Here, in this work, we have considered common gate (tied front and back gate) [12] as an input port and the drain terminal as an output port of DGJLT. The critical frequency (f k) is the frequency at which stability factor K = 1. Critical frequency (f k) is expressed in the small signal parameters.

$$f_k \cong \frac{f_T N}{\sqrt{g_{ds} g_m R_{gs} M^2 + NM(g_m R_{gd} + 1)}} \text{where}$$

$$M = \frac{C_{gs}}{C_{gg}}$$

$$N = \frac{C_{gd}}{C_{gg}}$$

f T is unity gain cut-off frequency, gds is output conductance, Rgs is the gate to source, Rgd is the gate to drain resistance, and Cgg is total gate capacitance [1]. The total gate to source capacitance (Cgs) and total gate to drain capacitance (Cgd) without considering overlap capacitance are reported.

$$C_{gs} = C_{gsi} + C_{fext} + C_{fint}$$

$$C_{gd} = C_{gdi} + C_{fext} + C_{fint}$$

$$C_{f_{int}} = \left[\frac{W\varepsilon_{si}}{3\Pi}\ln\left(1+\frac{t_{si}}{2t_{ox}}\sin\left(\frac{\Pi}{2}\frac{\varepsilon_{ox}}{\varepsilon_{si}}\right)\right)\right]\otimes e^{-\left(\left(V_{gs}-V_{FB}-2\varphi_f-V_{ds}\right)/(3/2)\varphi_f\right)^2}$$

$$C_{fext} = \left[\frac{2W\varepsilon_{ox}}{3\Pi}\ln\left(1+\frac{t_g}{2t_{ox}}\right)\right]$$

where Cfint is the inner fringing field capacitance due to high k gate dielectric, Cfext external fringing field capacitance due to high k spacer, and εsi and εox are a dielectric constant of silicon and oxide. W, tsi, and tox are the width, thickness of silicon body[1], and gate oxide thickness, respectively. VFB and Φ f are the flat band voltage and Fermi potential, respectively. From Figure, it is evident that the Stern stability factor (K) [4] becomes unity at a lower frequency with the increase of the dielectric spacer constant. Junctionless transistors do not have junctions, and the capacitances associated with the device are mainly due to the parasitic capacitance consisting of Cfint and Cfext which are made known in Equations.

7.0 RESULTS

A. Impact of Gate Dielectric Material (k) on Critical Frequency (fk)

Due to higher impact of gm over the Cgg, fT which is calculated from simulation values gm and Cgg using equation is increasing with increase in gate dielectric value.

As discussed earlier, from Fig, due to improved performance of fT, Cgg and gm with a high-k gate dielectric, DGJL-TFET with high-k gate material (HfO2, TiO2) yielded higher fk as compared to low-k gate material (SiO2). From Fig. fk which is calculated using equation 8 is 1.5GHz for low-k gate oxide material (SiO2) and for 130GHz for high-k gate oxide material (TiO2). Various parameters which has effect on the stability and fk for various oxide materials are presented in Table.

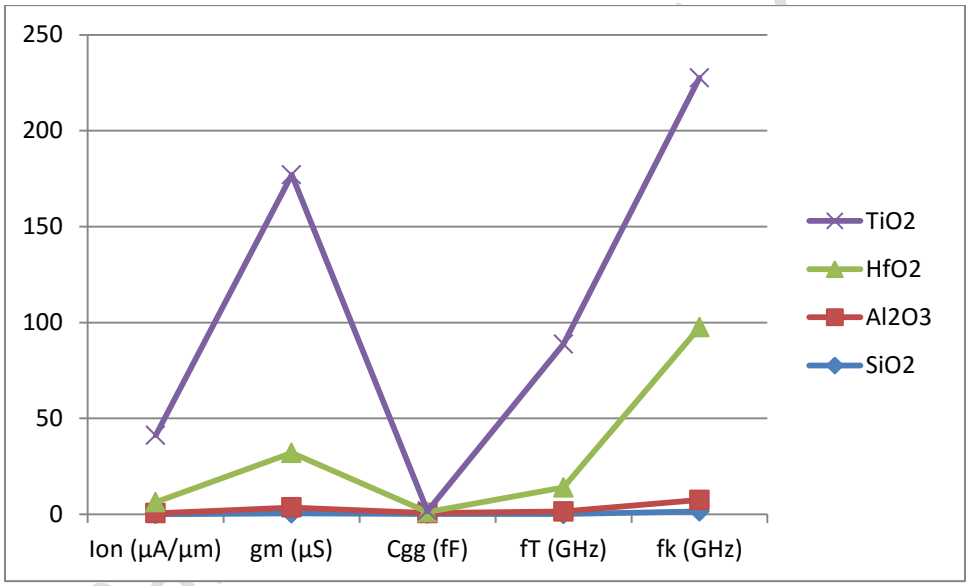
Table key performance metrics of dgjl-tfet for different gate oxides at vcgs= vds=1v

Gate oxide material	Ion (μA/μm)	gm (μS)	Cgg (fF)	fT (GHz)	fk (GHz)
SiO2	0.1	0.5	0.269	0.2	1.5
Al2O3	0.5	3.09	0.375	1.31	6

HfO2	5.71	28.4	0.495	12.5	90
TiO2	34.9	145	0.633	74.7	130

B. Impact of Isolation Spacer Length (Lsp) on fk

In the previous subsection, it is observed that the ON current of the DGJL-TFET is improved with the aid of high-k gate dielectrics. The other way to increase ION is by scaling the isolation spacer length (Lsp), with the aid of charge plasma concept [24]. With scaling of spacer length (Lsp), the gate controllability over the source-channel region is increased, which reduces the tunneling barrier height, due to which the tunneling probability increases, subsequently increasing the ION. However, this improved ION is obtained at the expense of increased Cgg, which is shown in Fig.



Graph key performance metrics of dgjltfet for different gate oxides at vcgs= vds=1v

This impact is largely attributed by interface defects at high-k oxide and Si interface, the induced trapped charges and capacitive fringing field's associated with high-k spacers. For TiO2 spacer, fk is varied from 3GHz to180GHz when Lsp scaled from 10nm to 3nm.

However, a large variation of fk nearly twice as that of the high-k spacer (TiO2) is noticed with the low-k spacer (SiO2). i.e., fk is varied from 6 GHz to 350 GHz, when Lsp scaled from 10nm to 3nm. C. Impact of Gate Oxide Thickness (tox) on fk Tunneling process in T-FET devices is greatly affected by the variation gate oxide thickness (tox), this effect is noticed due to the variation of gate-capacitive coupling with variation of tox. As per WKB approximation, oxide

thickness affects the tunneling probability by modulating the tunneling width. Equation 16 gives the dependency of tunneling width in terms of gate oxide thickness and other parameters. A thinner gate oxide will have less tunneling width (λ) and vice versa for thicker gate oxides.

$$\lambda = \sqrt{\left(\frac{t_{ox} t_{si} \varepsilon_{si}}{\varepsilon_{ox}}\right)}$$

The ON current of device with tox=5nm is smaller when compared to 2nm tox device, since 5nm oxide thickness devices have low capacitive coupling, due to which it has a lesser influence on the tunneling phenomena. Through simulation, it is also observed that irrespective of gate oxide material, DGJL-TFET exhibits improved ION with the scaling of the tox. It is also observed that TiO2 gate dielectric with tox =5nm has better ION (6.6 µA) than low-k gate dielectric (Al2O3) with tox= 2nm (0.35 µA) The simulated values effecting the stability and fk with tox scaling for TiO2 gate oxide material are given in Table. Fig. shows fk variation with the scaling of tox for different gate oxide materials of a DGJL-TFET with 5nm SiO2 isolation spacer. It is observed that, with the scaling of tox, DGJL-TFET with lowk gate dielectric has lower fk then that of high-k gate dielectric.

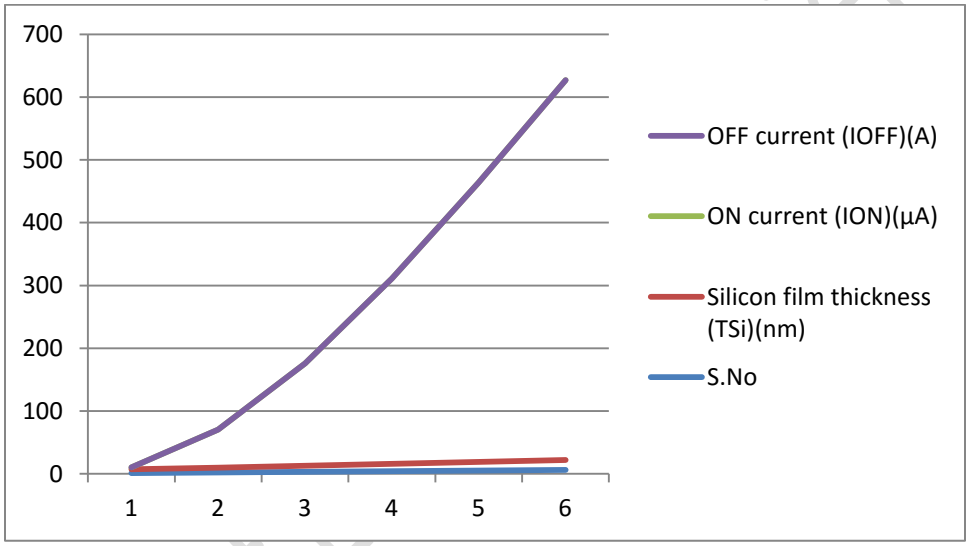
Before doing the radiation study, the impact of silicon film thickness (TSi) and channel doping (Nch) on the DC performance parameters (i.e. ON Current (ION) and OFF Current (IOFF)) of BPJLT device are studied and is given in Table.

Table ION and IOFF of BPJLT devices with various TSi

S.No	Silicon film thickness (TSi)(nm)	ON current (ION)(µA)	OFF current (IOFF)(A)
1	6	3.22	2.45E-16
2	8	60.5	1.00E-13
3	10	163	1.10E-10
4	12	295	1.02E-07
5	14	445	1.80E-05
6	16	605	1.21E-04

The practical values of the film thicknesses are highlighted in Table II. Beyond this range, either the ION is too low or the IOFF is too high. Similarly the increase in the channel doping increases both ION and IOFF. Once again the practical values of doping values are highlighted in Table III. Beyond this range, either the ION is too low or the IOFF is too high.

Either the increase in the film thickness for the given channel doping or the increase in the channel doping for the given film thickness increases IOFF due to the reduced electrostatic control resulting from poor depletion of the channel in the OFF state. Since the IOFF is affected drastically when the film thickness or channel doping is changed, for the fair comparison IOFF is maintained constant (i.e. IOFF is constrained to 100 nA/μm which is the IOFF of reference device). For the subsequent study carried out IOFF is maintained constant. This constraint is met by changing the two other parameters as one parameter is not sufficient to achieve this constraint. Following cases are explored to study the impact of TSi and Nch on BPJLT DC performance.



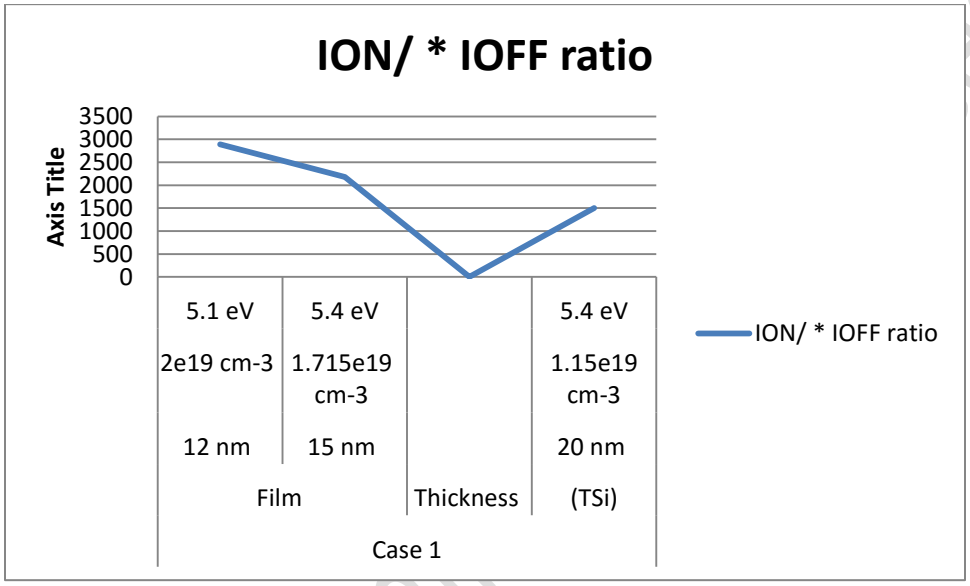
Graph ION and IOFF of BPJLT devices with various TSi

- Case 1: Vary Tsi and adjust WF and Nch to constraint IOFF
- Case 2: Vary Nch and adjust WF and Tsi to constraint IOFF

Table ION/IOFF ratio of various BPJLT devices

Name	Varying Parameter	Silicon film thickness (TSi)	Channel doping concentration (Nch)	Gate work function (WF)	ION/ * IOFF ratio
Case 1	Film	12 nm	2e19 cm-3	5.1 eV	2894
	Thickness	15 nm	1.715e19 cm-3	5.4 eV	2180
	(TSi)	20 nm	1.15e19 cm-3	5.4 eV	1501

Reduced TSi improves the electrostatic control of the channel in the OFF state whereas increased Nch enhances the conductivity in the ON state. So the devices with increased Nch and reduced TSi (i.e. Case 2 devices) yields better ION/IOFF ratio in the BPJLT devices. The access pulse (V(nacc)) of 10 ps of rise and fall times, and a pulse width of 250 ps is used to verify the SRAM functionality.



Graph ION/IOFF ratio of various BPJLT devices

After SRAM functionality verification, the soft error simulation is done by using heavy ion models in SDEVICE simulator. The heavy ion radiation model isFor further study (radiation study) on BPJLT devices we have taken only the devices with better ION/IOFF ratio (i.e. Case 2 devices in Table).

SEU study on BPJLT based 6T-SRAMs

The SEU study is carried out using TCAD simulations. The 6T-SRAM cell used in this SEU study is shown in Fig. The BPJLT devices with better ION/IOFF ratio are used for creating SRAMs.

8.0 CONCLUSION

With the increase in dielectric constant of the spacer from 9.3 to 80, the stern's stability factor, transconductance, and gate capacitance are increased, and unity gain cut-off frequency and f max are decreased. Critical frequency (fk) is examined to figure out the unconditional stability behavior of DGJLT. Furthermore, we also studied the effects of the geometrical scaling

parameters and biasing conditions on the critical frequency, and it is observed that lower gate work function, large gate oxide thickness, high k spacer, and lower bias conditions will yield the better stability, and thus, the device becomes unconditional stable at a lower frequency. Hence, the complicated nature involved in RF designing is reduced. Finally, device optimization is performed, which exhibits better stability performance with the critical frequency of38.8 GHz and above, where the device is unconditionally stable without any additional stabilization circuits.

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