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IMPLEMENTATION OF 2'S COMPLEMENT OF 4-BIT BINARY NUMBERS USING MAJORITY LOGIC

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ABSTRACT- All-QCA majority N-bit binary to 2's complement converter has been designed with the help of majority symmetric gates. 2's complement is common in computer systems and is used in binary subtraction and for logical manipulation. This design strategy aims towards the formation of digital circuits with ideally zero power dissipation. In this paper we have proposed a new majority logic module to design a 4-bit binary 2's complement circuit. This complement circuit using majority logic can be used to design other low loss Arithmetic circuit. Proposed circuits have been simulated using ISE and implemented using Xilinx platform.

1. INTRODUCTION

Conventionally digital circuits were designed using basic logic gates. These conventional basic logic gates dissipate some energy loss due to the information loss during the operation [1]. Irreversibility of energy is caused because the total number of output signals in the conventional gate is less than the number of total input signals. Reduced number of output signals is the major cause of the lowering of entropy of the overall digital system. The amount of energy loss for one bit of information loss in an irreversible gate was given by R. Landauer in 1961. Later in 1973 C. H. Bennette has shown that this energy loss can be minimized or even removed if the circuit is made up from the reversible logic gates [2]. QCA circuit designing is gaining wide scope in the area of Quantum computing, Low power CMOS design, Nanotechnology, Optical computing, Signal processing, advanced computing etc due to its ability to design low loss or approximately lossless digital circuits. Reversible logic concept is based on the formulation of the input states of the digital logic system by knowing its output states at any moment, whereas we can generate the output states from input in a conventional digital system.

Presently Quantum-dot Cellular Automata (QCA) become an attractive research area due to high computing speed, low power and high device density in nano-electronics digital circuits (Bibhash Sen et al, 2015; C.S, Lent et al., 1993, Ali Newas bahar et al, 2015).In QCA cell formation of four quantum dots placed at the corner of a square and comprise two free electrons (Shaahi nangiziet al, 2014, S. Hashemi et al., 2013). In QCA logic state is laid down by the polarization of electrons. The two stable polarization of electrons are binary logic 0 (P= -1) and binary logic 1 (P=1) as depicted in Fig. 1e. The timing in QCA is versed by the synchronized of four clock zones and each clock zone has 900 phase shift as depicted in Fig 1f. The fundamental QCA layout design are the three input majority voter gate (MV) and an inverter, depicted in Fig 1b, 1c. The majority voter gate described as MV (A, B, C) = AB+BC+CA. We look into that majority vote (MV) is the optimum preference in designing of logic design such as AND, OR as depicted in Fig. 1d, 1h.

2. QCA FUNDAMENTALS

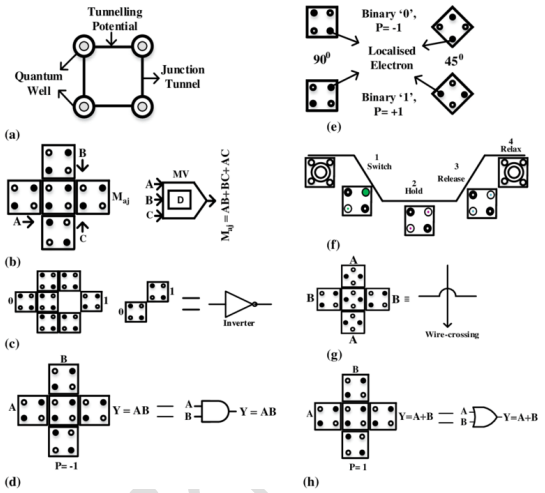

Fig. 1: QCA fundamentals (a) Quantum cell (b) QCA, Majority voter (c) QCA, Inverter (d) QCA, AND gate (e) Four-dot QCA cell with two different polarization (f) QCA, clock (g) QCA, Wire (h) QCA, OR gate

In QCA cell has a quantum dot, with a four number. The shape of quantum-dot is circular with a specified diameter of 1 nm, and each dot is situated within a neighbor radius of 2 nm. Whether two extra electrons are situated in existing two quantum dots and the arrangement is always in a diagonal way. The formed QCA cell can be a definite polarization (Fig. 1a). The majority gate, inverter, fan-out concept, and clock are depicted in Fig. 1 b– d, respectively. The binary value stored in the QCA cell can be defined by polarization.

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3. 4-BIT BINARY 2'S COMPLEMENT CIRCUIT

There are two ways to represent a negative binary number in the digital systems [14]. These are as follows-

[a] Signed Binary Negative Number

[b] Unsigned Binary Negative Number

In signed binary negative number, the most significant bit (MSB) is used to represent the sign of the number. For negative binary number MSB is set to 1otherwise 0 for positive binary number. In the concept of unsigned binary negative number there are two techniques for the representation-

[a] 1"s Complement Method

[b] 2"s Complement Method

In 1"s complement method each and every bit of the binary number is interchanged by its complement bit i.e. 0 by 1 and 1 by 0. In the 2"s complement method, binary 1 is added to the 1"s complement of the respective binary number. 2"s complement method is considered better for arithmetic operations as compared to 1"s complement method due to the following reasons-

[1] For subtraction with complements, 2"s complement requires only one addition operation, whereas 1"s complement requires two addition operations if there is an end carry.

[2] 1"s complement has two arithmetic zeros, all 0s and all 1s.

So due to above reasons 2"s complement is preferred in the calculations generally. Table 1 is a listing of the 4-bit binary number from 0 to 15 and its corresponding 2's complement value. To design binary to two's complement converter circuit Karnaugh map has been drawn as shown in the Fig. 3 from Table 1. Here, each bit of the 4-bit binary code is labeled as A to D starting from MSB (most significant bit) to LSB (least significant bit) and the corresponding 2's complement is labeled as E to H starting from MSB to LSB.

TABLE I. TRUTH TABLE FOR BINARY TO 2'S COMPLEMENT

Decimal	Binary code				2's Complement			
	A	B	C	D	E	F	G	H
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1
2	0	0	1	0	1	1	1	0
3	0	0	1	1	1	1	0	1
4	0	1	0	0	1	1	0	0
5	0	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	0
7	0	1	1	1	1	0	0	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	0	1	1	1
10	1	0	1	0	1	1	1	0
11	1	0	1	1	0	1	0	1
12	1	1	0	0	0	1	0	0
13	1	1	0	1	0	0	1	1
14	1	1	1	0	0	0	1	0
15	1	1	1	1	0	0	0	1

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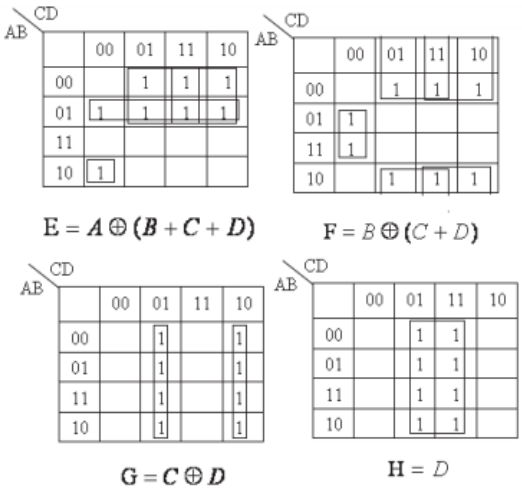

Figure 2. Karnaugh map for binary to 2's complement

From the above Karnaugh map (Fig. 2), the Boolean equations are obtained as product of sums form for the each output as in equation

E=A⊕B ⊕ C ⊕ D

F=B ⊕ C ⊕ D

G=C ⊕ D

H=D

4. QCA IMPLEMENTATION

The layout design of 2's complement of a 4-bit number is shown in the figure 3 below where A, B, C & D are inputs and outputs are taken from E, F, G and H.

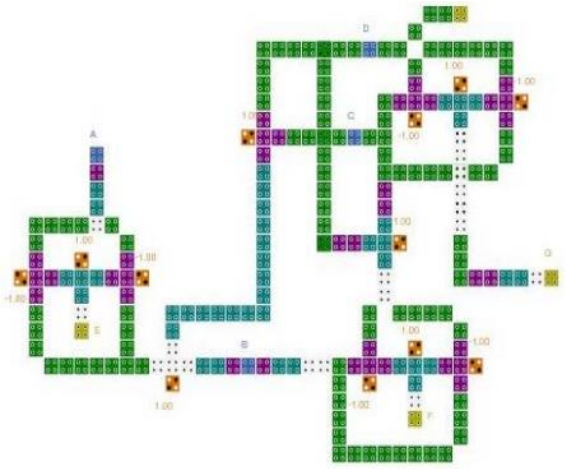

Fig.3QCA Layout of 2's Complement of 4-bit number

As mentioned in above equations, XOR function plays a pivotal role in implementing complement circuits. An N-input XOR function is usually implemented by combining several 2-input XOR gates. Moreover, use of existing designs of QCA 2-input XOR gates, which use a large number of majority gates, lead to significant compromise with the area as well as latency.

For instance, implementation of a 4-bit XOR function using three 2-input XOR gates takes at least 9 majority gates. However, we have observed that more efficient implementation of n-input XOR function is possible by using combinations of 2-input and 3-input XOR gates following ESOP based transformation [16]. Accordingly, we have used combination of

2-input and 3-input XOR gates to implement n-bit XOR function instead of relying solely on 2-input XOR gates which was the case in existing implementations. We have also used majority logic reduction to further optimize the designs of individual XOR gates (both 2-input and 3-input). The logical expression representing 2- input XOR function can be re-written equivalently as M[M(A, B, 1), M(A, B, 0), 0] using majority logic reduction, where M(X, Y, Z) represents a 3-input majority gate [6] with inputs X, Y, and Z. The above Boolean expression can be implemented using three 3-input majority gates and one inverter as shown in Fig.4(a).

Similarly, the logical expression ($A\bar{B}C\bar{}$ +$AB\bar{}$ $C\bar{}$ +$AB\bar{C}\bar{}$ +ABC), representing a 3-input XOR function can be re-written as M[M(A, $\bar{}$ B, $\bar{}$ $C\bar{}$), C,M(A, B, $C\bar{}$)] using majority logic reduction, where M(X, Y, Z) represents a 3-input majority gate with inputs X, Y, and Z. Fig. 4(b) shows the schematic diagram of the gate level implementation of the above expression.

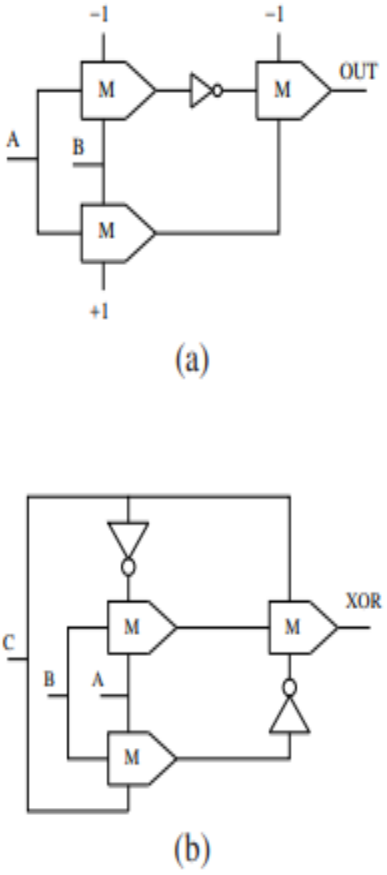

Fig. 4: Gate level implementation of (a) 2-input XOR and (b) 3-input XOR

The logical expression for the output of F is B⊕C⊕D and hence, it can be implemented simply by using the 3-input XOR gate of Fig.4 (b). The logical expression for the output of G is B ⊕ C ⊕ D and hence, it can be implemented simply by using the 2-input XOR gate of Fig.4(a).similarly 4 input XOR gate is implemented by using the combinations of 2-input XOR and 3-input XOR gates for the logic expression E.

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4. SIMULATION RESULTS

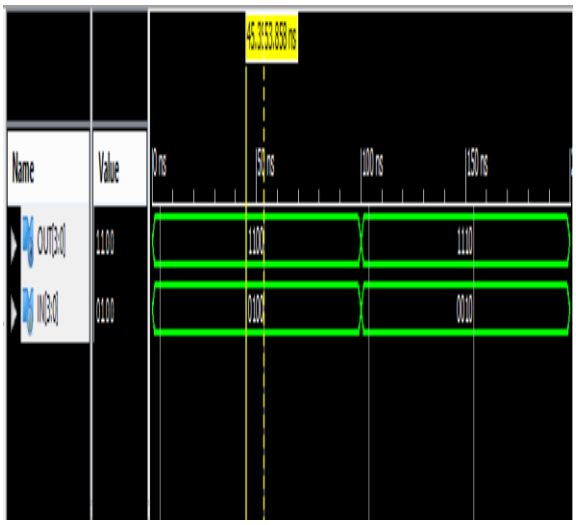

Fig 5. SIMULATION OUTPUT

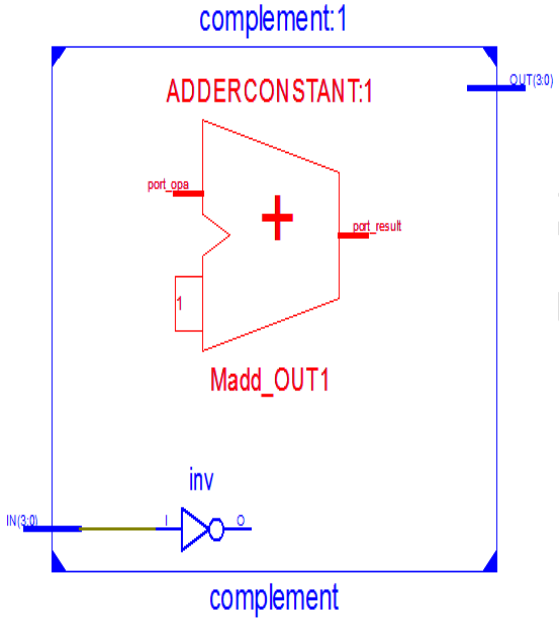

Fig 6. RTL OUTPUT

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	2	5472	0%
Number of 4 input LUTs	3	10944	0%
Number of bonded IOBs	8	240	3%

Fig 7. AREA DESIGNSUMMARY

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	2	0.754	0.567	IN_2_IBUF (IN_2_IBUF)
LUT4:I0->O	1	0.147	0.266	Madd_OUT_xor<3>11 (OUT_3_OBUF)
OBUF:I->O		3.255		OUT_3_OBUF (OUT<3>)
Total		4.989ns (4.156ns logic, 0.833ns route) (83.3% logic, 16.7% route)		

Fig 8. TIME SUMMARY

5.CONCLUSION

Majority logic is becoming the modern way of digital logic circuit designing. Here in this paper we have attained a highly optimized four-bit 2"s complement calculator circuit by using various combinations of the basic Majority gates and a new reversible gate proposed in the paper. The base of optimization is total Majority gates used and garbage outputs generated. Optimized 2"s complement calculator circuit (shown in figure 3 and 4) has been designed using a Majority gates and have zero unused outputs generated. This design can be employed in low power logical design applications.

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