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PERFORMANCE COMPARISON AMONG VARIOUS PARALLEL PREFIX ADDER TOPOLOGIES

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Abstract- VLSI Integer adders find applications in Arithmetic and Logic Units (ALUs), microprocessors and memory addressing units. Speed of the adder often decides the minimum clock cycle time in a microprocessor. The need for a Parallel Prefix Adder (PPA) is that it is primarily fast when compared with a ripple carry adder. PPA is a family of adders derived from the commonly known carry look ahead adders. These adders are suited for additions with wider word lengths. PPA circuits use a tree network to reduce the latency to O(log2 n) where 'n' represents the number of bits. The proposed architectures have the least number of computation nodes when compared with existing one's. This reduction in hardware of the proposed architectures helps to reap a benefit in the form of reduced power and power-delay product.

Keywords- Parallel prefix adders, carry look ahead adders, power-delay product

I. INTRODUCTION

Binary addition is most important operation in computer arithmetic. Very large scale integrated (VLSI) integer adders are critical elements in general purpose micro processer and digital signal processer since they are employed in ALUs, in floating point arithmetic data paths and in address generation units [2].

A large variety of algorithms and implementations have been proposed for binary addition [2]. High speed operation adders in tree structure Parallel prefix adders like Sklansky adder, Kogge-Stone adder, Brent-Kung adder and Ladner- Fischer adder and Han-Carlson adder

II. PARALLEL PREFIX ADDERS

Parallel prefix adder (PPA) perform parallel addition Which reduce the delay of the adder and there is an improvement in speed. PPA carries out three necessary and very important steps that are as follows.

1) Computation of carry generation and carry propagation signals by number of input bits (**pre-processing**).

2) Calculating all the carry signals in parallel that is called prefix computation (**Carry graph**).

3) Evaluating total sum of given inputs**(Post processing)** [3]. As shown in below.

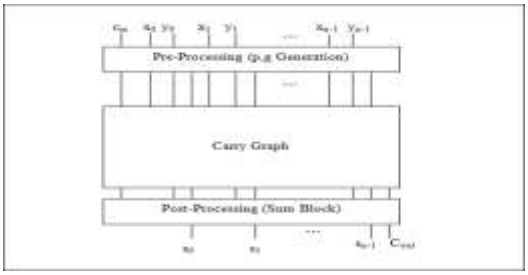


Figure 1: The Mechanism of Parallel Prefix Adders

The three step process is carried by the fallowing Parallel prefix addition as follows:
1) Pre-processing: computation of carry generation (Gi) and carry propagation (Pi). Previous carry is calculated to the next bit is called Propagate signal and generate is used to generate the carry bit they are

$G_i = A_i \cdot B_i$

$P_i = A_i$ xor B_i

2) Calculation of carry signals:

$G_{i:j}=G_{i:k}+P_{i:k}\cdot G_{k-1:j}$

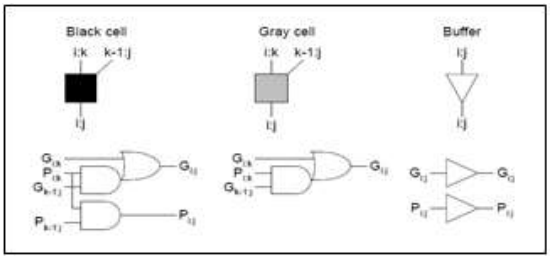
$P_{i:j} = P_{i:k} \cdot P_{k-1:j}$

3) Calculation of final sum and carry:

$C_i=G_i$

$S_i = P_i \text{ xor } G_{i-1}$

Figure 2: schematics for Black cell, Grey cell and Buffer.



Five types of Parallel prefix adder are taken for the analysis in this paper.

III. SKLANSKY ADDER

Figure 3 shows a 16-bit Sklansky adder (Sklansky, 1960). It has minimum depth prefix graph. The longest lateral fanning wires go from anode to $\frac{n}{2}$other nodes. The structure possesses an optimal depth given by $\log_2 n$and the number of computational nodes is given by $[\frac{n}{2}(\log_2 n)]$.The fan-out of the Sklansky's adder increases drastically from the inputs to outputs along the critical path, which accounts for large amount of latency. This degrades the performance of the structure when the number of bits of the adder becomes large.

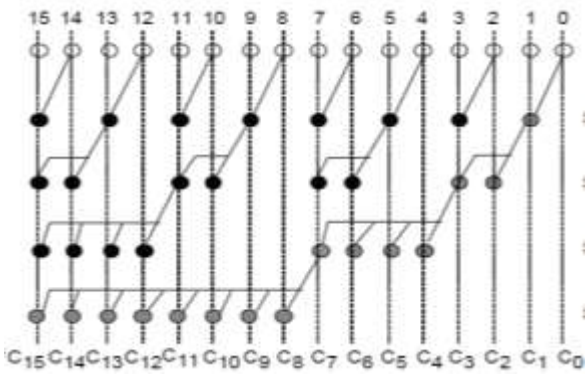


Figure 3: Prefix Graph of 16-bit Sklansky Adder

IV. KOGGE-STONE ADDER

Figure 4 shows the prefix graph for a 16-bit Kogge-Stone adder(Kogge and Stone, 1973). Adders implemented using this technique possess regular layout and a controlled fan-out of two. Kogge-Stone structure is very attractive for high-speed applications. However, it comes at the cost of area and power. The delay of the structure is given by $\log_2 n$.This structure possesses $[(n)(\log_2 n) - n + 1]$computation nodes. The Kogge-Stone scheme addresses the problem of fan out by introducing a recursive doubling algorithm. It uses idempotency property to limit the lateral fan-out, but at the cost of a dramatic increase in the number of lateral wires at each stage. This is because there, is a massive overlap between the prefix sub-terms being pre-computed.

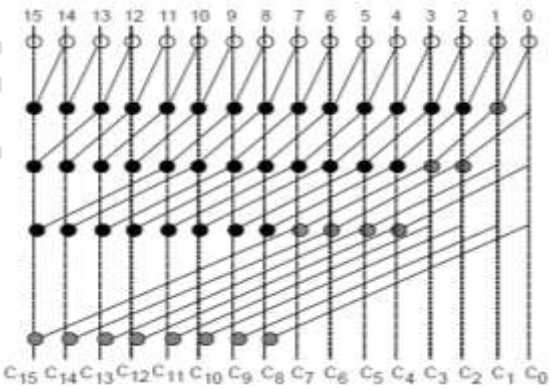


Figure 4: Prefix Graph of 16-bit Kogge Stone Adder

V. BRENT-KUNG ADDER

Figure 5 shows the prefix graph of a 16-bit Brent-Kung adder(Brent and Kung, 1980). A simpler tree structure could be formed, if only the carry at every power of two positions is computed as proposed by Brent and Kung. An inverse carry tree is added to compute intermediate carries. Its wire complexity is much less than that of a Kogge-Stone adder.The delay of the structure is given by $[(2)(\log_2 n) - 2]$ and the number of computation nodes is given by computation nodes is given $[2(n) - 2 - (\log_2 n)]$.

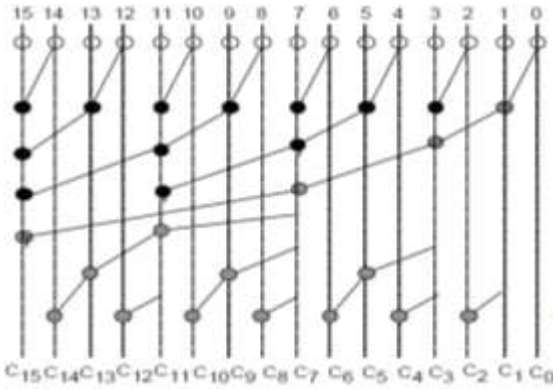


Figure 5: Prefix Graph of 16-bit Brent-Kung Adder

VI. HAN-CARLSON ADDER

Figure 6 shows the prefix graph for a 16-bit Han-Carlson adder(Han and Carlson, 1987). It is a hybrid design combining stages from Brent-Kung and Kogge-Stone. It has five stages, the first stage resembles Brent-Kung adder and the middle three stages resemble Kogge-Stone adder. It possess wires with shorter span than Kogge-Stone. The dot operator was placed in the odd bit positions in the initial stages, but the dot operator was placed in the even bit positions in the final stage. The delay in this structure is given by $[(\log_2 n) + 1]$, while the computation hardware complexity is $[\frac{n}{2}(\log_2 n)]$.The hardware complexity is reduced compared to Kogge-Stone adder, but atthe cost of introducing an additional stage to its carry merge path. This structure again trades off an increase in logical depth for a reduction in fan out.

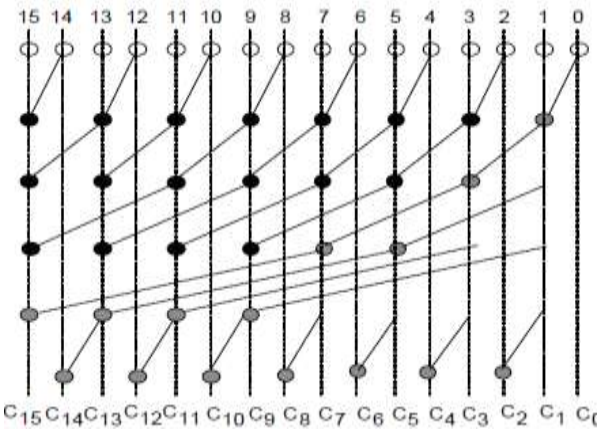


Figure 6: Prefix Graph of 16-bit Han-Carlson Adder

VII. LADNER-FISCHER ADDER

The Figure 7 shows the prefix graph structure for a 16-bit Ladner-Fischer adder (Ladner and Fischer, 1980).This structure is a modified version of Sklansky's adder. In a 16-bitLadner-Fischer adder, the longest lateral fanning wires go from a node to$\frac{n}{4}$other nodes. The delay of the structure is given by $[\log_2 n + 1]$. The number of computational nodes is given by $[\frac{n}{2}(\log_2 n)]$.Table1 summarizes the structural details of the existing PPAs.

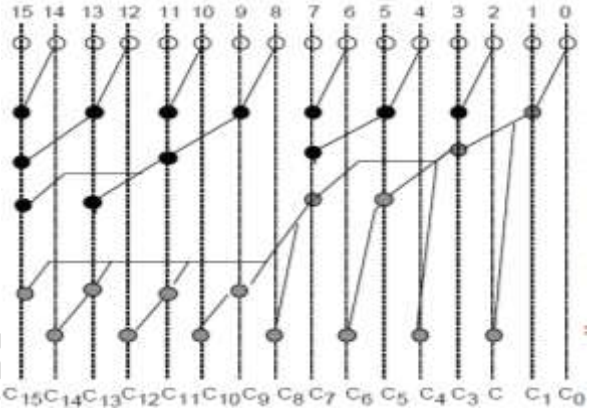


Figure 7: Prefix graph of 16-bit Ladner-Fischer Adder.

Table 1: Structural Comparison of n-bit Parallel Prefix Adders

Adder Type	Number of Computation Nodes	Logic Depth
Brent-Kung	$[2(n)-2-\log_2 n]$	$[(2(\log_2 n)-2]$
Kogge-Stone	$[(n)(\log_2 n)-n+1]$	$\log_2 n$
Han-Carlson	$[\frac{n}{2}(\log_2 n)]$	$[(\log_2 n)+1]$
Ladner-Fischer	$[\frac{n}{2}(\log_2 n)]$	$[(\log_2 n)+1]$
Sklansky	$[\frac{n}{2}(\log_2 n)]$	$\log_2 n$

VIII. SIMULATION RESULTS

Various parallel prefix adder's performance is tested in the Xilinx ISE Design Suite of version 14.7. The simulation results for the Sklansky adder, Brent Kung Adder, Kogge-stone adder, Ladner fischer adder and

Han-Carlson adder are shown in the following figures.

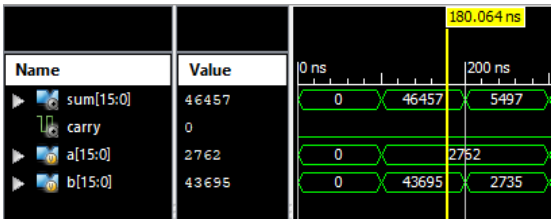


Figure 8: Simulation result for the 16-bit Sklansky Adder

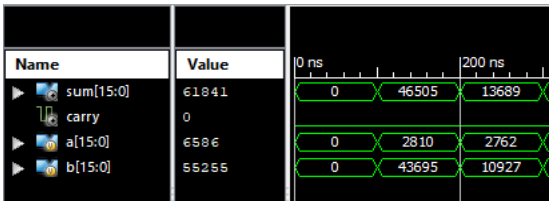


Figure 9: Simulation result for the 16-bit Brent-Kung Adder

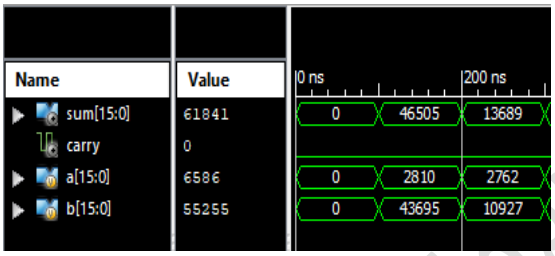


Figure 10: Simulation result for the 16-bit Kogge-Stone Adder

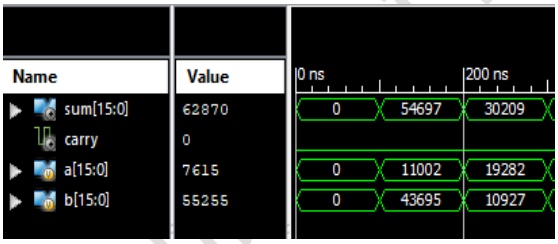


Figure 11:Simulation result for the 16-bit Ladner-Fischer Adder

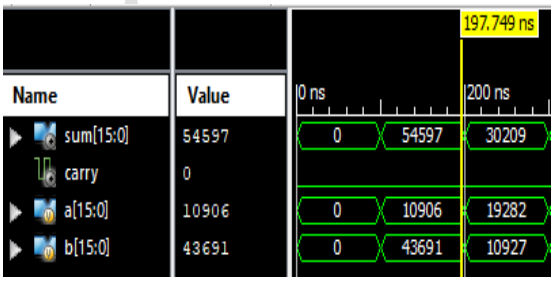


Figure 12: Simulation result for the 16-bit Han-Carlson Adder

Table 2: Comparison among the 16-bit PPA's

Adder	Area (in-terms of LUT's)	Delay (in nSec)
Skylansky	**25**	**11.423**
Kogge-Stone	**40**	**11.990**
Brent-Kung	**24**	**12.094**
Ladner-Fischer	**26**	**11.379**
Han-Carlson	**24**	**12.045**

IX. CONCLUSION

This paper gives the detailed description of five Paralle Prefix Adder's like Sklansky Adder, Brent-Kung Adder, Kogge-Stone Adder, Han-Carlson Adder and Ladner-Ficher Adder. The Parallel prefix adders are faster because of less delay and area efficient compared to other basic adders. The work compares the area and delay of the parallel prefix adders. Five adders are simulated using Xilinx ISE Design Suite of version 14.7. Further these structures can be utilized for the development of Hybrid Prefix structure for better improvement

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