Journal of Engineering Sciences

Vol 10, Issue 11, Nov /2019
ISSN NO: 0377-9254

LOW POWER FAULT TOLERANT REVERSIBLE LOGICAL CIRCUITS

[1]VALLURI VEERENDRA SUBHASH, [2]DASARI GOWTHAMI
[1]Assistant Professor, Dept. of ECE, Kakinada Institute of Engineering & Technology WOMEN"S, Korangi, A.P
[2]M. Tech student, Dept. of ECE, Kakinada Institute of Engineering & Technology WOMEN"S, Korangi, A.P

Abstract- This paper presents the design of Reversible Fault tolerant logic gates which gives the zero amount of energy consumption. It is very important in the area of VLSI circuits. Because of very low heat dissipation, reversible technology plays an important role in nanotechnology, less energy Complementary metal-oxide Semiconductor (CMOS) designs .It has been realized that quantum computing is one of the latest technologies using reversible logic gates. So, we can use reversible logic technology for decreasing the energy dispersion, heat wave dissipation, increasing rapidness etc. So, it is used to maximize the speed and reducing energy consumption. In this, we can describe following reversible logic gates like fredkin, peres, Feynmen and toffoli gate etc. and proposing two new gates called MSB and MSH reversible gates. At last we can analyse the design of 1-bit full adder, 4:1 Multiplexer and D-Latch using these reversible gates..

Keywords- **Heat dissipation, reversible technology, nano technology, MSB and MSH gates**

I.INTRODUCTION

Researchers like Landauer have shown that for irreversible logic computations, each bit of information lost, generates kTlog2 joules of heat energy, where k is Boltzmann's constant and T the absolute temperature at which computation is performed [1]. Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [2], since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information. Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa. In the reversible circuits, there is a one-to-one mapping between input and output vectors. Bennett's theorem [2] about heat dissipation is only a necessary and not sufficient condition, but its extreme importance lies in the fact that every future technology will have to use reversible gates to reduce power. As the Moore's law continues to hold, the processing power doubles every 18 months. The current irreversible technologies will dissipate a lot of heat and can reduce the life of the circuit.

The reversible logic operations do not erase (lose) information and dissipate very less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low-power CMOS design, optical computing, nanotechnology and quantum computing. The most prominent application of reversible logic lies in quantum computers.

A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; each gate performing an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information; corresponding to the classical bit values 0 and 1. Any unitary operation is reversible hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).Thus, Quantum Arithmetic must be built from reversible logical components [10].

Figure 1: Different Reversible logic gates

TYPES OF LOGIC GATES

One of the main constraints in reversible logic is to minimize the number of reversible gates used and garbage output produced. Garbage output refers to the output that is not used for further computations. In other words, it is not used as a primary output or as an input to another gate. In literature, there are a number of existing reversible gates such as Fredkin gate[3,4,5],Toffoli Gate[3,4] and New Gate [6].Thus, the paper provides the initial threshold to build more complex systems which can which can execute more complicated operations. The reversible circuits designed and proposed here form the basis of the ALU of a primitive quantum CPU.

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Vol 10, Issue 11, Nov /2019
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Reversible Logic Gates and its input-output relations				
Name of the Gate	**Order**	**Inputs**	**Outputs**	**Relation**
Fredkin Gate	3 X 3	[A,B,C]	[P,Q,R]	P = A Q = AB ⊕ AC R = A'C ⊕ AB
Feynman Gate	2 X 2	[A,B]	[P,Q]	P = A Q = A ⊕ B
Double Feynman Gate	3 X 3	[A,B,C]	[P,Q,R]	P = A Q = A ⊕ B R = A ⊕ C
Peres Gate	3 X 3	[A,B,C]	[P,Q,R]	P = A Q = A ⊕ B R = PQ ⊕ R
TR Gate	3 X 3	[A,B,C]	[P,Q,R]	P = A Q = A ⊕ B R = AB' ⊕ C

DESIGN OF ADDER AND SUBTRACTOR BY USING REVERSIBLE LOGIC GATES:

Reversible circuits are designed by using the reversible logic gates only. There are many circuits of 1-bit full adder and subtractor design [12]. Here two circuits are design of full adder and subtractor Using 4 and 8 reversible logic gates and in this we can desing our circuit in the terms of reversible logic gates but using pass transistor and CMOS

A. 1-bit full adder and subtractor: In fig.2, 1-bit reversible full-adder and subtractor[13] using the 3 Feynman gates, 2 TR gates, 1 Fredkin gate and 2 Peres gates to design the circuit. And the control input is given to the switch in between adder and subtractor. If provided control input is 1 then addition is achieve and if that is 0 then subtraction is achieve.[14]

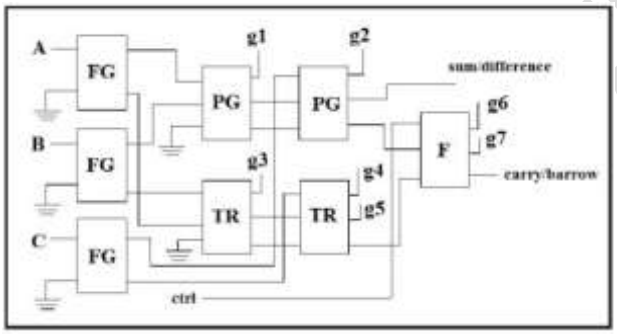

*Figure 2***:** *Design 1of one bit full adder/subtractor*

Now, fig 3, in this we can use 2 Peres gates and 2 Feynman gates[14] and provide the control input to the switch between full adder and subtractor, so then, now if the control is 0 then adder is created or if i.e 1 then the subtractor is created

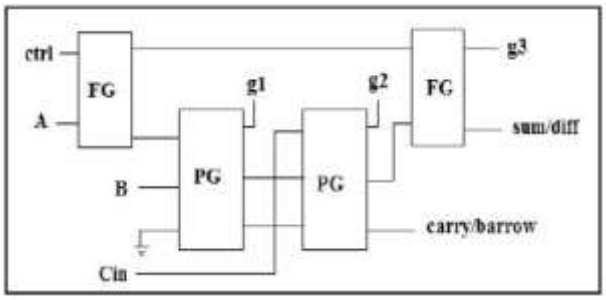

Figure 3: **:** *Design 2 of one bit full adder/subtractor*

PROPOSED REVERSIBLE LOGIC GATES

1) MSH (Mubin-Sworna Hasan) Gate:

It is a 4×4 reversible fault tolerant gate having four inputs and four outputs. The below figure represents the proposed MSH gate having input vector is [A,B,C,D] and output vector is [P,Q,R,S]

2) MSB (Mubin-SwornaBabu) Gate:

It is a 6×6 reversible fault tolerant gate having six inputs and six outputs. The below figure represents the proposed MSB gate having input vector is [A,B,C,D,E,F] and output vector is [P,Q,R,S,T,U].

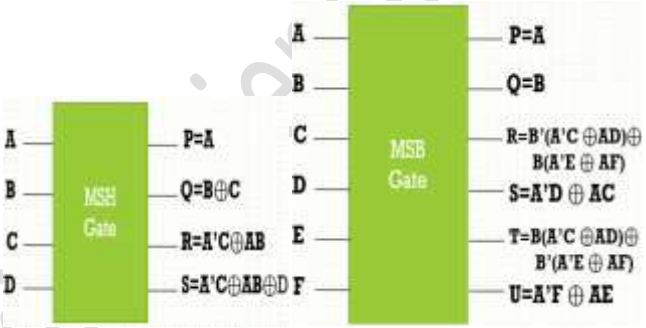

Figure 4: Proposed MSH and MSB gates

PROPOSED REVERSIBLE FAULT TOLERANT D-LATCH AND 4×1 MULTIPLEXER

Fig. 5(a) presents the architecture of proposed reversible fault tolerant D-latch using one MSH gate to produce the desired output, S=Clk .feedback⊕Clk.D with only two garbage G1 and G2 and one constant input. We use one proposed MSB gate to form a reversible fault tolerant 4×1 Mux having the Equation 1 and our proposed RFT multiplexer obtain the least garbage output which is clarified in Property 1. Block diagram is exhibited Fig. 5(b).

$$O_{MUX} = \overline{A}\,\overline{B}\,C + \overline{A}BE + A\overline{B}D + ABF \quad (1)$$

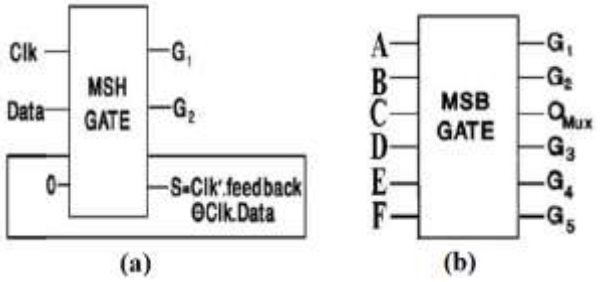

Figure 5: Block diagram of Proposed Reversible Fault Tolerant (a) D-Latch (b) 4X1 MUX.

Journal of Engineering Sciences

Vol 10, Issue 11, Nov /2019
ISSN NO: 0377-9254

SIMULATION RESULTS

A. 1-bit Full Adder/Subtractor

The schematic diagram and the simulation result for the Design-1 of one bit adder/subtractor using reversible gates is shown in the figures 6 and 7 respectively.

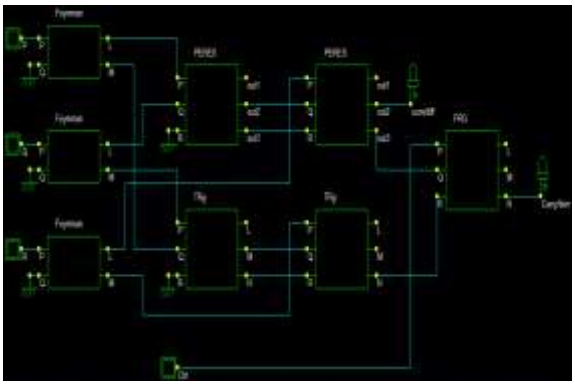

Figure 6: Schematic for Design-1 Reversible adder/subtractor

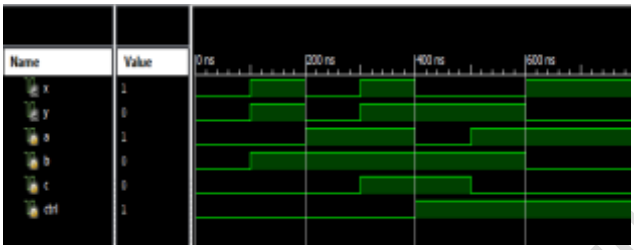

Figure 7: Simulation result for Design-1 Reversible adder/subtractor

The number of transistors in design-1 for the one bit full adder/subtractor can be further reduced by adopting the Design-2. The Schematic and simulation result for Design-2 of one bit full adder/subtractor is as shown in the figures 8 and 9 respectively.

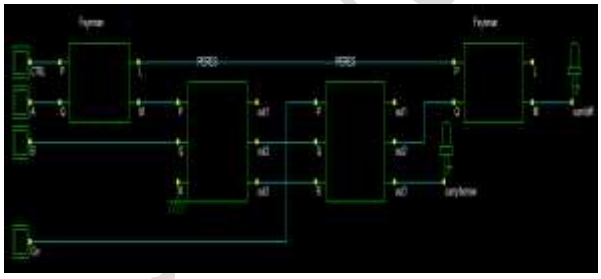

Figure 8: Schematic for Design-2 of Reversible adder/subtractor

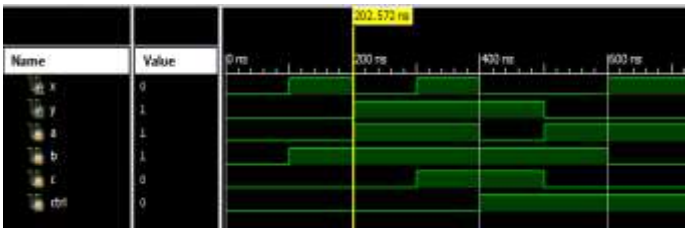

Figure 9: Simulation result for Design-2 of Reversible adder/subtractor

The following table briefly gives the comparison among the proposed Design-1 and Design-2 for Reversible one-bit full adder/subtractor circuit.

Paramater	Design-1	Design-2
No.of Transistors	126	48
Area (μm2)	656.5	205.7
Power (μW)	40.212	35.367

B. Reversible D-Latch

The schematic and timing diagram for the proposed reversible fault tolerant D-Latch using MSH gate is as shown in the following figures 10 and 11 respectively.

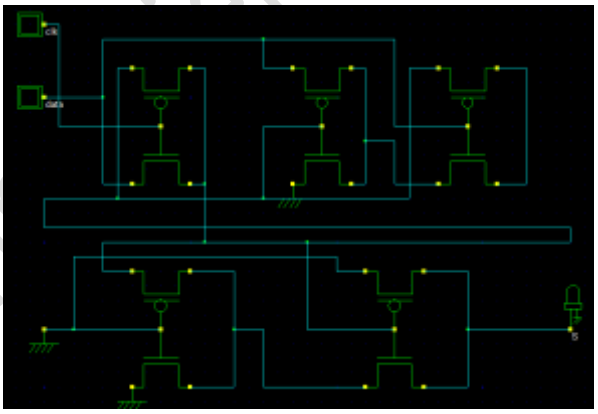

Figure 10: Schematic for D-Latch using MSH Gate

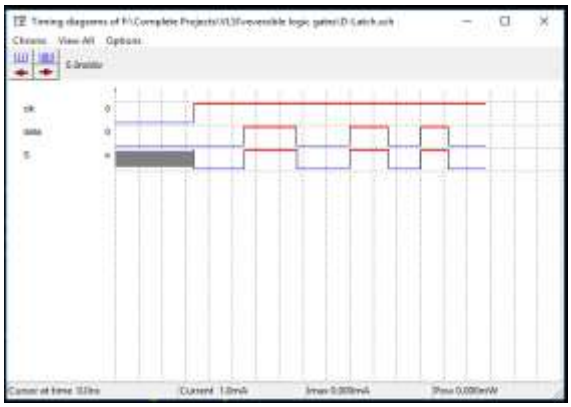

Figure 11: Timing Diagram for D-Latch

C. Reversible 4X1 Multiplexer

The schematic and timing diagram for the proposed reversible fault tolerant 4X1 Multiplexer using MSB gate is as shown in the following figures 12 and 13 respectively.

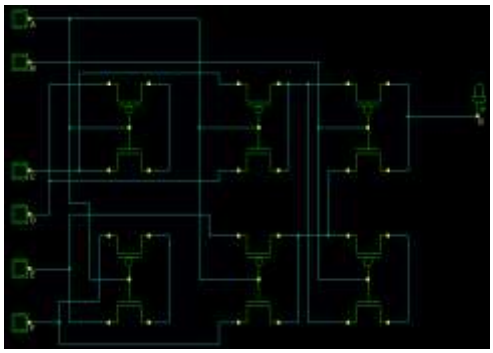

Figure 12: Schematic for 4X1 MUX using MSB Gate

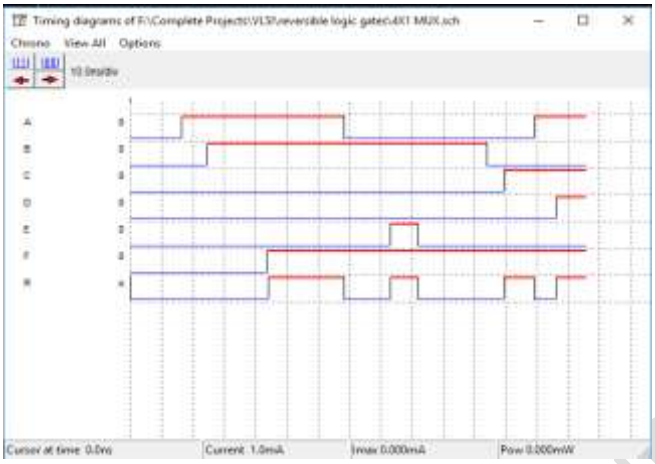

Fig 13: Timing Diagram for 4X1 MUX CONCLUSION

Reversible logic gates are used in the security system, increasing excessive power productivity, rate and effecting, less energy wastage etc. [16] It includes some of the areas like design of low power digital circuit, field programmable gate arrays in CMOS, low power circuit designs, nano technology and the optical computing etc. Proposing two new reversible gates known as MSH and MSB gates and these gates are solely used for the design of D-Latch and 4X1 Multiplexer respectively.

This paper presented the two different design methodologies of reversible fault tolerant 1-bit full adder/subtractor using Feynman, Peres, TR reversible gates. The simulation results are verified in Xilinx ISE Design suite 14.7 and the performance metrics are compared using the DSCH (Digital Schematic Editor and simulator) and Microwind.

CONCLUSION

Use of the reversible logic gates are increasing day by day but the scientists are still continue with their work on this to further more decreasing environmental decay growth .So mostly we can use this for the power consumption. In this project we just explained the types of the logic gates and its uses and how we can implement on these logic gates.Many Reversible gates are developed which can be further used for the design of various logic circuits.

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