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AN AREA EFFICIENT DESIGN OF PAL AND PLA USING REVERSIBLE LOGIC

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ABSTRACT- Reversible logic is the emerging field for research in present era. Reversible Logic owns its applications in various fields which include Quantum Computing, Optical Computing, Nano- technology, Computer Graphics, low power VLSI etc., Reversible logic is gaining its own importance in recent years largely due to its property of low power consumption and low heat dissipation. The aim of this paper is to design and synthesize a Programmable array Logic (PAL) and Programmable Logic array (PLA) using reversible logic with minimum quantum cost. The PAL is a Programmable Logic device which consists of programmable AND Gates and fixed OR gates array. The PLA is the PLD which contains programmable AND array and programmable OR array. The PLDs are the combinational circuits mainly used to realize Boolean functions on our interest. The reversible logic must run both forward and backward in such a way that the inputs can also be retrieved from outputs. Fan-out and Feed-back are not allowed in Logical Reversibility. To overcome the Fan out limitation, the signals from required output lines are duplicated to desired lines using additional reversible combinational circuits. In this paper, the design of PAL and PLA which has less heat dissipation and low power consumption is proposed. The designed circuits are analyzed in terms of quantum cost, garbage outputs and number of gates. Based on the results obtained from the proposed designs, it is certain that its performance is most overwhelming with the existing techniques of PLD's. The Circuit has been designed and simulated using Xilinx software.

I. INTRODUCTION

Conventional irreversible logic gates like two input AND, OR, NOT map two-bit input state to one-bit output state. Erasure of one bit and impossible to construct input from output consequently leads to energy loss. To avoid such energy loss two input states can be mapped to two output states so that input states can be uniquely recovered from output states and under such circumstances, a gate is said to be reversible. Reversible logic gates differ from Conventional irreversible logic gates as they don't permit feedback. The optimized reversible logic circuit consider various metrics like quantum cost, ancillary input lines, garbage outputlines.The quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-V+ and CNOT gates from NCV gate library and integrated qubit gates. Integrated qubits are a combination of Feynman gate and either controlled V or controlled V+ gate. Quantum cost of integrated qubit gate as well as 1*1 and 2*2 is one. The output lines which are not required but deliberately need to be added to maintain reversibility criterion of a reversible gate are known as Garbage Outputs. Garbage outputs are always undesired in any reversible circuit. Sometimes constant values 0 or 1 are deliberately applied to maintain reversibility criterion of a reversible gate. These constant values are also called as Ancillary Input lines. Ancillary inputs are also undesired in any reversible circuit .Programmable Array Logic (PAL) is a family of programmable logic device semiconductors used to implement logic functions in digital circuits introduced by Monolithic Memories, Inc. (MMI) in March 1978. MMI obtained a registered trademark on the term PAL for use in "Programmable Semiconductor Logic Circuits". The trademark is currently held by Lattice Semiconductor.PAL devices consisted of a small PROM (programmable read-only memory) core and additional output logic used to implement particular desired logic functions with few components. Using specialized machines, PAL devices were "field-programmable". PALs were available in several variants:

1) "One-time programmable" (OTP) devices could not be updated and reused after initial programming (MMI also offered a similar family called HAL, or "hard array logic", which were like PAL devices except that they were mask-programmed at the factory.).
2) UV erasable versions (e.g.: PAL Cxxxxx e.g.: PALC22V10) had a quartz window over the chip die and could be erased for re-use with an ultraviolet light source just like an EPROM.
3) Later versions (PAL CExxx e.g.: PALCE22V10) were flash erasable devices.

In most applications, electrically-erasable GALs are now deployed as pin-compatible direct replacements for one-time programmable PALs.
PAL devices have arrays of transistor cells arranged in a "fixed-OR, programmable-AND" plane used to implement "sum-of-products" binary logic equations for each of the outputs in terms of

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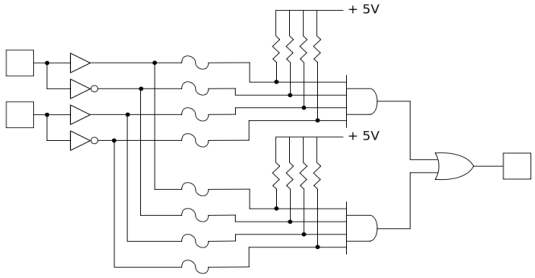
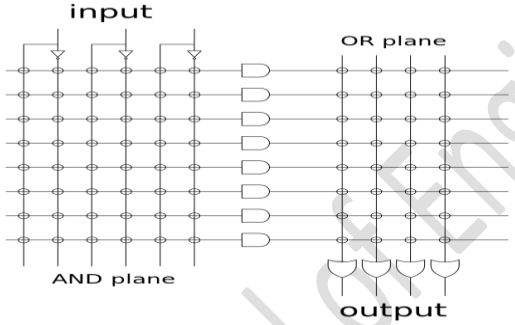
the inputs and either synchronous or asynchronous feedback from the outputs.



Simplified programmable logic device

A programmable logic array (PLA) is a kind of programmable logic device used to implement combinational logic circuits. The PLA has a set of programmable AND gate planes, which link to a set of programmable OR gate planes, which can then be conditionally complemented to produce an output. It has 2^N AND Gates for N input variables and for M outputs from PLA, there should be M OR Gates, each with programmable inputs from all of the AND gates. This layout allows for a large number of logic functions to be synthesized in the sum of products canonical forms. PLAs differ from Programmable Array Logic devices (PALs and GALs) in that both the AND and OR gate planes are programmable.



The Generic Array Logic (also known as GAL and sometimes as gate array logic [1]) device was an innovation of the PAL and was invented by Lattice Semiconductor. The GAL was an improvement on the PAL because one device was able to take the place of many PAL devices or could even have functionality not covered by the original range. Its primary benefit, however, was that it was erasable and re-programmable, making prototyping and design changes easier for engineers.

II. EXISTING METHOD

The Design of Combinational circuits [6][9][16] and Sequential Circuits [10][11] using reversible logic has been ongoing in research. Various proposals are given for the design of combinational circuits like adders, subtractors, multiplexers, decoders etc., in the existing method the author has given a novel design of 4x16 decoder [15] whose Quantum Cost is less than the previous design. Replacing fredkin gates for designing 2×4 decoder with reversible gates like Peres gate, TR gate, NOT gate and CNOT gate are used. The whole design is done using Fredkin, CNOT, Peres gates which give better Quantum. Cost when compared to the other reversible Logic gates. The number of gates required to design 4x16 decoder are 18 in which there are 12 fredkin gates, one peres gate, one TR gate, one NOT gate and 3 CNOT gates. The sum of all the quantum costs of each gate gives total quantum cost of 4x16 decoder. The sum of all the quantum costs of each gate used to design total circuit gives the quantum cost of total circuit.

A. EXISTING RPLA USING FEYNMAN GATE AND MUX GATE:

These two gates are best suits for the designing of as AND, OR, NOT and as data buffer which are used to implement the RPLA.

1. Feynman Gate

Fig.1 below shows the 2×2 reversible gate called Feynman gate [5]. Feynman gate is also recognized as controlled- not gate (CNOT). It has two inputs (A, B) and two outputs (P, Q). The outputs are defined by P=A, Q=A XOR B .This gate can be used to copy a signal. Since fan-out is not allowed in reversible logic circuits, the Feynman gate is used as the fan-out gate to copy a signal. Quantum cost of a Feynman gate is 1.

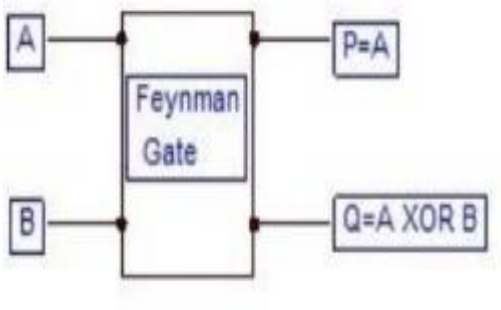


Fig.1 Feynman gate

2. MUX GATE:

Fig.2. shows the pictorial representation of 3×3 reversible gate called MUX (MG) gate [10]. It is a conservative gate having three inputs (A, B, C) and three outputs (P, Q, R). The outputs are defined by P=A, Q=A XOR B XOR C and R= A‟C XOR AB. The hamming weight of its input vector is same as the hamming weight of its output vector and its Quantum cost is 4.

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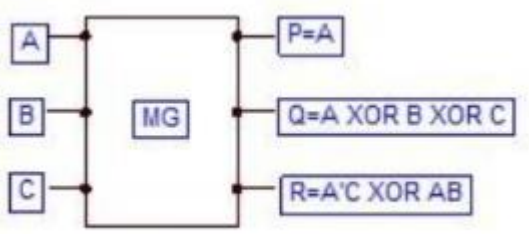
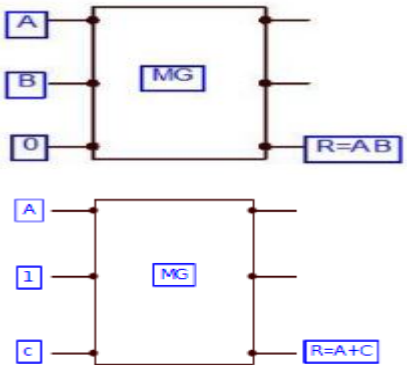


Fig.2. MG gate

3. MUX Gate as AND Gate and OR Gate

The structure of MUX gate as AND gate and OR gate are shown in the figures. If we provide "0" at third input C then the output R will provide the AND combination of first& second input and if we If we provide „1" at second input B then the output Q will provide the OR combination of the first & third input.



In this architecture, we used the two planes i.e. Reversible AND plane & Reversible OR plane as in conventional design. In this there are n number of inputs and m number of outputs and k number of product terms. The reversible AND plane is designed by the MUX & Feynman gates to produce the required product terms and to prevent of fan-out..The reversible AND plane is designed by the MUX gate.

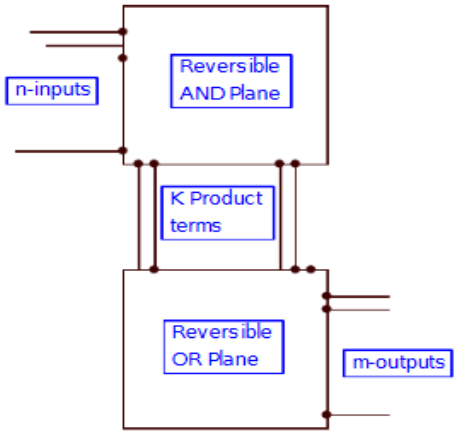


Fig.3 existing RPLA using Feynman gate and MUX gate.

III. PROPOSED METHOD

The Programmable Array Logic (PAL), Programmable Logic array (PLA) is realized using reversible Fredkin gate and Feynman gate as shown in the figures respectively. The concept of duplicating a single output to required number of outputs using Feynman gate is introduced where Fan-out was not allowed in reversible computation. The standard irreversible conventional PLDs can be programmed only once. The irreversible PLDs consist of a series of fuses which can be burned to program the device. By burning the fuses the chip can be programmed which is an irreversible process..In reversible PLDs structure, the fuses are replaced with a reversible fuse which is made of reversible Feynman gate and fredkin gate as shown in the below figure1. The Feynman reversible gate acts as a duplicating circuit. It duplicates the output line into two output lines out of which one output line drives the next circuit and the other drives the second input of 2×1 reversible multiplexer. The first input of reversible multiplexer is grounded so that when the enable signal 'E' is low it acts as an 'off' switch. The reversible multiplexer is made of Fredkin gate as shown in the below figure 4 (b).

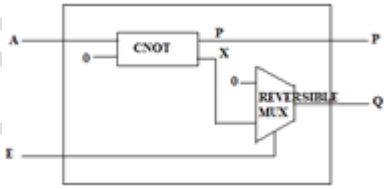


Fig.4 (a)Reversible Fuse

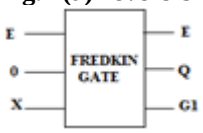


Fig.4 (b) Reversible MUX

The fixed connections are replaced by CNOT gates in which the second input is set to '0' always. The CNOT gates give solution for two remedies. It overcomes the feedback limitation and it acts as a fixed connection.

A. REVERSIBLE PAL

The Design of PAL made of reversible logic which is programmed to perform the operation of the below Boolean algebraic equations is shown in the below figure. The PAL consists of fixed OR gates array and programmable AND gate array.

F1=I[1]I[2]+I[1]I[3]'+I[1]'I[2]'I[3] ……Eqn(1)
F2=I[1]I[2]+I[1]'I[2]'I[3]+I[1]I[3] ……..Eqn(2)
F3=I[1]I[3]'+ I[1]I[2]I[3] …… Eqn(3)

Contemporary to irreversible PAL, the fuses are replaced with programmable reversible fuses and the fixed connections are replaced with the CNOT gates as shown in the figure. The 'P' output of fuse drives the subsequent fuse and the 'Q' output of

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fuse drives the input of AND gate as shown in figure. The output of AND gate drives the fixed connections i.e., CNOT gate. The 'P' output of CNOT gate drives the next. Fixed connection and the 'Q' output of CNOT drives the input of OR gate.

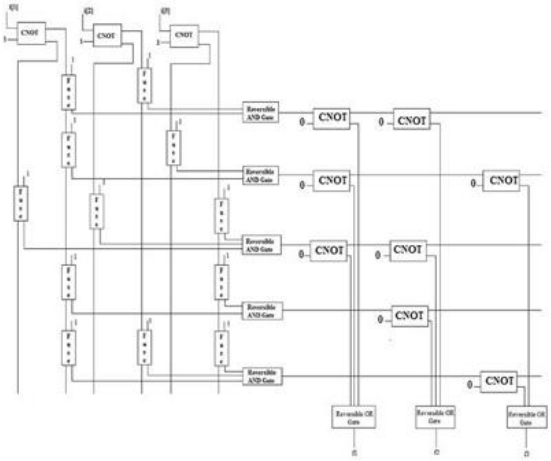

Fig.5. Circuit diagram of Reversible PAL to perform Boolean algebraic equations operation.

B. REVERSIBLE PLA

The OR Gates and AND gates used in PLDs are made of Reversible logic. The 'n' input OR gate consists of 'n' number of inputs. If any inputs are kept ideal without use they are to be driven with ground (binary value '0') so that the high impedance value is not driven to OR gate which effects the operation of OR gate. The fuses left without programming drives the value zero to the reversible OR gate which doesn't affect the operation of OR gate. Contrast to OR gate, for AND gate the left out inputs are driven with HIGH signal so that the operation of AND gate is not effected.The circuit diagram of a Programmable Logic Array constructed using reversible logic to program Boolean equations Eqn (1), Eqn (2), Eqn (3) is shown in the above figure. In PLA both the AND gate array and OR gate arrays are programmable. Hence reversible fuses are used to program the AND gate array and OR gate array of the device as shown in the figure.

C. REVERSIBLE GAL

Similarly the circuit diagram of a Generic Array Logic constructed using reversible logic to program Boolean equations Eqn(1), Eqn(2), Eqn(3) is shown in the below figure. In GAL the outputs are also programmable along with the AND gate array and OR gate array. Hence it differs from PLA. Therefore reversible fuses are used to program the device as shown in the figure.

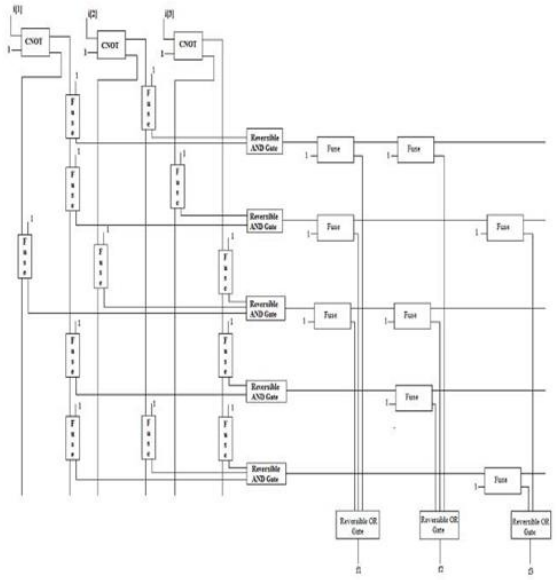

Fig.6. Circuit diagram of Reversible 3-5-3 PLA to perform Boolean Algebraic equations operation.

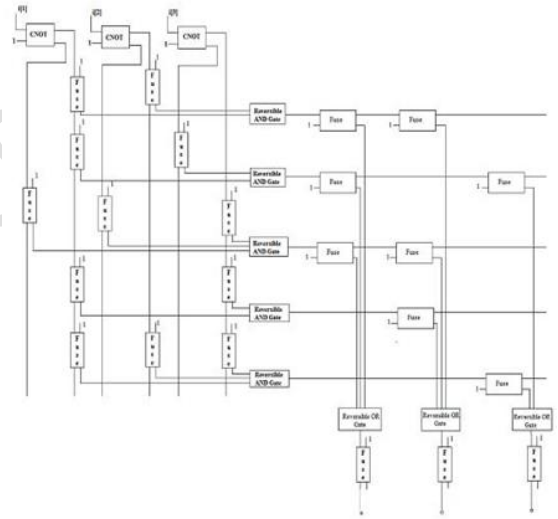

Fig.7. Circuit diagram of Reversible GAL to perform Boolean Algebraic equations operation

IV. SIMULATION RESULTS

The below figures shows the simulation output of proposed PAL, PLA, GAL simulated output for Eqn1 to Eqn3 implemented using reversible PAL is shown in the figure respectively.

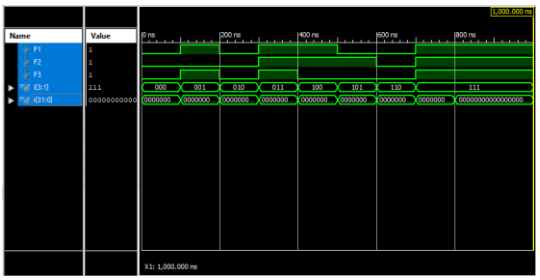

Fig.8. simulation output of proposed reversible PAL

Simulated output for Eqn1 to Eqn3 implemented using reversible PLA is shown in the figure respectively.

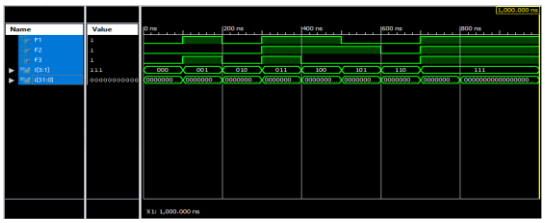

Fig.9. simulation output of proposed PLA

Simulated output for Eqn1 to Eqn3 implemented using reversible GLA is shown in the figure respectively.

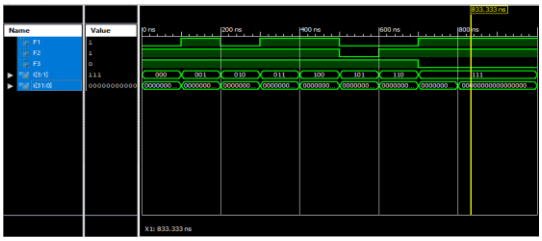

Fig.10. simulation output of proposed reversible GAL

V. CONCLUSION

The method of realizing different Boolean functions using reversible PLDs like reversible PAL, reversible PLA, reversible GAL are explained. These circuits are designed for minimum quantum cost and minimum garbage outputs. To overcome the fan-out limitation in reversible logic circuits the concept of duplicating the single output to required number of output lines is implemented by using additional reversible combinational circuits. The reversible PLDs are implemented using a reversible fuse and Feynman gate. The reversible fuse is made of CNOT gate and fredkin gate which is used for programmable connections. Feynman gate with second input made zero is used for fixed connections. The reversible circuits used for designing programmable connections and fixed connections give minimum heat dissipation. By using this reversible PLDs eighty percentage of efficiency can be acquired in terms of heat dissipation. The time delay increases a little when compared to irreversible PLDs which can be termed as a disadvantage but it is negligible. The time delays for reversible PAL, PLA and GAL are 5.847nsec, 5.847nsec and 5.847nsec respectively. The time delay depends upon the Boolean expressions considered to program on the device. The time delay is the function of quantum cost. The quantum cost increases with increase in length of Boolean function because the number of programmable reversible fuses and Feynman gates (fixed connectors) increases with increase in length of Boolean function. If quantum cost increases, the time delay also increases.

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