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A NEW CONTROL FOR TWO PV ARRAYS IN MISMATCHED ENVIRONMENTAL CONDITIONS IN GRID CONNECTED PV INVERTER TO MAXIMIZING POWER

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Abstract—A single phase grid connected transformer less photo voltaic (PV) inverter which can operate either in buck or in boost mode, and can extract maximum power simultaneously from two serially connected sub arrays while each of the sub array is facing different environmental conditions, is presented in this paper. As the inverter can operate in buck as well as in boost mode depending on the requirement, the constraint on the minimum number of serially connected solar PV modules that is required to form a sub array is greatly reduced. As a result power yield from each of the sub array increases when they are exposed to different environmental conditions. The topological configuration of the inverter and its control strategy are designed so that the high frequency components are not present in the common mode voltage thereby restricting the magnitude of the leakage current associated with the PV arrays within the specified limit. Further, high operating efficiency is achieved throughout its operating range. A detailed analysis of the system leading to the development of its mathematical model is carried out. The viability of the scheme is confirmed by performing detailed simulation studies. A 1.5 kW laboratory prototype is developed, and detailed experimental studies are carried out to corroborate the validity of the scheme. Index Terms—Grid connection, Single phase, Transformer less, Buck & Boost based PV inverter, Maximum power point, Mismatched environmental condition, Series connected module.

I.INTRODUCTION

THE major concern of a photo voltaic (PV) system is to ensure optimum performance of individual PV modules in a PV array while the modules are exposed to different environmental conditions arising due to difference in insolation level and/or difference in operating temperature. The presence of mismatch in operating condition of modules significantly reduces the power output from the PV array. The problem with the mismatched environmental conditions (MEC) becomes significant if the number of modules connected in series in a PV array is large. In order to achieve desired magnitude for the input dc link voltage of the inverter of a grid connected transformer less PV system, the requirement of series connected modules becomes high. Therefore, the power output from a grid connected transformer less (GCT) PV system such as single phase GCT (SPGCT) inverter based systems derived from H-bridge and neutral point clamp (NPC) inverter based systems get affected significantly during MEC. In order to address the problem arising out of MEC in a PV system, various solutions are reported in the literature. An exhaustive investigation of such techniques has been presented. Power extraction during MEC can be increased by choosing proper interconnection between PV modules or by tracking global maximum power point (MPP) of PV array by employing complex MPP tracking (MPPT) algorithm. However, these techniques are not effective for low power SPGCT PV system. Similarly, reconfiguration of the PV modules in a PV array by changing the electrical connection of PV modules is not effective for SPGCT PV system due to the considerable increment in component count and escalation in operating complexity. In order to extract maximum power from each PV module during MEC, attempts have been made to control each PV module in a PV array either by having a power electronic equalizer or by interfacing a dc to dc converter. Schemes utilizing power electronic equalizer require large component count thereby increasing the cost and operation complexity of the system. The scheme presented in uses generation control circuit (GCC) to operate each PV module at their respective MPP wherein the difference in power between each module is only processed through the GCC. Scheme presented in uses shunt current compensation of each module as well as series voltage compensation of each PV string in a PV array to enhance power yield during MEC.

The schemes based on module integrated converter use dedicated dc to dc converter integrated with each PV module. However, the efficiency of the aforesaid schemes are low due to the involvement of large number of converter stages, and further in these schemes the component count is high and hence they face similar limitations as that of power electronic equalizer based scheme. Instead of ensuring MPP operation of each and every module, certain number of modules is connected in series to form a string and the so formed strings are then made to operate

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under MPP. Even then there is not much reduction in overall component count and control complexity. In order to simplify the control configuration and to reduce the component count, schemes reported combine all the PV modules into two sub arrays, and then each of the sub array is made to operate at their respective MPP. However, the reported overall efficiency of both the schemes are poor. By introducing a buck and boost stage in SPGCT PV inverter, power extraction during MEC is improved. Further, as a consequence of the presence of the intermediate boost stage, the requirement of series connected PV modules in a PV array has become less.

In the schemes presented, the switches of either the dc to dc converter stage or inverter stage operate at high frequency; as a result there is a considerable reduction in the size of the passive element count, thereby improving the operating efficiency of these schemes. Further, the reported efficiency is 1-2 % higher than that of. An effort has been made in this paper to divide the PV modules into two serially connected sub arrays and controlling each of the sub array by means of a buck and boost based inverter so that optimum power evacuation from the sub arrays is ascertained during MEC. This process of segregation of input PV array into two sub arrays reduces the number of series connected modules in a sub array almost by half compared to that of the schemes proposed. The topological structure and control strategy of the proposed inverter ensure that the magnitude of leakage current associated with the PV arrays remains within the permissible limit. Further, the voltage stress across the active devices is reduced almost by half compared to that of the schemes presented, hence very high frequency operation without increasing the switching loss is ensured. High frequency operation also leads to the reduction in the size of the passive elements. As a result the operating efficiency of the proposed scheme is high. The measured peak efficiency and the European efficiency (ηeuro) of the proposed scheme is found to be 97.65% and 97.02% respectively.

II.PHOTOVOLTAIC INVERTER

The basic block diagram of grid connected PV power generation system is shown in Fig. 2.1.The PV power generation system consists of following major blocks:

1. PV unit : A PV unit consists of number of PV cells that converts the energy of light directly into electricity (DC) using photovoltaic effect.
2.Inverter : Inverter is used to convert DC output of PV unit to AC power.
3.Grid : The output power of inverter is given to the near by electrical grid for the power generation.
4.MPPT : In order to utilize the maximum power produced by the PV modules, the power conversion equipment has to be equipped with a maximum power point tracking (MPPT).It is a device which tracks the voltage at where the maximum power is utilized at all times.

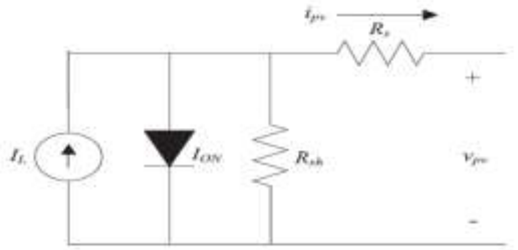


Fig1. Equivalent Circuit Diagram of PVCell

$$i_{pv} = I_L - I_s[\exp[\alpha(v_{pv} + R_s i_{PV})] - 1] - \frac{v_{pv} + R_s i_{pv}}{R_{sh}}$$

2.1 MPPT: (Maximum Power Point Tracking)

Maximum power point tracking (MPPT) is a technique to maximize the energy obtained over all normal operating conditions. The use of MPPT can reduce the cost of energy by making the system more efficient. The problem raised by MPPT methods is to automatically find the voltage or current (V_{mp}, I_{mp}) in which a PV array works on its maximum power point under a certain irradiance and temperature. There are many techniques to realize the MPPT. However, most techniques respond to both irradiance and temperature variations but some responds to constant temperature.

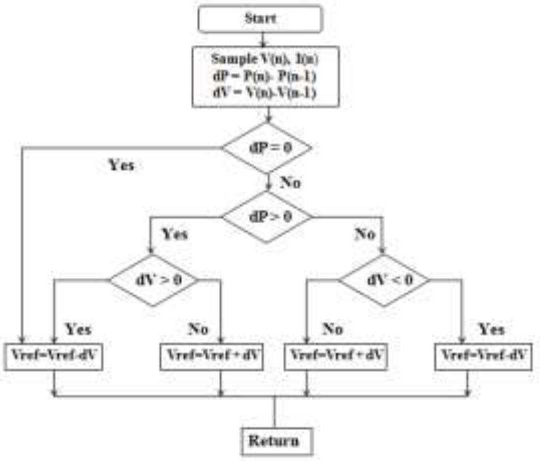
2.1.1 Perturb and Observe algorithm

At present, the most popular MPPT method in the PV systems is perturb and observe. In this method, a small perturbation is injected to the system and if the output power increases, a perturbation with the same direction will be injected to the system and if the output power decreases, the next injected perturbation will be in the opposite direction.

The Perturb and observe algorithm operates by periodically perturbing (i.e. incrementing or decrementing) the array terminal voltage and comparing the PV output power with that of the previous perturbation cycle.

If the PV array operating voltage changes and power increases, the control system moves the PV array operating point in that direction, otherwise the operating point is moved in the opposite direction.

In the next perturbation cycle, the algorithm continues in the same way. The logic of algorithm is shown in flow chat 2.1. A common problem in perturb and observe algorithm is that the array terminal voltage is perturbed every MPPT cycle, therefore when the maximum power point is reached, the output power oscillates around the maximum power point resulting in power loss in the PV system.



Flow Chart 1: Perturb and Observe

III. DC-DC CONVERTER BASICS

A DC-to-DC converter is a electronic circuit or electromechanical device that converts a source of direct current(DC) from one voltage level to another.It is a type of electrical power converter.Power levels range from very low (small batteries) to very high (high-voltage power transmission).It is a gadget that acknowledges a DC info voltage and produces a DC yield voltage. Normally the yield delivered is at an alternate voltage level than the info. Also, DC-to-DC converters are utilized to give clamor confinement, force transport regulation, and so on. This is a synopsis of a portion of the prevalent DC-to-DC converter topologies.

3.1 Boost Converter

The schematic in Fig.3.6 shows the basic boost converter. This circuit is used when a higher output voltage than input is required.

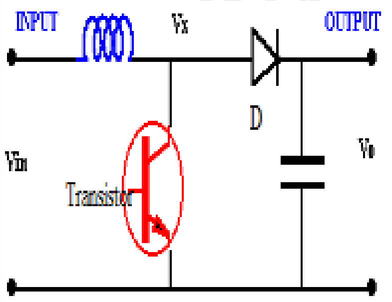


Fig1.1. Boost Converter Circuit

While the transistor is ON $V_x = V_{in}$, and the OFF state the inductor current flows through the diode giving $V_x = V_o$. For this analysis it is assumed that the inductor current always remains flowing (continuous conduction). The voltage across the inductor is shown in Fig.3.7 and the average must be zero for the average current to remain in steady state

IV.PROPOSED INVERTER AND ITS CONTROL

The schematic of the proposed Dual Buck & Boost based Inverter (DBBI) which is depicted in Fig. 2 is comprising of a dc to dc converter stage followed by an inverting stage. The dc to dc converter stage has two dc to dc converter segments, CONV1 and CONV2 to service the two subarrays, P V1 and P V2 of the solar PV array. The segment, CONV1 is consisting of the self-commutated switches, S1 along with its anti-parallel body diode, D1, S3 along with its anti-parallel body diode, D3, the free wheeling diodes, Df1, Df3 and the filter inductors and capacitors, L1, Cf1, and Co1. Similarly, the segment, CONV2 is consisting of the self-commutated switches, S2 along with its anti-parallel body diode, D2, S4 along with its anti-parallel body diode, D4, the free wheeling diodes, Df2, Df4 and the filter inductors and capacitors, L2, Cf2, and Co2. The inverting stage is consisting of the self-commutated switches, S5, S6, S7, S8, and their corresponding body diodes, D5, D6,D7 and D8 respectively. The inverter stage is interfaced with the grid through the filter inductor, Lg. The PV array to the ground parasitic capacitance is modeled by the two capacitors, Cpv1 and Cpv2.

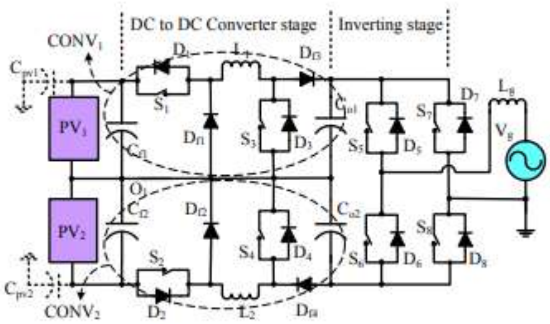


Fig. 2. Dual Buck & Boost based Inverter (DBBI)

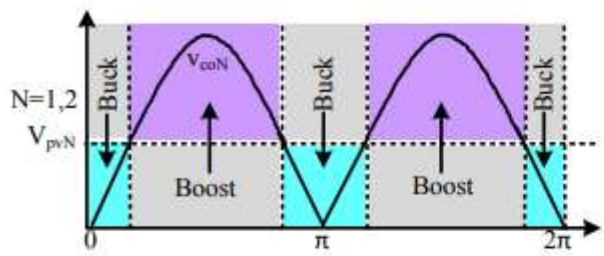
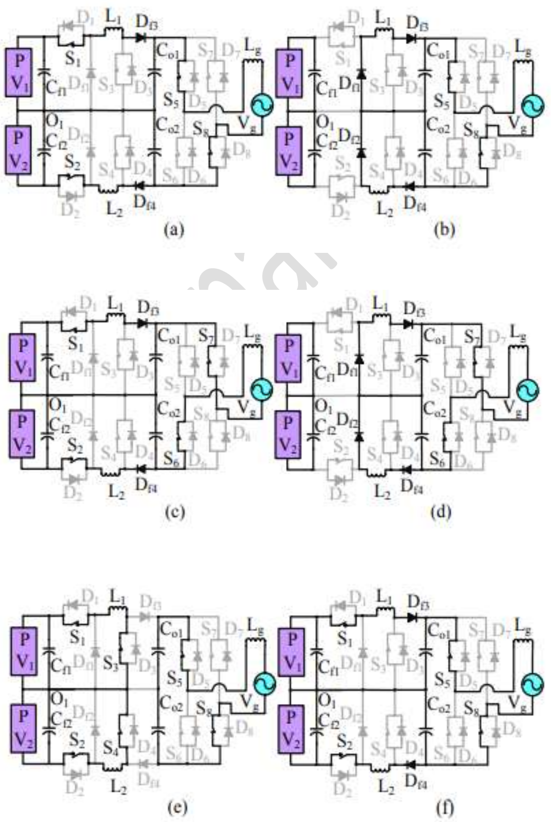


Fig. 2.1. Buck stage and Boost stage of the proposed inverter

Considering Fig. 2, CONV1 operates in buck mode when Vpv1 ≥ vco1, while CONV2 operates in buck mode when Vpv2 ≥ vco2. Vpv1, Vpv2 are the MPP voltages of P V1 and P V2 and vco1, vco2 are the output voltages of CONV1 and CONV2 respectively. During buck mode duty ratios of the switches, S1 and S2 are varied sinusoidally to ensure sinusoidal grid current (ig) while S3 and S4 are kept off. When Vpv1 < vco1, CONV1 operates in boost mode while CONV2 operates in boost mode when Vpv2 < vco2. During boost mode duty ratios of the switches, S3 and S4 are varied sinusoidally to ensure sinusoidal ig while S1 and S2 are kept on throughout this mode. The sinusoidal switching pulses of the switches of CONV1 and CONV2 are synchronized with the grid voltage, vg to accomplish unity power factor operation. The switches, S5 and S8 are kept on and switches S6 and S7 are kept off permanently during the entire positive half cycle (PHC) while during entire negative half cycle (NHC), the switches, S6 and S7 are kept on and switches, S5 and S8 are kept off permanently. All the operating states of the proposed inverter are depicted in Fig. 2.1. When the insolation level and ambient temperature of subarray P V1 are different from that of P V2, the MPP parameters



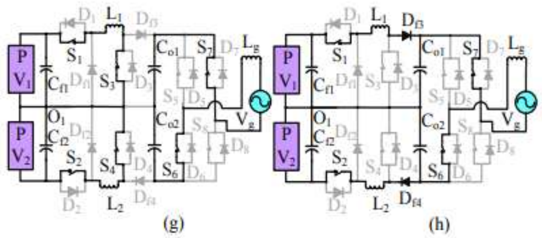


Fig. 3. Operating states of DBBI: (a) Active and (b) Freewheeling states in buck mode of PHC, (c) Active and (d) Freewheeling states in buck mode of NHC, (e) Active and (f) Freewheeling states in boost mode of PHC, (g) Active and (h) Freewheeling states in boost mode of NHC

of the two subarrays, Vpv1 and Vpv2, MPP current, Ipv1 and Ipv2 correspond to P V1 and P V2 respectively and power at MPP, Ppv1 and Ppv2 correspond to P V1 and P V2 respectively differ from each other. By considering that both the subarrays are operating at their respective MPP and neglecting the losses incurred in power processing stages, the average power involved with Co1 and Co2, Pco1 and Pco2 over a half cycle can be assumed equal to the power extracted from P V1 and P V2. Therefore,

Pco1 = Ppv1 & Pco2 = Ppv2 (1)

The power injected to the grid averaged over a half cycle, Pg can be written as

Pg = Ppv1 + Ppv2 (2)

4.1 CONTROL STRATEGY OF THE PROPOSED SCHEME

The control strategy of the proposed scheme is depicted in Fig. 5. The controller is designed to fulfill the following objectives: i) both subarrays operate at their corresponding MPP simultaneously, ii) sensing of output voltages, vco1 and vco2 are not required, iii) ig is sinusoidal and is in-phase with vg throughout the operating range. Two separate MPP trackers and two proportional integral (PI) controllers are employed to determine the value of Ppv1 and Ppv2 which are required to estimate Vco1m and Vco2m. Using (12), Vco1m and Vco2m are determined where the information of Vm is obtained from the phase locked loop (PLL). A rectified version of a unity sinusoidal function, R is generated from a unity sinusoidal function, X, synchronized with vg, and is obtained from the same PLL. R is multiplied with Vco1m and Vco2m to estimate vco1 and vco2. Hence, two voltage sensors which otherwise would have been required to determine vco1 and vco2 get eliminated. Vpv1 and vco1 are compared to decide about the mode of operation (buck mode or boost mode) of CONV1, while Vpv2 and vco2 are compared to determine the mode of operation of CONV2. RMS values of vco1 and vco2 are estimated which are then subsequently squared and are then divided by Ppv1 and Ppv2 to obtain the emulated effective resistances, Rpco1 and Rpco2 of the two component converters. Subsequently the reference current, iL1ref of L1 and the reference current, iL2ref of L2, are synthesized by utilizing (28) in the buck mode

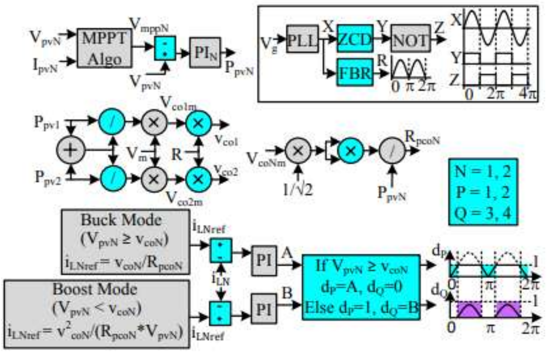


Fig. 5. Control configuration of the proposed inverter

V. SIMULATION RESULTS

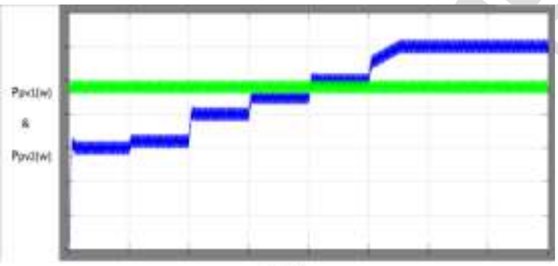


Fig. 6.a. Simulated Waveform: Variation in Ppv1 and Ppv2

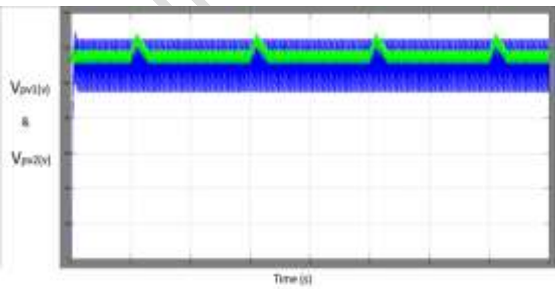


Fig. 6.b. Simulated Waveform: Variation in Vpv1 and Vpv2 during entire range of operation

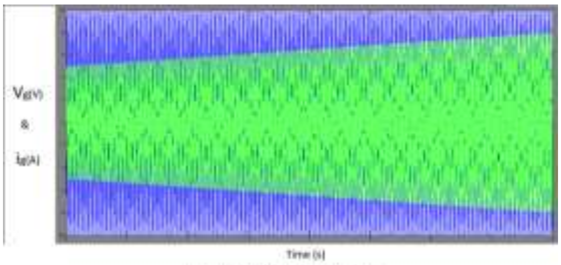


Fig. 7. Simulated Waveform: Vg and Ig

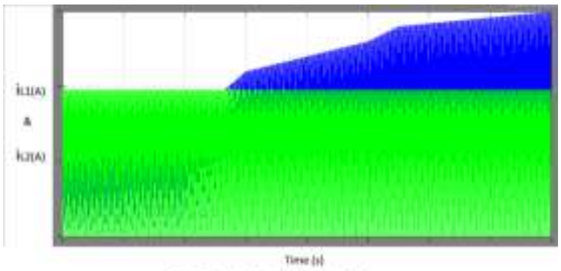


Fig. 8. Simulated Waveform: iL1 and iL2

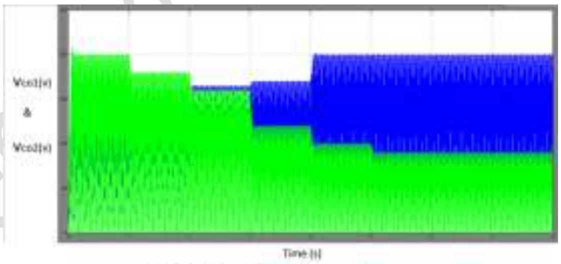


Fig. 9. Simulated Waveform: Vco1 and Vco2

VI.CONCLUSION

A single phase grid connected transformer less buck and boost based PV inverter which can operate two sub arrays at their respective MPP was proposed in this paper. The attractive features of this inverter were i) effect of mismatched environmental conditions on the PV array could be dealt with in an effective way, ii) operating efficiency achieved, ηeuro = 97.02% was high, iii) decoupled control of component converters was possible, iv) simple MPPT algorithm was employed to ensure MPP operation for the component converters, v) leakage current associated with the PV arrays was within the limit mentioned in VDE 0126-1-1. Mathematical analysis of the proposed inverter leading to the development of its small signal model was carried out. The criterion to select the values of the output filter components was presented. The scheme was validated by carrying out detailed simulation studies and subsequently the viability of the scheme was ascertained by carrying out thorough experimental studies on a 1.5 kW prototype of the inverter fabricated for the purpose.

REFERENCES

[1] T. Shimizu, O. Hashimoto, and G. Kimura, "A novel high-performance utility-interactive photovoltaic inverter system," IEEE Trans. Power Electron., vol. 18, no. 2, pp. 704-711, Mar. 2003.

[2] S. V. Araujo, P. Zacharias, and R. Mallwitz, "Highly efficient single phase transformer less inverters for grid-connected photovoltaic systems," IEEE Trans. Ind. Electron., vol. 57, no. 9, pp. 3118-3128, Sep. 2010.

[3] B. Ji, J. Wang, and J. Zhao, "High-efficiency single-phase transformer less PV H6 inverter with hybrid modulation method," IEEE Trans. Ind. Electron., vol. 60, no. 5, pp. 2104-2115, May 2013.

[4] R. Gonzalez, E. Gubia, J. Lopez, and L. Marroyo, "Transformer less single phase multilevel-based photovoltaic inverter," IEEE Trans. Ind. Electron., vol. 55, no. 7, pp. 2694-2702, Jul. 2008.

[5] H. Xiao and S. Xie, "Transformer less split-inductor neutral point clamped three-level PV grid-connected inverter," IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1799-1808, Apr. 2012.

[6] A. Bidram, A. Davoudi, and R. S. Balog, "Control and circuit techniques to mitigate partial shading effects in photo voltaic arrays," IEEE J. Photovolt., vol. 2, no. 4, pp. 532-546, Oct. 2012.