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CASCADED H-BRIDGE MULTI LEVEL INVERTER BASED IMPROVED PHASE SHIFTED CARRIER BASED SYNCHRONIZED SINUSOIDAL PWM TECHNIQUES

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ABSTRACT:

This project analyses synchronization strategy for cascaded H-Bridge multi-level inverter (CHBMLI) topologies with carrier based sinusoidal phase shifted pulse width modulation (PSPWM) technique. In PSPWM technique a separate carrier is used for each H-Bridge (HB). The carriers are generally phase shifted from each other by π/x rad (x=No. of HBridges) for unipolar PWM. With the carrier frequency being an integer (odd/even) multiple of the fundamental frequency, it is observed that, the positions of zero crossings of the carriers with respect to the zero crossings of voltage references play an important role for maintaining quarter wave symmetry among multi level inverter (MLI) pole voltage waveforms. This paper analytically shows the conditions for half wave symmetry and quarter wave symmetry and experimentally verifies those conditions for PSPWM technique with a five level CHBMLI laboratory prototype.

Index Terms—cascaded H-Bridge multilevel inverter, phase shifted carrier based PWM, synchronous PWM, half wave symmetry, quarter wave symmetry.

I. INTRODUCTION

With the increasing demand of medium voltage and high power drives, the use of multilevel inverters is gradually becoming more and more important. This is due to reduced voltage stress on semiconductor devices, reduced harmonics in inverter output voltage and lesser electromagnetic interferences. For medium voltage and high power applications, the switching frequency and device ratings are limited [1]-[3]. Increasing the power rating by minimizing the switching frequency, while still maintaining reasonable power quality is an important requirement and a persistent challenge [2]-[3]. Hence, the use of multilevel inverters suitably distributes the stress among the semiconductor switches. Among the different multilevel inverter topologies, the cascaded H-Bridge (CHB) topology is a preferred choice for medium voltage drives for its modularity and this is also the target converter for the proposed PWM technique in this project.

In high power and medium voltage applications, the power converters operate at low switching frequency. This is very well defined in the literature as low pulse ratio operation of the converters. The applications consist of traction drives, grid applications etc. As the pulse ratio is less in these power converters, lower order harmonics including sub-harmonics are introduced in line currents resulting in higher total harmonic distortion (THD). Hence, synchronization among PWM voltages is necessary. Along with synchronization, the PWM voltage should maintain half wave, quarter wave and three phase symmetries [4]-[5].

II. Literature Survey:

Reference [6] shows the advantages of maintaining the above waveform symmetries. The synchronization ensures the PWM voltage is free from the sub-harmonics. Three phase symmetry among the PWM voltages ensures the fundamental and the harmonics are balanced and also free from dc offset. Moreover, three phase symmetry also ensures that, the triplen harmonics are in phase and appear as zero

sequence voltage with the advantage of not contributing to the ripple current.

Half wave symmetry ensures the PWM voltages are free from even order harmonics. Although quarter wave symmetry does not eliminate any harmonics, it ensures that the existing fundamental and harmonics have only sine component and eliminates the possibility of phase error between the reference and the fundamental output voltage. Reference [7] proposes an optimal PWM scheme for two level inverters to reduce current harmonics with offline calculations of switching pattern. This optimized PWM strategy can also be extended to multilevel inverters.

Reference [8] shows the application of synchronized optimal PWM technique for a cascaded nine level inverter, where the average device switching frequency is limited to rated fundamental frequency. Reference [9] compares the performances of five level and seven level NPC inverters with synchronous optimal PWM technique. But, the synchronized optimal PWM technique is an offline calculation based technique. The switching angles are pre-calculated assuming steady state condition and this requires storage of large data for better accuracy. Reference [10] proposes a trajectory tracking control for three level NPC with synchronous optimal PWM technique.

Reference [11] proposes the model predictive pulse pattern control for a five level NPC inverter with optimized PWM technique. Selective harmonic elimination and selective harmonic mitigation PWM techniques are the other alternatives. Reference [12] shows the application of SHEPWM technique for cascade multi level inverters, whereas [13] shows the use of SHMPWM technique. But they are also offline calculation based PWM technique and require lookup tables for implementation, hence the more microcontroller memory space. References [14]-[16] show the application of online harmonic compensation scheme to improve the existing SHEPWM technique for high power converters. These references mainly focus on grid connected high power converters (i.e. current source rectifiers).

All the above multilevel inverter PWM techniques are based on offline calculations. The calculation complexity increases with increase in number of voltage levels or increase in the number of commutation angles at lower modulation indexes. But the carrier based PWM techniques are independent of motor parameters, independent of optimization and does not require offline calculation or look-up tables to generate firing angles. Hence, carrier based PWM technique is well suited to multi level inverters although the harmonic contents of the inverter output pole voltage are not optimized.

Two carrier based PWM techniques are available in literature for MLIs. They are:- (i) Level shifted PWM technique (LSPWM technique) (ii) Phase shifted PWM technique (PSPWM technique). But, the major challenge for the carrier based PWM techniques for MLIs is to position the zero crossings of carriers‘ with respect to the zero crossings of voltage references so that different symmetries among pole voltage waveforms can be maintained. For two-level inverters, synchronization with different symmetries is achievable if the zero crossings of the carrier matches with the zero crossings of the voltage references and the ratio _p‘ (p=fc /fs where fc= carrier frequency and fs=voltage reference frequency) is maintained to be an odd integer (multiple of 3).

The carrier synchronization with the voltage references is sufficient for the Level Shifted PWM (LSPWM) technique for CHBMLIs, as only one synchronous carrier is sufficient to implement different voltage levels [17]. Hence, the pole voltage maintains all the basic properties of an ideal synchronous PWM technique. But, the power distribution and average device switching frequencies of different H-Bridges are different. But this scenario is completely different for the PSPWM technique, as multiple phase shifted synchronous carriers are used for different H-Bridges. So, it is impossible to match the zero crossings of each carrier with the voltage reference zero crossings.

Hence, the positions of the zero crossings of voltage references with respect to the zero crossings of carriers play an important

role for maintaining different basic properties of an ideal synchronous PWM, as stated in the previous paragraph. This paper mainly deals with the analytical studies for maintaining half wave symmetry and quarter wave symmetry among CHBMLI pole voltage waveform with synchronous sinusoidal PSPWM technique. The carriers used for the analysis in this paper are generated from the instantaneous voltage references, as in [17]-[19] and always maintain an integer ratio p.

III. HARMONIC

The typical definition for a harmonic is "a sinusoidal component of a periodic wave or\ quantity having a frequency that is an integral multiple of the fundamental frequency." [1]. Some references refer to "clean" or "pure" power as those without any harmonics. But such clean waveforms typically only exist in a laboratory. Harmonics have been around for a long time and will continue to do so. In fact, musicians have been aware of such since the invention of the first string or woodwind instrument. Harmonics (called "overtones" in music) are responsible for what makes a trumpet sound like a trumpet, and a clarinet like a clarinet.

Electrical generators try to produce electric power where the voltage waveform has only one frequency associated with it, the fundamental frequency. In the North America, this frequency is 60 Hz, or cycles per second. In European countries and other parts of the world, this frequency is usually 50 Hz. Aircraft often uses 400 Hz as the fundamental frequency. At 60 Hz, this means that sixty times a second, the voltage waveform increases to a maximum positive value, then decreases to zero, further decreasing to a maximum negative value, and then back to zero. The rate at which these changes occur is the trigometric function called a sine wave, as shown in figure 1. This function occurs in many natural phenomena, such as the speed of a pendulum as it swings back and forth, or the way a string on a voilin vibrates when plucked.

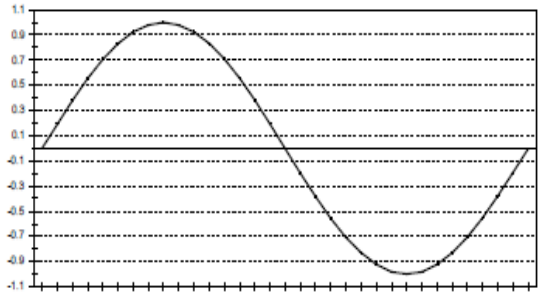

Fig.1. Sine wave

The frequency of the harmonics is different, depending on the fundamental frequency. For example, the 2nd harmonic on a 60 Hz system is 2*60 or 120 Hz. At 50Hz, the second harmonic is 2* 50 or 100Hz.

300Hz is the 5th harmonic in a 60 Hz system, or the 6th harmonic in a 50 Hz system. Figure 2 shows how a signal with two harmonics would appear on an oscilloscope-type display, which some power quality analyzers provide.

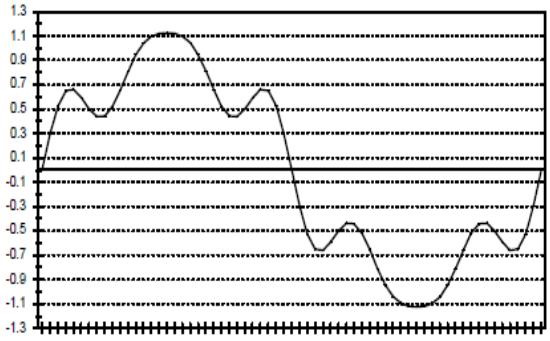

Figure.2 Fundamental with two harmonics

In order to be able to analyze complex signals that have many different frequencies present, a number of mathematical methods were developed. One of the more popular is called the Fourier Transform. However, duplicating the mathematical steps required in a microprocessor or computer-based instrument is quite difficult. So more compatible processes, called the FFT for Fast Fourier transform, or DFT for Discrete Fourier Transform, are used.

These methods only work properly if the signal is composed of only the fundamental and harmonic frequencies in a certain frequency range (called the Nyquist frequency, which is one-half of the sampling frequency). The frequency values must not change during the measurement period. Failure of these rules to be

maintained can result in mis-information. For example, if a voltage waveform is comprised of 60 Hz and 200 Hz signals, the FFT cannot directly see the 200 Hz. It only knows 60, 120, 180, 240... Which are often called “bins”. The result would be that the energy of the 200 Hz signal would appear partially in the 180Hz bin, and partially in the 240 Hz bin. An FFT-based processer could show a voltage value of 115V at 60 Hz, 18 V at the 3rd harmonic, and 12 V at the 4th harmonic, when it really should have been 30 V at 200 Hz.

These in-between frequencies are called “inter harmonics”. There is also a special category of inter harmonics, which are frequency values less than the fundamental frequency value, called sub-harmonics. For example, the process of melting metal in an electric arc furnace can result large currents that are comprised of the fundamental , inter harmonic, and sub harmonic frequencies being drawn from the electric power grid. These levels can be quite high during the melt-down phase, and usually effect the voltage waveform.

IV. INVERTER

An inverter is an electrical device that converts direct current (DC) to alternating current (AC) the converted AC can be at any required voltage and frequency with the use of appropriate transformers, switching, and control circuits. Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utilityhigh voltage direct current applications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries. The electrical inverter is a high power electronic oscillator. It is so named because early mechanical AC to DC converterswas made to work in reverse, and thus was "inverted", to convert DC to AC.

Cascaded H-Bridges inverter

A single phase structure of an m-level cascaded inverter is illustrated in Figure 4.1. Each separate DC source (SDCS) is connected to a single phase full bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the DC source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The AC outputs of each of the different full bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate DC sources. An example phase voltage waveform for an 11 level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 4.2. The phase voltage

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5} \ldots (4.1)$$

For a stepped waveform such as the one depicted in Figure 4.2 with s steps, the Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_n [\cos(n\theta_1) + \cos(n\theta_2) + \cdots + \cos(n\theta_s)]\frac{\sin(n\omega t)}{n}, \quad where\ n = 1,3,5,7 \ldots$$

… (4.2)

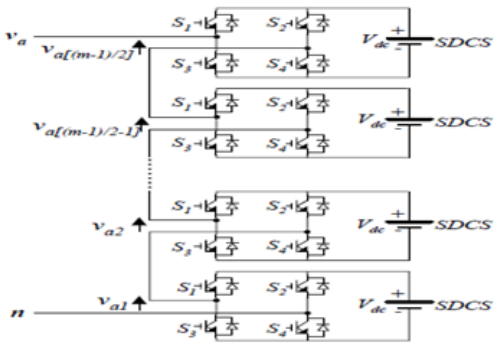

Fig.3.Single-phase structure of a multilevel cascaded H-bridges inverter

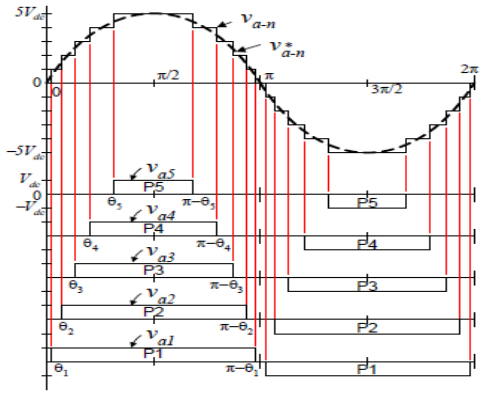

Fig.4 Output phase voltage waveform of an 11 level cascade inverter with 5 separate dc sources.

V. PROJECT DISCRIPTION AND CONTROL DESIGN

CONDITIONS OF PHASE SHIFTED SYNCHRONOUS PWM FOR CHBMLI

The unipolar PWM technique is used for generating gate pulses for each H-Bridge. The H-Bridge pole voltage varies between 0 to +Vdc when the sign of the voltage reference is positive and varies between 0 to -Vdc when the sign of thevoltage reference is negative (where Vdc is the input DC link voltage of the H-Bridge). For implementing unipolar PWM in an H-Bridge1 (Fig.1.(a)), a positive voltage reference R1 is used to generate gate pulses for switches S11 and S12 of leg1 and a negative voltage reference R2 is used to generate gate pulses for switches S13 and S14 of leg2. A common carrier CHB1 is used for both the legs in order to generate gate pulses. The resultant output pole voltage VHB1 is the algebraic summation of individual leg voltages i.e. VHB1=VHBL1-VHBL2. A. Verification of Synchronization The synchronization between voltage reference and fundamental component of inverter output pole voltage can be maintained if the synchronous carrier frequency is n (n being any integer) times the voltage reference frequency. By maintaining the above condition the intersection points between the carrier and the voltage reference (i.e. in a fundamental cycle of the voltage reference) repeat after 2πrad (i.e. the next consecutive fundamental cycle of the voltage reference), hence synchronization is maintained.

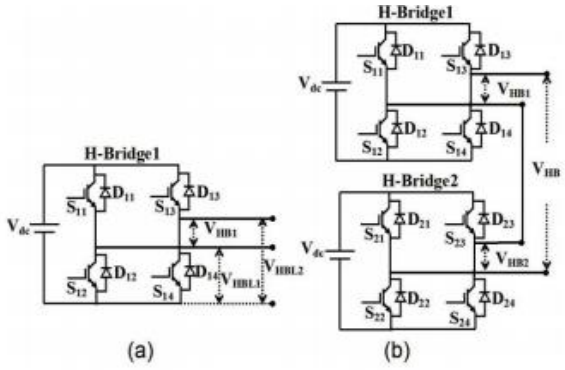

Fig. 1. (a) Single H-Bridge ; (b) Double cascaded H-Bridges.

Fig.5 H-bridge circuit

Verification of Three Phase Symmetry & Half Wave Symmetry

With synchronous carriers having 3n times the fundamental frequency (n being any integer) being used for the PSPWM technique, three phase symmetry is always maintained among individual H-Bridge output pole voltage waveforms. Also, from Fig.2.(a) it can be observed that, for an odd integer ratio between the carrier and fundamental frequency, the region from πrad to 2πrad is equivalent to a mirror image of the region from 0rad to πrad with respect to xaxis(θ). Hence, the intersection points C1 to C6 are the mirror images of points from C7 to C12 respectively. In fact, for an odd integer ratio, individual pole voltages of both the legs (VHBL1 and VHBL2) of one H-bridge maintain half wave symmetry and hence their difference also maintains half wave symmetry. If the ratio is even then, individual pole voltages of both the legs (VHBL1 and VHBL2) do not maintain half wave symmetry. But the waveform of VHBL1 from 0rad to πrad is an exact replica of VHBL2 from πrad to 2πrad and vice versa. Hence, their difference (i.e. VHB1= VHBL1-VHBL2) maintainshalf wave symmetry. Hence, for an H-bridge, the half wave symmetry is satisfied for any carrier having its frequency equal to integer (odd/even) multiple of the fundamental frequency. Therefore, it can be concluded that the inverter pole voltage

waveform maintains three phase and half wave symmetry for carriers having 3n times the fundamental frequency (n being any odd/even integer). It is therefore only necessary to determine the conditions for quarter wave symmetry in the inverter output pole voltage waveform.

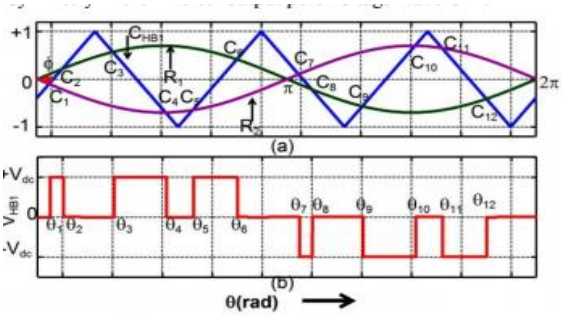

Fig.6. Verification of Three Phase Symmetry & Half Wave Symmetry

Determination of conditions for Quarter Wave Symmetry

1) Single H-Bridge The quarter wave symmetry among pole voltage waveform of an H-Bridge (Fig.6.1.(a)) can be maintained, if the positive zero crossing of the voltage reference coincides with the positive zero crossing of the carrier. The normalized fundamental voltage references are sine waves with their amplitude less than or equal to one. The carriers are triangular waves with the magnitude of their positive and negative peak equal to one. Positive zero crossing means, the instantaneous values of these periodic waveforms have completed their negative half cycles and become zero before entering the positive half cycle.

The carrier can be of two types. They are: - (i) In phase carrier (positive zero crossing of positive voltage reference coincides with the positive zero crossing of the carrier) (ii) Out of phase carrier (positive zero crossing of the positive voltage reference coincides with the negative zero crossing of the carrier). For carrier frequency being an odd multiple of the fundamental frequency, individual pole voltages of both the legs (VHBL1 and VHBL2) maintain quarter wave symmetry ensuring quarter wave symmetry of the bridge output voltage VHB1. For carrier frequency being an even multiple of the fundamental frequency, individual pole voltages of both the legs (VHBL1 and VHBL2) do not maintain quarter wave symmetry. But their difference VHB1= VHBL1- VHBL2 maintains quarter wave symmetry. If the carrier is phase delayed by π/2rad (where 2πrad is one carrier period), then the reverse phenomenon happens.

Now, for carrier frequency being an even multiple of the fundamental frequency, individual pole voltages of both the legs (VHBL1 and VHBL2) maintain quarter wave symmetry. Whereas, for carrier frequency being an odd multiple of the fundamental frequency, individual pole voltages of both the legs (VHBL1 and VHBL2) do not maintain quarter wave symmetry. But their difference VHB1= VHBL1- VHBL2 maintains quarter wave symmetry. This can also be derived mathematically as shown in the following discussion. As a specific case, the carrier frequency is taken to be three times the fundamental frequency. From Fig. 2, for maintaining quarter wave symmetry of the pole voltage waveform VHB1, the constraint to be satisfied among voltage reference and carrier intersection points C1 to C6 is given by (1). 7−−=θπθll for l = 1, 2 and 3 (1) For l=1, the values of θ1 and θ6, at points C1 and C6 can be found out by equating the equations of voltage reference‘s and the carrier‘s. A small step is shown below to determine the equations of voltage references and carriers at points C1 and C6 with the help of the equations (2), (3), (4) and (5). Fig.3 shows the enlarged view of voltage references R1 and R2 along with carrier CHB1. The point C1 (whose trace is θ1 along x-axis (θ)) is the intersection point between voltage reference R2 and line AB which is one part of the carrier CHB1. The equation of the voltage reference at C1 can be written as (2). 1 1 −=mz sinθ (2)

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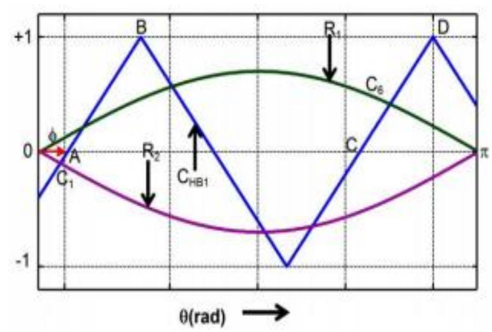

Fig.7. Determination of conditions for Quarter Wave Symmetry

The co-ordinates of the points A and B are (Φ, 0) and (Φ+π/6, 1) respectively. Hence, the equation of the line AB at point C1 can be written as (3). ()ϕθπ ⎟⎠⎞⎜⎝⎛ − 1 = 1 6 z (3) Similarly, the point C6 is the intersection point between R1 and line CD (which is a portion of carrier CHB1). The equation of the voltage reference at C6 can be written as (4). 6 6 =mz sinθ (4)

The co-ordinates of the points C and D are (2π/3+Φ, 0) and (Φ+5π/6, 1) respectively. Hence, the equation of the line CD at point C6 can be written as (5). ⎟⎠⎞⎜⎝⎛ ⎟⎠⎞⎜⎝⎛=ϕπθπ 3 26 6 6 z (5) Where z1 & z6 = y-axis values at points C1 and C6 respectively m=modulation index of voltage references R1 and R2 From equations (2), (3), (4) and (5), the intersection angles θ1 and θ6 at points C1 and C6 can be found out by equating the equations of voltage references and carriers and can be written as (6) and (7) respectively. ()ϕθπθ ⎟⎠⎞⎜⎝⎛ 1 =− 1 6 msin (6) ⎟⎠⎞⎜⎝⎛ ⎟⎠⎞⎜⎝⎛=ϕπθπθ 3 26 msin 6 6 (7) Equation (7) can be modified as (8) by putting the constraint of quarter wave symmetry (2). ⎟⎠⎞⎜⎝⎛ ⎟⎠⎞⎜⎝⎛=ϕθππθ1 1 3 6 msin (8) By adding equations (6) and (8), the value of ϕ can be found as (9). rad 6 ϕ=π (9) From equation (9) it can be observed that, the quarter wave symmetry of the pole voltage waveform VHB1 can be maintained if the zero crossing of the carrier lags the voltage reference zero crossing by π/6rad. Equation (9) gives the value of Φ in terms of the fundamental period of the voltage reference. If the value of Φ is expressed in terms of carrier period, then Φ should be equal to π/2rad for p=3. In a similar way the conditions for quarter wave symmetry at the other intersection points can also be derived and all of them arrive at the same conclusion. Similarly, when the zero crossing of the carrier leads the voltage reference zero crossing by an angle Φ=π/2rad, quarter wave symmetry among pole voltage waveform VHB1 in a single H-Bridge can be maintained. Equation (9) shows the condition for quarter wave symmetry among pole voltage waveforms VHB1, when p=3. For carriers having frequency p=3n (where n=1, 3, 5, 7, 9,……,etc.) times the fundamental frequency and with their zero crossings lagging the fundamental voltage reference zero crossings by Φrad, the condition for quarter wave symmetry among pole voltage waveform VHB1 can be found by using (10)-(14). Here, for quarter wave symmetry, the constraint is given by (10). 16 −+−=θπθlln for l = 1, 2, ...3n (10) For l=1 ()ϕθπθ ⎟⎠⎞⎜⎝⎛ 1 =− 1 6 sin n m (11) ()⎭⎬⎫⎩⎨⎧ − ⎟⎠⎞⎜⎝⎛=ϕθππθ n nn m n n 3 6 13 sin 6 6 (12) By putting the constraint of quarter wave symmetry 6n −=θπθ 1 in (12), one gets ⎟⎠⎞⎜⎝⎛ ⎟⎠⎞⎜⎝⎛=ϕθππθ1 1 3 6 sin n n m (13) By adding (11) and (13), the value of ϕ can be found as (14). rad n ⎟⎠⎞⎜⎝⎛ ⎟⎠⎞⎜⎝⎛= 23 1 πϕ (14) Hence, by representing Φ in terms of carrier period, it can be concluded that, for maintaining quarter wave symmetry among pole voltage waveform VHB1, the zero crossing of the carrier should lag the zero crossing of the voltage reference by π/2 rad. In a similar way, conditions for quarter wave symmetry can be analytically derived for an even integer ratio of carrier and fundamental frequency with zero carrier phase shift, odd integer ratio with zero carrier phase shift and even integer ratio with π/2 rad phase shift. Therefore, the conditions for maintaining quarter wave symmetry among pole voltage waveform VHB1 in a single H-Bridge can be summarized as below:- I. The zero crossings of the voltage references should coincide with the zero crossings of the carrier. II. The zero crossings of the carrier should be placed at ±π/2 rad with respect to the zero crossings of the voltage references (where 2π rad denotes one carrier period). If we have only two H-Bridges per phase, then their individual carriers should be phase shifted from each other

by π/2rad. One carrier can satisfy condition I and the other carrier can satisfy condition II as described above. The output voltage of both the H-Bridges will maintain quarter wave symmetry and hence their sum will also maintain quarter wave symmetry. But, as the number of cascaded H-Bridges increases (more than two) it is not possible to place all the zero crossings of carriers at 0rad or ±π/2rad with respect to the zero crossings of voltage references, as the phase difference between (π/x rad for x≥2 number of cascaded H-bridges) zero crossings of the carriers decreases. For two cascaded HBridges, the next section deals with the conditions for maintaining quarter wave symmetry among resultant pole voltage VHB, where the zero crossings of the carriers are placed other than 0rad or ±π/2rad with respect to the voltage reference zero crossings. 2) Two Cascaded H-Bridges For two cascaded H-Bridges (Fig.1.(b)), it is also possible to maintain quarter wave symmetry among the resultant pole voltage waveform VHB, in spite of individual bridge voltage waveforms VHB1 and VHB2 not maintaining quarter wave symmetry. Two approaches are possible and pointed below. Both the approaches are analyzed in the coming sections.

Zero crossings of carriers CHB1 and CHB2 are placed on both sides of the zero crossing of carrier Cref1 (where Cref1 is a fictitious carrier whose zero crossings are in phase with the zero crossings of the voltage references R1 and R2). ¬ Zero crossings of carriers CHB1 and CHB2 are placed on both sides of the zero crossing of carrier Cref2 (where Cref2 is a fictitious carrier whose one positive or negative peak appears in the same instant as that of the zero crossings of the voltage references R1 and R2). In other words, it can be stated that Cref1 satisfies condition I and Cref2 satisfies condition II. The carriers CHB1 and CHB2 are used for generating gate pulses of H-Bridge1 and H-Bbridge2 respectively in a double cascaded H-Bridge (Fig.1.(b)). The voltage reference R1 is used for generating the gate pulses of S11, S12, S13 and S14. The gate pulses of S13, S14, S23 and S24 are generated by voltage reference R2. Fig.4 and Fig.5 show the voltage references, R1 and R2 along with carriers CHB1 and CHB2 with respect to the fictitious carriers Cref1 and Cref2 respectively. a) Approach I Fig.4 shows the case, where the zero crossing of carrier CHB1 leads the zero crossing of fictitious carrier Cref1 by Φ1rad, whereas the zero crossing of carrier CHB2 lags the zero crossing of Cref1 by Φ2rad for p=3. Fig.4.(b) shows that the resultant pole voltage VHB, does not maintain quarter wave symmetry. In order to show the intersection points and intersection angles, only the half cycle of each waveform is shown in Fig.4. For maintaining quarter wave symmetry of the resulting pole voltage VHB, the condition to be satisfied among voltage reference and carrier intersection points C1 to C12 is given by (15). 13−−=θπθll for l=1, 2, 3, 4, 5 and 6 (15) For l=1, the values of θ1 and θ12, at points C1 and C12 can be found out by equating the equations of voltage references and carriers and can be written as (16) and (17) respectively. 1 () 1 2 6 msinθθϕπ⌒−=−| |∪ (16) 12 () 12 1 6 msinθθπϕπ⌒−=−−+| |∪ (17) Equation (17) can be modified as (18) by putting the condition of quarter wave symmetry (15). 1 () 1 1 6 msinθϕθπ⌒=−| |∪ (18) By adding (16) and (18), the condition for quarter wave symmetry can be found out as (19). =ϕϕ21 (19) Fig. 4. (a) References R1 and R2 and Carriers CHB1 and CHB2 when Cref1 is in phase with voltage references (p=3); (b)VHB. From (19) it can be observed that, the quarter wave symmetry among resultant pole voltage waveform VHB can be maintained if Φ1 =Φ2, i.e. the zero crossings of carriers CHB1 and CHB2 are placed equidistantly from the zero crossings of carrier Cref1. In a similar way the conditions for quarter wave symmetry at the other intersection points can also be derived and each pair of intersection points will result in the condition of (19). Equation (19) shows the condition for quarter wave symmetry among pole voltage waveform VHB, when p=3. For carriers having frequency p=3n (where n=1, 2, 3, 4, 5, 6, 7, 8, 9, 10,….,etc.) times the fundamental frequency and with their zero crossings lagging and leading the zero crossing of C ref1 by Φ1rad and Φ2rad respectively, the condition for quarter wave symmetry among resultant pole voltage waveform VHB can be found by using the above

approaches (equations (16)-(19)) and the final conclusion is same as (19). b) Approach II In the second approach (Fig.5), the zero crossing of carrier CHB1 leads the zero crossing of carrier Cref2 by Φ1rad, whereas the zero crossing of carrier CHB2 lags the zero crossing of carrier Cref2 by Φ2rad for p=3. Fig.5.(b) shows that the resultant pole voltage VHB does not maintain quarter wave symmetry. For maintaining quarter wave symmetry among resultant pole voltage waveform VHB, the condition to be satisfied among voltage reference and carrier intersection points C1 to C12 is given by (20). 13−−=θπθll for l=1, 2, 3, 4, 5 and 6 (20) For l=1, the values of θ1 and θ12, at points C1 and C12 can be found out by equating the equations of voltage references and carriers and can be written as (21) and (22) respectively. ⎩⎨⎧+−⎩⎨⎧ 1 =− 11 6 6 sin ϕπθπ m θ (21) ⎩⎨⎧−−⎩⎨⎧ 12 = 12 2 6 56 sin ϕπθπ m θ (22)

VI. SIMULATION RESULTS:

A. By Using Phase Shift PWM Technique

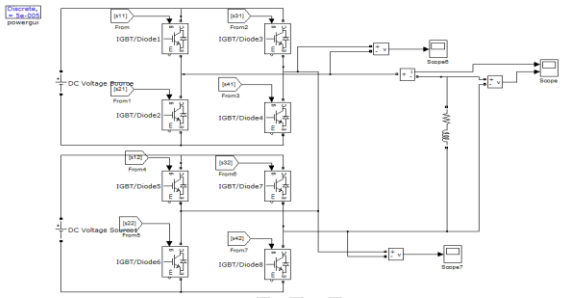

Fig.8.Five level inverter simulation circuit

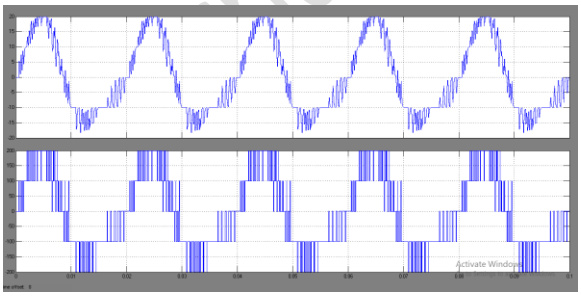

Fig.9.Five level inverter output waveform

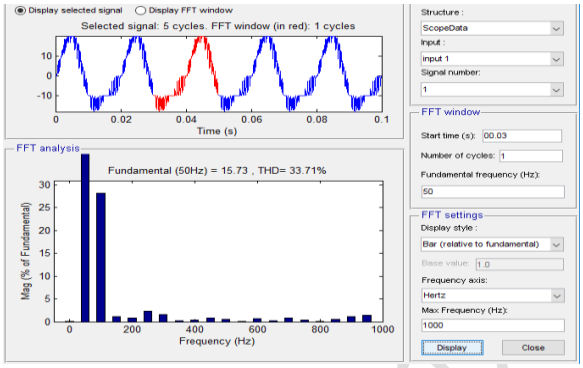

Fig.10.THD of Five level inverter using phase shift PWM

B. By Using PWM Technique

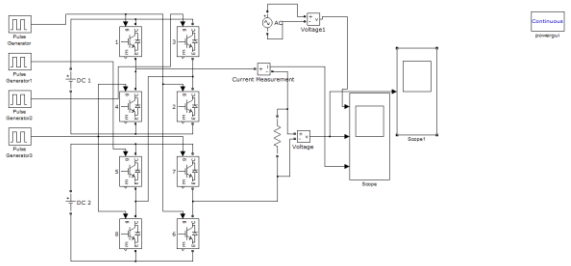

Fig11. Simulation circuit of five level inverter using PWM technique

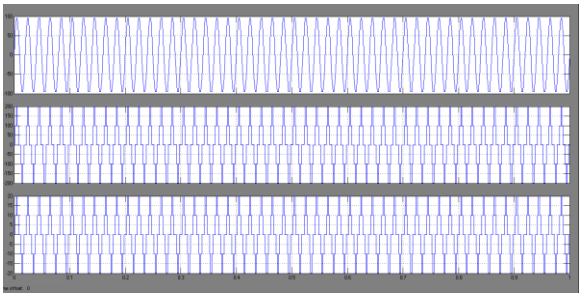

Fig .12.Simulation output of five level inverter

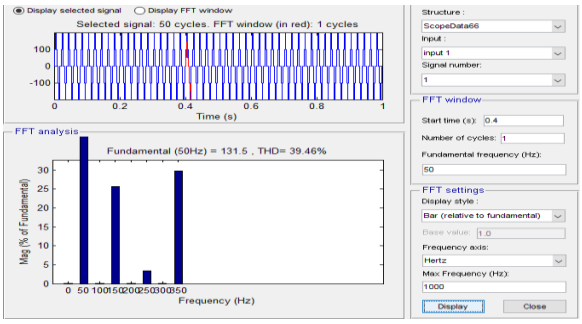

Fig.13.THD of Five level inverter using PWM

VII. CONCLUSION

This paper shows analytically the possible positions of zero crossings of the carriers with respect to the zero crossings of voltage references for the CHBMLIs using the PSPWM technique for maintaining three phase symmetry, half wave symmetry and quarter wave symmetry. Three phase and half wave symmetries are maintained among the H-Bridge pole voltage waveforms for any position of zero crossing of carrier with respect to the zero crossing of the voltage references; as long as carrier frequency is 3n time the fundamental frequency with n being any integer (even/odd). But the positions of zero crossings of the carriers with respect to the zero crossings of voltage references are important for maintaining quarter wave symmetry among the pole voltage waveforms. This is analytically studied in this paper for single and two cascaded H-Bridges and generalized for x number of cascaded HBridges. The study is experimentally verified with the help of a three phase five level CHBMLI laboratory prototype and the results are presented.

In this project the simulation results of five level using phase shift PWM technique gives better results compared to that of the normal PWM technique.

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