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DUAL USE OF POWER LINES FOR DESIGN-FOR-TESTABILITY—A CMOS RECEIVER DESIGN

[#1]RASAKATLA SWETHA, M.Tech Student,
[#2]P.AJAY KUMAR, Assistant Professor,
Dept of ECE,
VAAGESWARI COLLEGE OF ENGINEERING, KARIMNAGAR, TELANGANA.

Abstract— As the circuit complexity increases, the number of internal nodes increases proportionally, and individual internal nodes are less accessible due to the limited number of available I/O pins. To address the problem, we proposed power line communications (PLCs) at the IC level, specifically the dual use of power pins and power distribution networks for application/ observation of test data as well as delivery of power. A PLC receiver presented in this paper intends to demonstrate the proof of concept, specifically the transmission of data through power lines. The main design objective of the proposed PLC receiver is the robust operation under variations and droops of the supply voltage rather than high data speed. The PLC receiver is designed and fabricated in CMOS 0.18-µm technology under a supply voltage of 1.8 V. The measurement results show that the receiver can tolerate a voltage drop of up to 0.423 V for a data rate of 10 Mb/s. The power dissipation of the receiver is 3.26 mW under 1.8 V supply, and the core area of the receiver is 74.9 µm × 72.2 µm.

Keywords: Power Line Communication (PLC), power efficient CMOS PLC receiver, power consumption, stacking method.

1. INTRODUCTION

Today's VLSI technology is advancing in such a way that the designers can incorporate a large number of functions inside a chip. Microprocessors are one of the best examples for this. Day by day the size of ICs reduces and the operations it can perform are increasing. So many challenges still exist such as, the need of proper provision for the thermally generated heat removal, the number of the input output pins that an IC needs, proper power supply injection etc., due to which there exists limits on incorporating functions inside ICs. Also routing inside the IC too has a major role in it. There should also be the provisions in ICs like sensors to detect what is happening inside each and every point and if anything happens wrongly, the normal state have to be recovered. Even though the increase in system complexity is an advantage in the sense that the size of ICs can be reduced, with that there should be new inventions for proper data passage inside the same. The power line communication aspect presented in this paper is one of such methods. In power line communication, it efficiently uses the power distribution networks inside ICs since they are the only components that reach each and every node. So if there have a provision to pass the test data, which are used for fault diagnosis, scan design etc. to whichever areas we need to apply the test that will be an attractive way of communication in ICs, So that the routing overhead inside the ICs to pass these testing data can be intelligently avoided. So in PLC, the power distribution networks are used for power delivery and also data communication. The test data are superimposed on the power signal and are transmitted through the power distribution networks of ICs rather than the separately allotted routing paths. Also the number of power pins can be reduced since there is no need to carry the test data through the input pins. Of course, adopting such a power line communication always has to overcome the extreme noise level at the power lines. So there should be effective methods to overcome the same. Essentially there is the need of receivers at each and every node to extract these data signals efficiently from the power lines. Many variants of the same already exist, but a power efficient design is not yet met. Why the receiver should be power efficient is because, otherwise if each unit of receiver consumes such huge power, the overall power consumption of the

entire chip will increase by a large value, which is hard to afford.

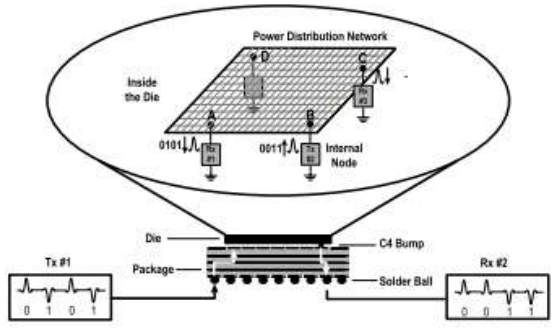

Fig. 1. Proposed conceptual PLC system in an IC environment.

2. PRELIMINARIES

A. Operating Environment

PLC at the IC level faces a different set of technical challenges from that of the traditional PLC over such applications as power lines of residential buildings and long distance transmission lines. First, power lines of a chip are very noisy due to factors, such as cyclo stationary background noise, resulting from switching synchronous to the main and sub clocks, strong deterministic components at frequencies corresponding to those clocks, and low-frequency (20–100 MHz) noise resulting from the resonances of the PDN . Resultantly, the signal-to-noise ratio (SNR) of PLC at the IC level is low, which would require special treatments. One rudimentary approach is to increase the signal level of the data superimposed on the supply voltage. However, the superimposed data signal should not affect the integrity of the supply voltage, and the variations of the supply voltage for ICs should remain less than ±10% . Second, the supply voltage varies and droops in space. It is caused by the factors such as nonideal voltage regulators, IR drop, and varying power consumption of underlying blocks. Bernstein et al. eported that the supply voltage droop ranges from 3% to 15% of the supply voltage across the chip area. Therefore, it is necessary for a PLC receiver in an IC to overcome large voltage variations and droops. Third, a PDN is heavily damped with the decoupling capacitors connected to power lines. It intends to reduce the slew rate of current variations by locally supplying or sinking currents and suppress voltage and current ringings at power lines. Consequently, a PDN behaves as a low-pass filter, which prevents high-frequency data signals from propagating through the PDN. The problem is aggravated when a data signal travels through the power and ground planes of the package shown in Fig. 1.

B. Previous Works

To the best of our knowledge, we are the only group who reported the works on PLC in ICs. Our group proposed PLC in ICs to reduce the pin count, size, and hence the cost of a chip initially and later to increase the channel capacity for the multiple parallel scan design. To follow up the proposal, we investigated several relevant topics for PLC in ICs, and reviewed them briefly as follows. We measured the propagation loss from a core power supply pin to an on-chip node of a PDN of a cold Pentium 4 die (65 nm version). The largest passband was observed ∼2 GHz over a 200-MHz band, and the path loss increases above 40 dB beyond 2.5 GHz. Other measurements were carried out on three different samples of cold 45-nm Core 2 Duo processors and two randomly picked locations on the PDNs. The averaged transfer function shows narrow sporadic passbands, where about 5% ∼ 7% of the input signal passes through the PD N. We observed that there is little correlation between the passbands of the 65 nm Pentium 4 and that for the 45-nm Core 2 Duo processors. We suggested the use of ultra wideband (UWB) and direct-sequence code division multiple access (DS-CDMA) communication technologies to circumvent the blocking of data signals in low frequencies at packages and PDNs and increase the SNR. Compared with the traditional narrow-band communication systems, UWB signaling has several advantages, such as high data rate, low average power, and simple RF circuitry. Shannon's theorem states that the channel capacity is given as $B \times \log2(1 + SNR)$, where B is the bandwidth. As the bandwidth is much larger (on the order of several gigahertz) for UWB than a narrow-band signal, the SNR can be much smaller for UWB to achieve the same data rate. The DS-CDMA technology assigns a codeword to each bit of information called spreading, and orthogonal code words are assigned to different users or power pins for the PLC in ICs to support multiple channels. The spreading operation represents 1 bit of data as a series of binary pulses spread over a

codeword, which increases the pulse repetition frequency. The benefit of spreading is the processing gain, which is 10 × log (spreading_ factor) in decibel. For example, the spreading factor for 4-bit code words is 4, which yields a processing gain of 6 dB, or increases the SNR by 6 dB. We also investigated the modeling of I/O pads and PDNs, and estimated the performance of the proposed PLC systems. We designed several versions of PLC receivers and transmitters for the proposed PLC system in ICs. The first PLC receiver was designed in TSMC 0.18-µm CMOS process. Transient simulations indicate that the PLC receiver can recover data from impulses with the amplitude of ~90 mV and the period of 300 ps superimposed on the supply voltage of 1.8 V. The pulse repetition rate of the impulses is 1 GHz. A PLC receiver based on a correlator is reported , and its improved version is reported. Another PLC receiver based on a differential Schmitt trigger is presented. Design of a transmitter for the proposed system is reported. All the above PLC receivers and transmitters report only simulation results. This paper presents a PLC receiver whose main design objective is the robust operation under voltage variations and droops of the supply voltage. The PLC receiver intends to demonstrate the feasibility of a robust receiver as a proof of concept. Therefore, regular pulses (rather than UWB) with a low repetition frequency of 10 Mb/s and a simple amplitude shift keying (ASK) are adopted for the receiver. The receiver was designed and fabricated in CMOS 0.18-µm technology with a supply voltage of 1.8 V.

C. Amplitude Shift Keying

Various types of digital modulation schemes, such as ASK, phase-shift keying, and frequency-shift keying, are possible for PLC at the IC level. A major requirement for the PLC in ICs is small area for on-chip receivers and transmitters, while high data rates are not critical for applications, such as scan design, system debugging, and fault diagnosis. The proposed PLC receiver adopts binary ASK, in which a signal level higher than VDD + VTH represents logic 1 and a signal level lower than VDD + VTH logic 0, where VTH is a preset threshold voltage. A PLC receiver adopting the binary ASK is simple and easy to implement, which leads to low circuit complexity and, hence, small area. However, ASK is susceptible to noise and disturbances, which can be mitigated through the system design (such as adoption of UWB and DS-CDMA technologies) and the circuit design such as a differential Schmitt trigger adopted for the proposed PLC receiver.

3. PROPOSED LOW VOLTAGE CMOS SCHMITT TRIGGER FOR PLC RECEIVER

The Proposed Low Voltage CMOS Schmitt Trigger for PLC receiver designed in this paper under a supply voltage of 1V in CMOS 0.18-µm technology using Tanner EDA tool which consists three major building blocks, they are the level shifter, the signal extractor and the logic restorer. The block diagram of the Proposed Low Voltage CMOS Schmitt Trigger for PLC receiver is shown in fig.2. The test data is represented by Vdd(t) and the main power signal by VDD. So VDD+Vdd(t) represents the test data superimposed on the power lines. The input signal is the power line signal in which the test data is superimposed and it is supplied to each of the building blocks. The output of the level shifter is the input of the signal extractor and the output of it, which is a differential signal and is applied to the logic restorer. The detailed operation and design concepts of each of the building blocks are described below.

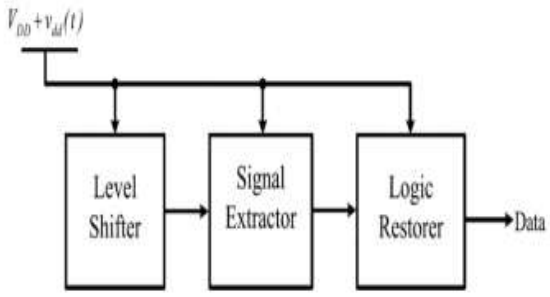

Fig.2 Proposed Low Voltage CMOS Schmitt Trigger for PLC Receiver

1. Level Shifter

The level shifter is the first stage in the proposed PLC receiver which is nothing but a common source amplifier having diode connected load and is shown in fig. 3. The purpose of this level shifter is to lower the DC level of the signal at the output so that, it will be easy for the subsequent blocks to process the data.

Also since the test data signals are superimposed on the power lines, this stage should have the ability to sense the variations that are present in the power lines and for that, its sensitivity to the input signal is purposefully lowered and the same to power signal is increased by lowering the characteristic called the Power Supply Rejection Ratio (PSRR). It can be expressed as in equation (1)

$$PSRR = Av/Avdd \quad (1)$$

Where is the small signal voltage gain of the circuit and is the small signal voltage gain from the power input to circuit's output. The small signal voltage gain can be expressed in terms of as

$$Av = -\ gm1/gm2 \quad (2)$$

The small signal voltage gain from the supply voltage can be expressed as

$$Avdd = \frac{r01}{(1/gm2)+r01} = 1 \quad (3)$$

Substituting (2) and (3) in (1) gives

$$PSRR = -\ gm1/gm2 \quad (4)$$

PSRR can be again represented in terms of device dimensions and overdrive voltage as

$$PSRR = \frac{\mu n\left(\frac{W}{L}\right)1\,(Vgs-Vth)1}{\mu p\left(\frac{W}{L}\right)2\,(Vgs-Vth)2} \quad (5)$$

Since we need a level shifter having a low PSRR, the equation (5) can be treated in two different ways. In order to reduce the PSRR, either we can reduce the device dimension of transistor M1 and can increase the same of M2. Also the overdrive voltage of M1 should be lowered and that of M2 should be made high compared to M1. These two concerns should be kept in mind while designing the level shifter stage for a smaller PSRR.

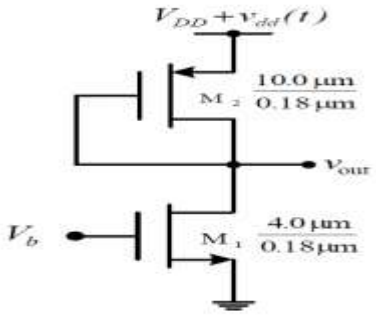

Fig. 3 Level Shifter

2. Signal Extractor

The signal extractor in the proposed design is a differential amplifier and is shown in Fig 4. The output of the level shifter is simultaneously fed to two input terminals of the differential amplifier, out of which a low pass filter is connected to one of the terminals. The low pass filter is used in this design to extract the DC value from the level shifter output. Since the differential amplifier has a property of rejecting the common mode signal, which is the DC signal in our design, is thus successfully eliminated. The use of the same has another advantage that it reduces the noise levels that are already present in the signals. The signal extractor of the proposed design is shown in fig. 4. The signal extractor converts the single ended output of the level shifter to a differential signal. In this proposed design we consider only signal output. This output is connected to the next block new logic restorer.

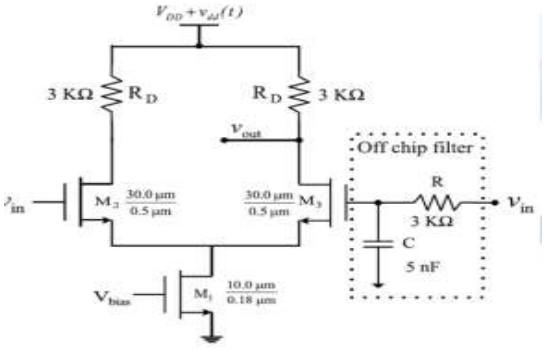

Fig. 4 Signal Extractor with Low Pass Filter

3. Logic Restorer

The logic restorer is the block which contributes to a great part in the noise immunity of the entire system.

It is a Low Voltage CMOS Schmitt Trigger with tunable hysteresis property. The main advantage of using this Schmitt trigger is that, it is excellent in handling the situations of extreme noise and disturbances. The Low Voltage CMOS Schmitt trigger based logic restore employed in the design is shown in fig. 5.

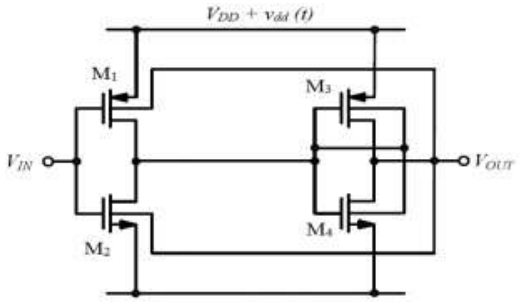

Fig. 5 Low voltage CMOS Schmitt Trigger based logic restorer

Schmitt trigger circuits are widely used for waveform shaping under noisy conditions in electronic circuits. In VLSI circuits, they are often used at the chip input side and as single-ended receivers in DRAMs. The hysteresis in a Schmitt trigger offers better noise margin and noise stable operation. With proliferation of portable devices, low power circuits are extremely desirable. In a recent work, a low power Schmitt trigger circuit design is reported for 3V operation. The cascade architecture used in this design limits lowering the operating voltage. In this paper, we report novel Schmitt trigger circuit designs in CMOS for operation at 1V and below using a dynamic body-bias method.

4. MEASUREMENT RESULTS

The proposed PLC receiver was designed and simulated in CMOS 0.18-µm technology with a supply voltage of 1.8 V. The measurement results followed are of the individual blocks and after all that of the final PLC receiver. Also the layouts of individual blocks are generated. The total power consumption of the PLC receiver is also calculated.

1. Level Shifter

The level shifter that is the common source amplifier with diode connected load is simulated with the proper bias voltage at the gates of the transistor M2.The timing response obtained is shown below in fig. 6

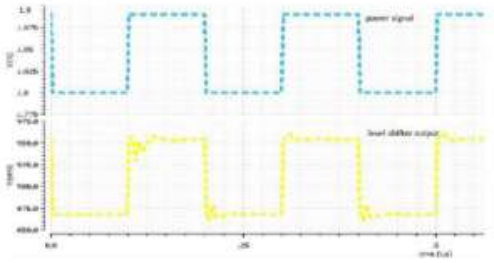

Fig. 6 Level Shifter Transient Response

The supply voltage is 1.8 V with the superposition of the data signal. The top waveform is the input signal superimposed on the supply voltage, in which the voltage level of 1.89 V represents logic 1 and 1.8 V represents logic 0. The bottom waveform shows the output signal of the level shifter. The output signal obtained is the level shifted version of the test data signal which is superimposed on the power lines. The layout of the level shifter is created with the help of cadence tool and is shown in fig. 7

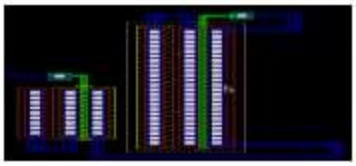

Fig. 7 Level Shifter Layout

2. Signal Extractor

The signal extractor is a differential amplifier having diode connected loads .The output of the level shifter is supplied directly to one of the differential amplifier input and the other input is fed from the output of the filter attached to the second input terminal. The filter extracts the DC value from the signal to reject the common mode signals that is the DC levels in the input. The transient response of the signal extractor is shown below in fig 8.

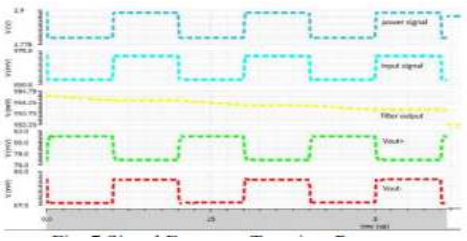

Fig. 8 Signal Extractor Transient Response

The top waveform is the input signal superimposed on the supply voltage. Second is the applied input signal which is followed by the output of the low pass filter and the outputs of the differential amplifier Vout+ and Vout-.The noise level that was incorporated at the output of the differential amplifier in the previous design is somewhat reduced in this new design and is clear from the transient responses. The layout of the signal extractor is created with the help of cadence tool and is shown in fig. 9

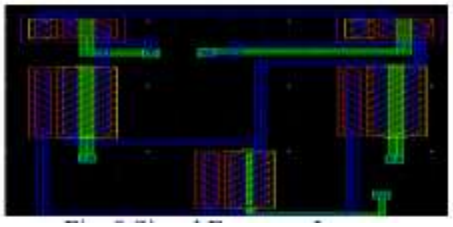

Fig. 9 Signal Extractor Layout

3. Logic Restorer

Logic restorer is a differential Schmitt trigger having the stacked model for the cross coupled inverter pair. The outputs of the differential amplifier are supplied to the inputs of the logic restorer. Clock signals of value 0-1.8 are fed and proper biasing signals are applied and finally simulated the entire circuit. The simulation results of the logic restorer are shown in fig. 10

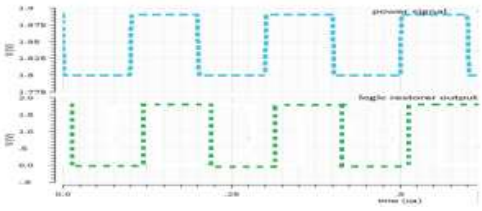

Fig. 10 Logic Restorer Transient Response

The data signal superimposed on the supply voltage of 1.8 V and the restoration of the logic values are shown in order. The layout of the logic restorer is created with the help of cadence tool and is shown in fig. 11

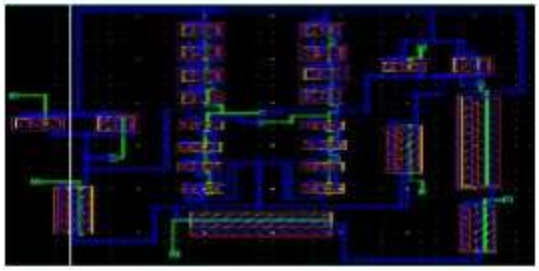

Fig. 11 Logic Restorer Layout

4. Power Efficient PLC Receiver

The three sub blocks of the PLC receiver are combined together after the verification of the individual blocks. The overall transient response is shown below in fig 12 .The power line superimposed data signal output of level shifter, signal extractor outputs, the clock signal and the final output of the PLC receiver are shown in order. It can be noticed that the designed CMOS PLC receiver can cleanly separate the original data signal of value 0 to 1.8 V from the power lines with the help of improved circuitry.

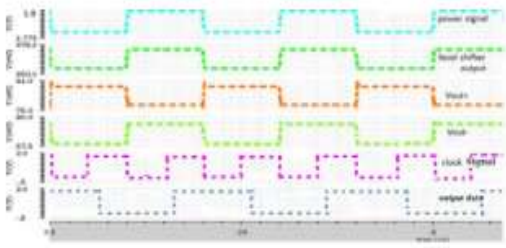

Fig. 12 PLC Receiver Transient Response

The work was mainly concentrated on a power efficient design, since power is one of the most important criterions in the VLSI design. The total power consumption of the PLC receiver is calculated with the help of the cadence tool and it is found to be about 1.228mWs, which is very small compared to the power consumption of previously implemented PLC receivers. Since these PLC receivers are required in large amounts in each ICs, the

achievement here is of great importance because, the power consumption of the entire IC can be reduced by a large amount. The power could be reduced in this paper by too less than half of the existing design.

5. CONCLUSION

A receiver for PLC at the IC level, which can be applicable to low data rate communications, such as scan design, system debugging, and fault diagnosis, was investigated in this paper. The proposed PLC system adopts a binary ASK modulation scheme, and the PLC receiver consists of three building blocks. The level shifter shifts the dc level of the data signal to a half of the supply voltage. The signal extractor, based on a differential amplifier, removes the dc voltage from the data signal with the aid of a low-pass filter, which mitigates supply voltage fluctuations and droops. The logic restorer, based on a differential Schmitt trigger, extracts logic values from the data signal while improving the noise immunity of the receiver. The PLC receiver was designed to demonstrate the feasibility of a robust receiver as a proof of concept and fabricated in CMOS 0.18-μm technology. The measurements show that the PLC receiver can tolerate a supply voltage drop of 0.423 V or 23.5%. The power dissipation for the receiver is 3.2 mW under 1.8 V supply. It requires a wide scope of research efforts to exploit the potential of the PLC in ICs fully. To point out a few, modeling of power pins, packages, and PDNs, channel characterization, modulation and multiple access schemes, SNR versus bit-error rates of a given system, design of PLC receivers and transmitters, and adverse impact of the data signals superimposed on power lines to the operation of digital circuits.

REFERENCES

[1] W. C. Chung and D. S. Ha, "A new approach for massive parallel scan design," in Proc. IEEE Int. Test Conf., Nov. 2005, pp. 1–10.

[2] L. T. Wang, C. E. Stroud, and N. A. Touba, System-on-Chip Test Architectures: Nanometer Design for Testability. San Mateo, CA, USA: Morgan Kaufmann, 2010.

[3] S. M. Saeed and O. Sinanoglu, "Design for testability support for launch and capture power reduction in launch-off-shift and launch-off-capture testing," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 22, no. 3, pp. 516–521, Mar. 2014.

[4] J. Rajendran, O. Sinanoglu, and R. Karri, "Regaining trust in VLSI design: Design-for-trust techniques," Proc. IEEE, vol. 102, no. 8, pp. 1266–1282, Aug. 2014.

[5] S.-J. Wang, Y.-S. Chen, and K. S.-M. Li, "Low-cost testing of TSVs in 3D stacks with pre-bond testable dies," in Proc. IEEE Int. Symp. VLSI Design, Autom., Test (VLSI-DAT), Apr. 2013, pp. 1–4.

[6] Jebreel M. Salem and Dong Sam Ha, "dual use of power lines for design for testability-A CMOS receiver design," IEEE Trans. Very Large Scale Integr. (VLSI), 2015

[7] F. Yuan,"Differential CMOS Schmitt trigger with tunable hysteresis," Analog Integ. Circuits Signal Process. vol. 62, no. 2, pp. 245–248, Feb. 2010.

[8] B. Razavi, Design of Analog CMOS Integrated Circuits. New York, NY, USA: McGraw-Hill, 2001.

[9] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, Analysis and Design of Analog Integrated Circuits, 5th ed. New York, NY, USA: Wiley, 2009.

[10] P. E. Allen and D. R. Holberg, CMOS Analog Circuit Design, 3rd ed. London, U.K.: Oxford Univ. Press, 2002

[11] Dual Use of Power Lines forDesign-for-Testability— A CMOS Receiver Design IEEE transactions on very large scale integration (vlsi) systems, vol. 24, no. 3, march 2016