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IMPLEMENTATION OF LOW POWER SEQUENTIAL CIRCUIT USING ADVANCED CLOCKED PAIR FLIP-FLOP

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ABSTRACT

The clock system consisting of clock distribution networks and sequential elements is most power consuming VLSI components. Reductions of flip flop, power consumption have a deep impact on the total power consumption. Since power consumption is a major bottleneck of system performance, the clock load should be reduced to reduce the power consumption. The clock distribution network distributes the clock signal from a common point to all the elements that need it. Since this function is vital to synchronous system, much attention has been given to the characteristics of these clock signal and the electrical networks used in their distribution. In synchronous system clock distribution networks consumes a large amount of total power because of high operation frequency of highest capacitance. An effective way to reduce capacity of clock load is by minimizing number of clocked transistor. In low swing differential capturing flip flop system clock distribution networks consumes a large amount of chip power and there exist a more number of clocked transistor. Hence by a novel approach, clocked paired shared flip flop is used to reduce the number of local clocked transistors.

I. INTRODUCTION

The versatile market continues growing. Notwithstanding the customary cell phone, advanced camera, and tablet PC, improvement of different sorts of wearable data gear or human services related hardware has recently flourished as of late. In those sorts of battery-working gear, decrease of intensity is an imperative issue, and interest for control decrease in LSI is expanding. In view of such foundation, different sorts of circuit system have us been proposed.

In LSI, for the most part the greater part of the power is dispersed in irregular rationale, of which half of the power is scattered by flip-flops (FFs). Amid the previous done years, a few low-control FFs have been hurried into improvement. Be that as it may, in genuine chip outline, the ordinary FF is as yet utilized regularly as a favored FF in light of its very much adjusted power, execution and cell region. The reason for this paper is to introduce an answer for accomplishes the majority of the objectives: control decrease with no corruption of timing execution and cell territory.

Given an outline that the areas of the cells have been resolved, the power devoured by timing can be decreased hide there by supplanting a few flip failures with multi bit flip lemon. Amid clock tree amalgamation, less number of flip lemon implies less number of clock sinks. Subsequently, the subsequent clock system would have littler power utilization and uses less steering asset. Furthermore, again littler flip lemon are supplanted by bigger multi bit flip failures; gadget varieties in the comparing circuit can be successfully lessened.

As CMOS innovation advances, the driving capacity of an inverter based clock cradle increments fundamentally. The driving ability of a clock cushion can be assessed by the quantity of least - estimated inverters that it can drive on a given rising or falling time. In view of this wonder, a few flip lemons can share a typical clock cushion to stay away from pointless power squander. The aggregate power utilization can be decreased in light of the fact that the two 1 bi flip - failures can have a similar clock support. Lessening the power utilization not exclusively can upgrade battery life yet additionally can stay away from the overheating issue, which would build the trouble of bundling or cooling .Therefore, the thought of intensity utilization in complex SOCs has turned into a major test to architects. Besides, in current VLSI plans, control devoured by timing has taken a noteworthy piece of the entire outline particularly for those outlines utilizing profoundly scaled CMOS advancements. Thus, several philosophies have been proposed to lessen the power utilization of timing.

In gadgets, a flip-tumble or hook is a circuit that has two stable states and can be utilized to store state data. A flip-tumble is a bi stable multi vibrator. The circuit can be rolled out to improvement state by signals connected to at least one control inputs and will have a couple of yields. It is the fundamental stockpiling component in successive rationale. Flip-tumbles and hooks are a major building square of computerized hardware frameworks utilized in PCs, correspondences, and numerous different sorts of frameworks.

Flip-flounders and locks are utilized as information stockpiling components. Such information stockpiling can be utilized for capacity of state, and such a circuit is depicted as consecutive rationale. At the point when utilized in a limited state machine, the yield and next state depend on its present contribution, as well as on its present state (and consequently, past information sources). It can likewise be utilized for tallying of heartbeats, and for synchronizing fluidly coordinated info signs to some reference timing signal.

Flip-failures can be either basic (straightforward or hay) or timed (synchronous or edge-activated). In spite of the fact that the term flip-slump has generally alluded blandly to both straightforward and timed circuits, in current utilization usually to hold the term flip-tumble only to examine timed circuits; the basic ones are normally called latches[1][2]

Utilizing this phrasing, a lock is level-touchy, while a flip-slump is edge-delicate. That is, the point at which a hook is empowered it winds up straightforward, while a flip tumbles yield us changes on a solitary kind (positive going or negative going) of clock edge. Flip-lemon can be either basic (straightforward or non-concurring) or timed (synchronous); the straightforward ones are usually called locks. The word hook is primarily utilized for capacity components, while timed gadgets are depicted as flip-flops.

Straightforward flip-lemon can be worked around a couple of cross-coupled upsetting components: vacuum tubes, bipolar transistors, field impact transistors, inverters, and modifying rationale entryways have all been utilized in down to earth circuits. Timed gadgets are uniquely intended for synchronous frameworks; such gadgets disregard their contributions with the exception of at the progress of a committed clock flag (known as timing, beating or stroking). Timing makes the flip-tumble either change or holds its yield flag in view of the estimations of the information signals at the progress. Some flip-flops change yield on the rising edge of the clock, others on the falling edge.

Since the rudimentary intensifying stages are transforming, two phases can be associated in progression (as a course) to shape the required non-reversing intensifier. In this arrangement, every enhancer might be considered as a functioning altering criticism organizes for the other modifying speaker. In this manner the two phases are associated in a non-altering circle in spite of the fact that the circuit outline is normally drawn as a symmetric cross-coupled combine (both the illustrations are at first presented in the Eccles– ordain patent).

1.1 FLIP FLOP TYPES:

Flip-failures can be separated into regular kinds: the SR ("set-reset"), D ("information" or "deferral" T ("flip"), and K composes are the normal ones. The conduct of a specific sort can be depicted by what is named the trademark condition, which determines the "following" (i.e., after the following clock beat) yield, next as far as the information signal(s) as well as the present yield.

II. EXISTING SYSTEM

2.1 BACKGROUND

In this we break down issues on beforehand revealed commonplace low-control FFs with correlation with a regular FF appeared in Fig. 1.

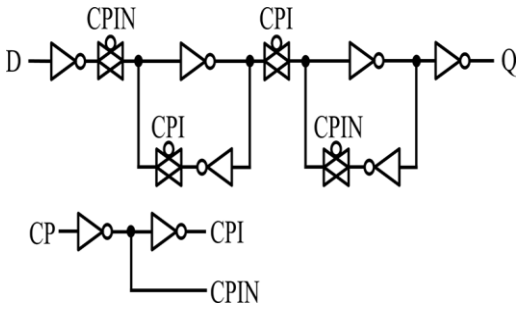

Fig.1.Conventional transmission-gate flip-flop (TGFF).

2.2A reduced clock-swing flip-flop (RCSFF) for 63% power reduction

Through RCSFF which can decrease the timing framework intensity of a VLSI down to 1/3 contrasted with the customary FF. The territory and the deferral of the RCSFF can likewise be decreased by a factor of around 20%

Underneath Figure indicates circuit outlines of the RCSFF and the traditional F/F. The RCSFF is made out of a present hook sense enhancer and cross-coupled NAND entryways which go about as a slave latch2'3. The striking element of the RCSFF is to acknowledge a lessened voltage swing clock. The voltage swing, Vick, can be as low as IV. By bringing down the clock swing, the intensity of the clock appropriation arrange is diminished as corresponding to either Vick or Vick , relying upon the clock driver design. At the point when a clock driver Type an is utilized, control change is corresponding to Vick, whale let 1s Vick if Type B driver is utilized. Sort An is anything but difficult to execute yet less productive Type B needs either an outer Vclk supply or a DC-DC converter. us three MOSFET's, Pl, P2 and NI are timed, which is valuable to diminish capacitance of a clock system, P1 and P2 can be little since they may recharge gradually while the clock is low. The issue of the RCSFF is that when a clock is high to Vclk, P1 and P2 don't turn off totally, leaving release current moving through either P 1 or P2. The power utilization by this Iclk current ends up being admissible for a few cases (see next segment), additionally control change is conceivable by lessening the release current One path is to apply back entryway predisposition to P 1 and P2 and increment the limit voltage,

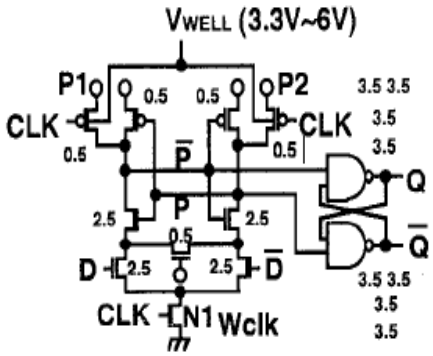

Fig RCSFF 2. Voltage swing of CLK is reduced to Vclk

The other path is to build the Vth of P 1 and P2 by particle embed, which needs process adjustment and is generally restrictive. Hence this case has not been considered here. At the point when the clock is to be ceased, it ought to be halted at vs. then there is no release current. A Low-Power Half-Swing Clocking Scheme for Flip-Flop with Complementary Gate and Source Drive A half-swing timing plan with an integral door and source drive is proposed for a CMOS flip-slump to lessen the power utilization of the clock framework by 43%, while keeping the flip-tumble defer time the same as that of the customary full-swing timing plan. The defer time of the former half phase of a flip-flounder utilizing this plan is not as much as half of that utilizing the past half-swing timing plan.

This sort of circuit is extremely powerful to increase little swing signals, so is by and large utilized in yield of memory circuits. In this FF, be that as it may, the impact of intensity reduction goes down in the state of lower information action, in light of the fact that these sorts of circuits have pre-charge task in each clock-low state. Besides, in the event that we utilize decreased clock swing, a customized clock generator and an additional predisposition circuit are essential.

1. A 200 MH 13 mm2 2-D DCT microcell utilizing sense-intensifying pipeline flip-flounder conspire

The two-dimensional discrete cosine change (2D DCT) has been generally perceived as a key handling unit for picture information pressure/decompression. In this paper, the usage of a 200 MH 13.3 mm2 8×8 2-D DCT full scale cell equipped for HDTV rates, in view of an immediate acknowledgment of the DCT, and utilizing circulated number juggling is exhibited. The full scale cell, created utilizing 0.8 am base-lead CMOS innovation and 0.5 am MOSFET's, plays out the DCT preparing with 1 test (pixel)- per-clock throughput. The quick speed and little one are accomplished by a novel sense-intensifying pipeline flip-tumble (SA-F/F) circuit method in blend with mom's differential rationale. The SA-F/F, a class of defer flip-flops, can be utilized as a differential synchronous sense-intensifier, and can open up double rail contributions with swings lower than 100 mV. A 1.6 ns 20 bit convey skip snake utilized in the DCT large scale cell, which was composed by a similar plan, is additionally portrayed. The viper is half quicker and 30% littler than an ordinary CMOS convey look forward snake, which lessens the large

scale cell measure by 15% contrasted with a regular CMOS usage.

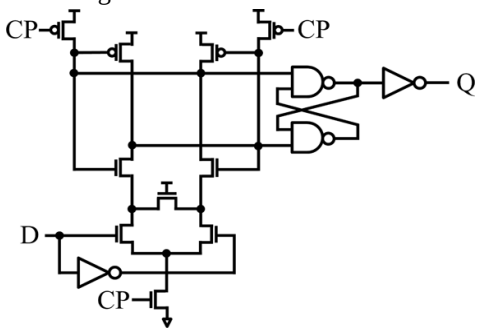

Fig. 3. Differential sense-enhancer flip-slump (Daffy).

Fig. 3 demonstrates a circuit of contingent timing composes FF (CCFF) [4]– [6]. This circuit is accomplished from an utilitarian perspective. The circuit screens input information change in each clock cycle and cripples the task of inside clock whenever input information are not changed. By this task, control is diminished when input information are not changed. However, lamentably, its cell territory turns out to be twofold that of the traditional circuit appeared in Fig. 1. What's more, essentially because of this see issue, it turns out to be difficult to utilize if the rationale territory is generally extensive in the chip.

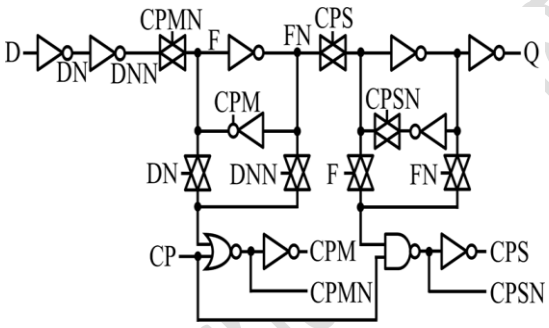

Fig.4.Conditional-locking flip-flop (CCFF)

Fig. 4 demonstrates the circuit of cross-charge control FF (XCFF) [7]. The element of this circuit is to drive yield transistors sep-irately keeping in mind the end goal to decrease charged and released door capacitance. Be that as it may, in real activity, a portion of the inward hubs are pre-set with check motion on account of information is high, and this task disperses additional capacity to charge and release interior hubs. Therefore, the impact of intensity decrease will diminish. Circuits including pre-set task have a similar issue [8].

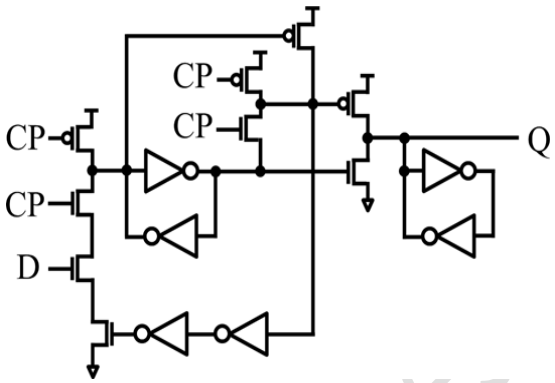

Fig.5. Cross-charge control flip-flop (XCFF)

The versatile coupling composes FF (ACFF) [9], appeared in Fig. 3.5, and depends on a 6-transistor memory cell. In this circuit, rather than the ordinarily utilized twofold channel transmission-entryway, a solitary channel transmission-door with extra powerful circuit has been utilized for the information line keeping in mind the end goal to lessen clock-related transistor check. Be that as it may, in this circuit, delay is effectively influenced by input clock slew variety on the grounds that diverse sorts of single-channel transmission-entryways are utilized in similar information line and associated with a similar clock flag. Also, attributes of single-channel transmission-entryway circuits and dynamic circuits are firmly influenced by process variety. In this way, their improvement is moderately troublesome, and execution debasement crosswise over different process corners is a worry.

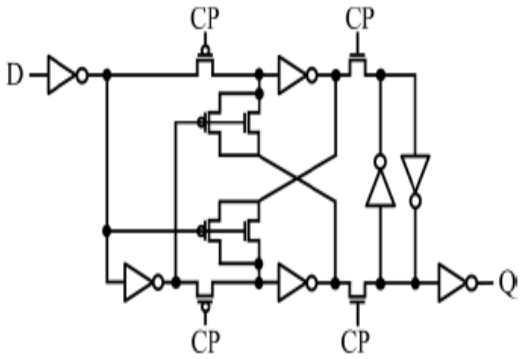

Fig. 6. Adaptive-coupling flip-flop (ACFF).

Give us a chance to outline the examination on beforehand revealed low-control FFs. For Daffy [1] and XCFF [7], pre-charge task is a worry particularly in brings down information action. As respects CFF [4], its cell territory turns into a bottleneck to utilize. What's more, for ACFF [9], resistance for input clock slew variety winds up subject to determine.

DISADVANTAGES

1. Input clock slew variety
2. Performance corruption

III. Multi-Bit Flip-Flops

3.1 Multi-Bit Flip-Flops

A as of late distributed paper has underscored the use of Multi-Bit Flip-Flops (MBFFs) as a plan procedure conveying extensive power decrease of advanced frameworks [1]. The information of advanced frameworks is typically put away in Flip-Flops (FFs), each having its own particular inner clock driver. Appeared in Fig. 1, an edge-activated 1-bit FF contains two fell ace and slave hooks, driven by inverse tickers CLK and CLK . It is appeared in Section 2 that the vast majority of the FF's vitality is devoured by its inner clock drivers, which are critical supporters of the aggregate power utilization.

While trying to diminish the clock control, a few FFs can be gathered in a module with the end goal that regular clock drivers are shared for all the FFs. Two 1-bit FFs gathered into 2-bit MBFF, called likewise double piece FF [1], are appeared in Fig. 1. In a comparable way, gathering of FFs in 4-bit and 8-bit MBFFs are conceivable as well. We consequently indicate a k - bit MBFF by k - MBFF. MBFF isn't us decreasing the entryway capacitance driven by a clock tree. The wiring capacitive load is additionally lessened on the grounds that us a solitary clock wire is required for various FFs. It likewise diminishes the profundity and the cushion sees of the clock tree and furthermore the quantity of sub-trees. Past clock control investment funds those highlights likewise lessen the silicon one.

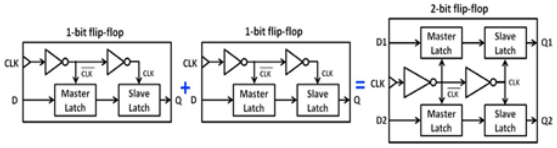

Fig. 7.1-bit FF and 2-MBFF.

MBFFs benefits don't seek free. By sharing basic drivers, the inclines of the clock signals turn out to be slower, causing bigger short out momentum and clock-to- engendering delay (tic) debasement. Revealed in [1], for an outline executed in a 90 nanometer, low-control, high voltage edge (HVT) CMOS innovation, the 4-MBFFs display a for each piece 30% decrease of dynamic clock control, and a for every piece 10% region decrease. That went ahead the cost of a for every piece 20% information control increment and furthermore 20% corruption of tic . In any case, because of the way that the normal information to-clock flipping proportion of a FF is little, fluctuating from 0.01 to 0.1 in many plans [2], the clock control investment funds dependably exceeds the short out power punishment on the information flipping. This work answers two inquiries; what ought to be the ideal piece assortment of MBFFs, and how to use from the information of the normal information to-clock flipping proportion (called likewise movement and information flipping likelihood) of the FFs in the fundamental outline.

To cure the short out power punishment and tic debasement because of the expansion of the heaps, the MBFF inward derivers can be fairly reinforce. This is demonstrated pictorially in Fig. 1 by the bigger 2-MBFF drivers contrasted with 1-bit. The MBFF variety k relies upon the information flipping likelihood p . Area 2 examines that reliance trying to upgrade the MBFF configuration stream and expand the power funds. To our best learning, that has not been examined up until now.

IV. RELATED WORK

Seyed E. Esmaeili Rttl. has proposed conditional capturing which is used to minimize power at low data switching activities by eliminating redundant internal transitions. Reduced swing inverters similar to the one presented in is used at the node fed by the low-swing [3] sinusoidal clock signal. This is done to reduce short circuit power. The load pMOS transistor in the reduced swing inverters is always in saturation since Vgs=Vds. It lowers the voltage at the source of the second pMOS in each inverter to approximately VDD-|Vtp| thus turning it off when the low-swing sinusoidal clock signal reaches its peak voltage. S.E. Esmaeili A.J. Al-Khalili G.E.R describes the differences in the results for the TDQ response of the dualedge triggered flip-flop at the positive and negative clock edges obtained from schematic and post-layout simulations. The resonant sinusoidal clock signal becomes a square wave clock when inverted using an inverter. The effect of the long rise time of the positive edge of the

sinusoidal clock signal CLK1, which defines the start of the first evaluation interval TE1, compared to the effect of the short rise time of the inverted square signal CLK2, which defines the start of the second evaluation interval TE2, on the TDQ delay against TDCLK delay (Tsetup) is investigated. Chulwoo Kim, Member, IEEE has proposed a schematic diagram of our LSDFF composed of a data-sampling front and data-transferring back end. Internal nodes X and Y are charged and discharged according to the input data D, not by the clock signal. Therefore, internal nodes of LSDFF switch only when the input changes. LSDFF does not require a conditional capture mechanism, as used in the pulse-triggered true-single-phase-clock (TSPC) flip-flop (PTTFF). In PTTFF, either one of the data-precharged internal nodes is in floating state, which may cause malfunction of the flip-flop. Also, its internal node does not have a full voltage swing, which causes performance degradation. Hamid Mahmoodi, has proposed the conventional energy recovery clocked flip-flop, are presented and their operations are discussed. The conventional energy recovery clocked flipflop is a four-phase transmission-gate (FPTG) flip-flop. FPTG is similar to the conventional transmission- gate flip-flop (TGFF) except that it uses four-transistor pass-gates designed to conduct during a short fraction of the clock period. The main disadvantages of this flip-flop are the need for four sinusoidal clock signals and its long delay. Transistors required for the pass-gates are large, resulting in large flip-flop area. Another approach for energy recovery clocked flip-flops is to locally generate square-wave clocks form a sinusoidal clock.

V. PROPOSED METHOD

Digital logic is the foundation for digital computers, to understand the innards of computers. There are a number of different systems for representing binary information in physical systems. A voltage signal with zero (0) corresponding to '0' volts and one (1) corresponding to five or three volts. VLSI is the field which involves packing more and more logic devices into smaller and smaller areas. This has opened up a big opportunity to do things that were not possible before. Resonant clocking is an emerging promising technique to reduce the power of the clock network. The inductor used in resonant clocking enables the conversion of the electric energy stored on the clock capacitance to magnetic energy in the inductor and vice versa. The concept of the slack in the clock skew has been extended for an LC fully-resonant clock distribution network [11]. This extra slack in comparison to standard clock distribution networks can be used to reduce routing complexity, achieve reduction in wire elongation, total wire length, and power consumption.

Around 66% of clock power is being dissipated in the last buffer stage driving the flip-flops leading to minor power savings in LC globally-resonant [7] locally square CDNs. In order to achieve maximum power savings, the LC tank should drive the entire clock network without using intermediate buffers. This would require designing, modifying and understanding flip-flop performance with the sinusoidal clock signal generated in LC resonant networks, demonstrated that a low-swing square-wave clock double-edge triggered flip-flop [8] has enabled 78% power savings in the CDN [11]. The clock buffers are removed to allow the global and local clock energy to resonate between the inductor and entire clock capacitance including the receiving end flip-flops thus enabling maximum power savings. In addition, removing the clock buffers simplifies LC low-swing clocking [3] since only reduced swing buffers are used at the flip-flop gate and not in intermediate levels within the clock tree. A low swing differential conditional capturing flip-flop is used in low-swing LC resonant CDNs introduced, application of low-swing clocking to LC resonant CDNs. No additional power supply is required to achieve low-swing clocking. A design of a global clock distribution network is presented in which four resonant circuits are connected to a conventional H-tree. Each quadrant consists of an on-chip spiral inductor that resonates with the wiring capacitance of the clock network and the decoupling capacitor is connected to the other end of the spiral inductor. A simple lumped circuit model is utilized to determine the resonant inductance. Based on this structure, a design methodology for resonant H-tree clock distribution networks is proposed. To deliver a full swing signal at the sink nodes, the magnitude of the transfer function of the network. This parameter is often fixed. Several resonant circuits can be utilized to improve the characteristics of the clock signal. The number of resonant circuits also affects the output signal swing. By increasing the number of resonant circuits and placing these circuits closer to the sink nodes, each inductor resonates with a smaller part of the circuit resulting in lower attenuation of the

output signal swing. Alternatively, increasing the number of resonant circuits and using larger inductors in each LC tank reduces the quality factor of the LC tanks, since in spiral inductors the effective series resistance increases more aggressively than the inductance. A lower quality factor for resonant circuits produces a higher signal loss and decreases the output signal swing.

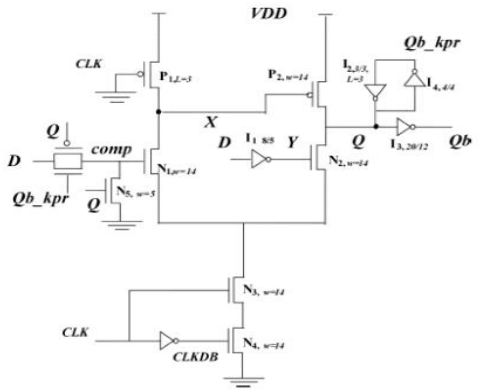

Fig.1. Clocked pair shared flip-flop.

By doubling the number of LC tanks, the inductance of each tank is also doubled. In this approach, the inductive component of the network wires is not considered. In large clock networks, with long interconnect, the inductance of the wires cannot be neglected. This method assumes that placing the resonant circuit in different locations does not change the equivalent capacitance of the network. These simplifications can result in inaccurate estimation of the resonant inductance, adversely affecting the signal swing. Employing any inductance within the crosshatched ranges, this clock network can meet the signal swing specifications. A distributed RLC model for the network wires is used to determine the required parameters for resonance. Different locations for the resonant circuits from the root to the sinks are investigated. For each location, the driver resistance is adapted to produce a transfer function magnitude of 0.9 for a wide range of inductor sizes. The inductance for which the driver resistance is maximum or the power consumption is minimum is determined.

To demonstrate the correct operation of the proposed LSDCCFF and to highlight potential power savings enabled through low-swing clocking, a test chip with a MAC unit designed using the proposed flip-flop under low-swing sinusoidal clocking was fabricated in TSMC 90-nm CMOS technology. Since the 16 bit multiplier not pipelined, a clock frequency of 100 MHz was chosen for the test chip. Due to the large inductor needed for clock generation and the limited area available, the clock generator was not implemented on-chip. The sinusoidal clock signal is fed by an external source through an analog pad. The differential conditional capturing flip flop was modified to enable dual-mode operation of the MAC unit under full and low swing clocking without significant area overhead.

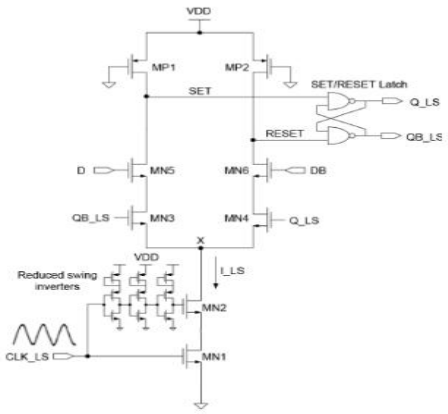

Fig.2. LS-DCCFF

When signal full swing is high, full-swing clocking is enabled and the inverted clock output of the normal inverters CLKD FS is feeding transistor MN1. Whereas low-swing clocking is enabled when signal full swing is low and the output of the reduced voltage swing inverters CLKD LS feeds transistor MN1. Two separate instances of the full and low swing DCCFF were implemented at the lower portion of the chip for testing. Due to the large capacitance [5] associated with the pads, all outputs were connected to the pads through a buffer stage consisting of four progressively sized inverters clock signal (channel 1, first signal from top), the inverted clock simulation on extracted circuits verifies correct functionality of both flip-flops under best conditions given by the Fast Fast (FF) corner at a low temperature , normal conditions given by the typical corner at room temperature, and worst conditions given by the Slow Slow (SS) corner at a high temperature. An average reduction in the delay of 130 ps was observed in the FF corner whereas the SS corner resulted in 76 ps increase in delay compared to the TT corner. Furthermore, correct functionality of both flip-flops under low and full swing sinusoidal clocking with 10% variation in the supply voltage was verified through measurements. A 10% variation in

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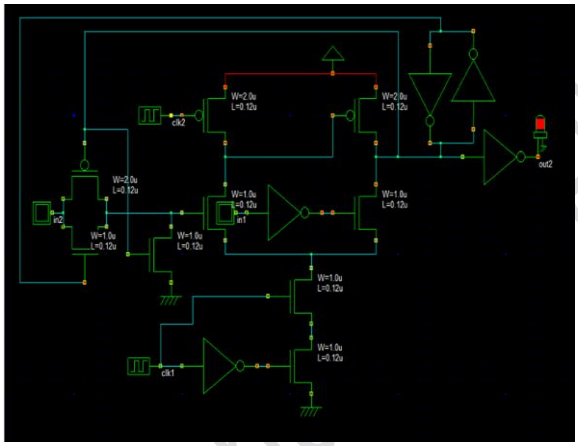
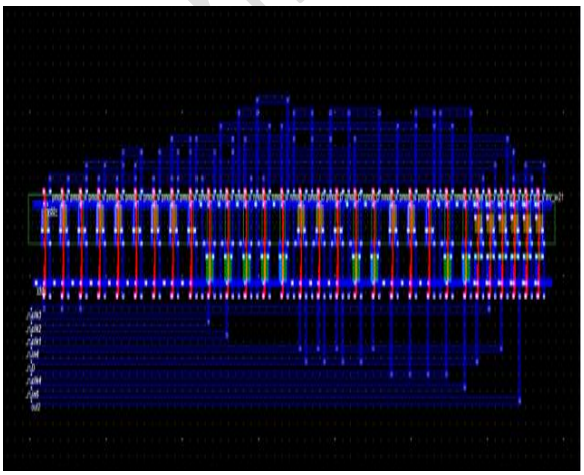
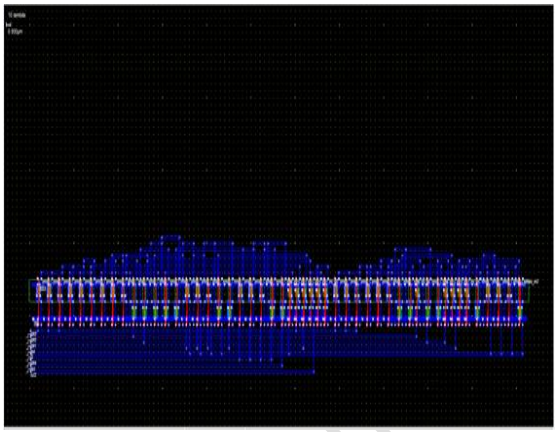
low swing clock results in 99 ps reduction and 300 ps increase in hold time. Hold time reduces with higher clock swing due to a reduction in the delay of reduced swing inverters. The opposite is true for lower clock swing. The negligible variation in delay with clock swing is basically due to the change in the time required for the clock signal. The extra delay associated with measurements can be related to the extra capacitance of the pads, package, wires, and test fixture. The behavior of the current flowing through node FS for the full swing flip flop and ILS for the low-swing flip flop as well as the voltage level of nodes SET and QB for the two flip-flops for the same setup time of 950 ps . The maximum current flowing from node to ground in the full and low swing flipflops occurs when the full swing clock CLK FS and low swing clock signal CLK_LS at the gate of transistor MN1 reaches 500 mV. At this point, node SET is pulled down and the output of the NAND latch is pulled up.

VI. SIMULATION RESULTS







VII. CONCLUSION

Low swing differential capturing flip-flop (LSDCFF) consume less power. It reduces capacity of clock load, reduces Short circuit current power. Low swing differential capturing flip-flop used only less clocked transistors, used less power. Overall power dissipation is different for the proposed methodologies due to the variation in the capacitive loading across the rotary ring. A novel energy recovery clocked flip-flops that enable energy recovery from the clock network, resulting in significant total energy savings compared to the square-wave clocking. The proposed flip-flops operate with a single-phase sinusoidal clock, which can be generated with high efficiency and implemented energy recovery clocked flip flops through a clock network driven by a resonant clock generator, generating a sinusoidal clock. The results demonstrate the feasibility and effectiveness of the energy recovery clocking scheme in reducing total power consumption. The power attained from low swing differential conditional capturing flip flop is 0.298mw

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