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DESIGN OF AREA EFFICIENT COUNTER DESIGN USING T-FLIPFLOP WITH MAJORITY FORMULATIONS

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ABSTRACT

The quantum-dot cellular automata (QCA) nano-technique has attracted computer scientists due to its noticeable features such as low power consumption and small size. Many papers have been published in the literature about the utilization of this technology for de-signing many QCA circuits and for presenting logic gates in an optimal structure. The T flip-flop, which is an essential part of digital designs, can be used to design synchronous and asynchronous counters. This paper presents a novel T flip-flop structure in an optimal form. The presented novel gate was used to design an N-bit binary synchronous counter. The QCA Designer software was used to verify the designed circuits and to present the simulation results. The proposed design provides minimal area over previous designs.

INTRODUCTION

1.1.CMOS

Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. In 1963, while working for Fairchild Semiconductor, Frank Wanlass patented CMOS. CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor. The words "complementary-symmetry" refer to the fact that the typical design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic, for example transistor–transistor logic (TTL) or NMOS logic, which normally have some standing current even when not changing state. CMOS also allows a high density of logic functions on a chip. It was primarily for this reason that CMOS became the most used technology to be implemented in VLSI chips. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material.

1.2.QUANTUM-DOT CELLULAR AUTOMATA (QCA)

CA takes great advantage of a physical effect of the cell, the Coulomb force that interacts between electrons. Though it is still difficult to yield and activate with these devices below typical temperature settings, simulations forecast promising numbers, like theoretical clock rates of several THz. QCA does not operate by the transport of electrons, but their operation is based on the fine-tuning of electrons in a small limited space of only a few square nanometers. Power consumption of QCA is extremely lower than CMOS because there is no any current in the circuit and output capacity. QCA is implemented by quadratic cells named as QCA cells. QCA cells are in squares shape has just four potential wells are located in each corner of the QCA cell.

In the QCA cells, exactly two electrons are locked in potential well that is only two wells able to be fill with electron and remaining two potential well remains empty. The potential wells are connected with electron tunnel junctions act as tunneling capacitor. By using a clock signal they can be unlocked for the electrons to travel through them under a particular condition. Due to the Coulomb force that interacts between the two electrons and without any interaction from outside will try to separate the electrons from each other as far as possible. The diagonal is the largest possible distance for them to reside so the electrons diagonally reside into potential well.

A basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. Electrons are able to tunnel between the dots, but cannot leave the cell. If two excess electrons are placed in the cell, Coulomb repulsion will force the electrons to dots on opposite corners. There are thus two energetically equivalent ground state polarizations can be labeled logic "0"and "1".The basic building blocks of the QCA architecture are AND,OR and NOT. By using the Majority gate we can reduce the amount of delay i.e. by calculating the propagation and generational carries.

The basic QCA device

The basic device in QCA is a QCA cell which enables both the computation and transmission of the information. A QCA cell consists of a hypothetical square space with four electronic sites and two electrons. The electronics sites, called Dots, represent the locations which the electrons can occupy. The dots are coupled through quantum mechanical tunneling barriers and electrons can tunnel through them depending on the state of the system. Exactly two mobile electrons are loaded in the cell and can move to different quantum dots in the QCA cell by means of electron tunneling.

Columbic repulsion will cause the electrons to occupy only the corners of the QCA cell resulting in two specific polarizations. Electron tunneling is assumed to be completely controllable by potential barriers (that would exist underneath the cell) that can be raised and lowered between adjacent QCA cells by means of capacitive plates.

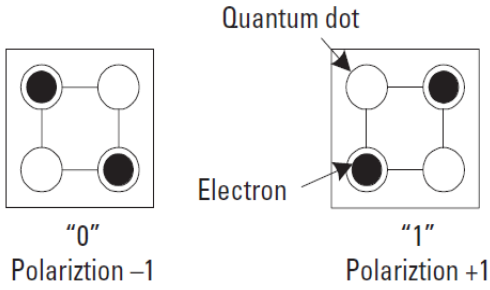

Fig 1. QCA cell with polarizations

For an isolated cell there are two energetically minimal equivalent arrangements of the two electrons in the QCA cell, denoted cell polarization P = +1 and cell polarization P = -1. Cell polarization P = +1 represents a binary 1 while cell polarization P = -1 represents a binary 0. This concept is also illustrated graphically in fig 1.8 It is also worth noting that there is an unpolarized state as well. In an unpolarized state, inter-dot potential barriers are lowered which reduces the confinement of the electrons on the individual quantum dots.

Consequently, the cells exhibit little or no polarization and the two-electron wave functions have delocalized across the cell. The numbering of dots denoted by i in the cell goes clockwise starting from the dot on the top right with i =1, bottom right dot i =2, bottom left dot i =3, and top left dot i=4. The polarization measures the charge configuration i.e. the extent to which the electronic charge is distributed among the four dots.

QCA wire

Figure 1.9 illustrates how a binary value propagates down the length of a QCA wire. A 90-degree wire is a horizontal row of QCA cells. The binary signal propagates from left-to-right because of the Columbic interactions between cells.

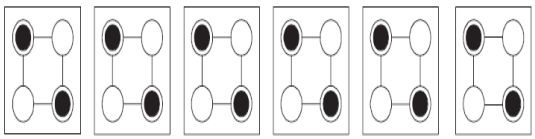

Fig .2. QCA wire composed of coupled cells

Binary '0' (from polarization P = -1) will propagate down the length of the wire because of the

Columbic interaction between the cells. Initially, the electron repulsion caused by Columbic interaction between cell 1 and cell 2 will cause cell 2 to change polarizations. Then, the electron repulsion between cell 2 and cell 3 will cause cell 3 to change polarizations. This process will continue down the length of the QCA wire.

Majority logic gate

The fundamental QCA logical circuit is the three-input majority logic gate that appears in Figure 1.10 from which more complex circuits can be built. The basic majority gate is obtained by placing four neighboring cells adjoining to a device cell, which is in the middle. Three of the side cells are used as inputs, while the remaining one is the output. The device cell will always assume the majority polarization because it is this polarization where electron repulsion between the electrons in the three input cells and the device cell will be at a minimum.

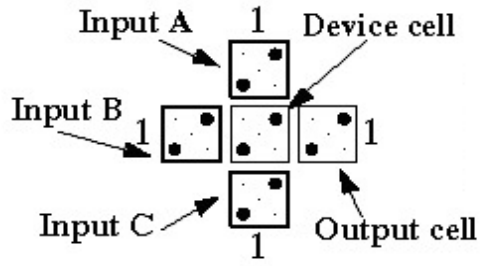

Fig.3. Fundamental QCA logic device

To understand how the device cell reaches its lowest energy state, consider the columbic interaction between cells 1 and 4, cells 2 and 4, and cells 3 and 4. Columbic interaction between electrons in cells 1 and 4 would normally result in cell 4 changing its polarization because of electron repulsion (assuming cell 1 is an input cell). However, cells 2 and 3 also influence the polarization of cell 4 and have polarization P=+1.

II. LITERATURE SURVEY

One of the hottest issues in today's nano electronics is quantum-dot cellular automata (QCA) which was firstly introduced by Lent et al. in 1993. In this concept, interfering of quantum physics and nano technology in electronics manufacturing leads to smaller and more efficient circuits. The logic of quantum- dot cellular automata is very similar to the binary logic models commonly used in computer architecture.

Attractive features of this new technology such as high speed, low power consumption and straightforward designing rules have resulted in many research works in last decade. One of the most attractive areas in QCA technology is designing memory cells. Saving data in computer architectures is a vital notion and consequently memory cell is among the most momentous and fundamental building blocks in digital systems which contribute to the major part of the area, delay and power consumption on electronic chips.

As a result, any optimization in its complexity and performance directly improves the performance of whole system. To date, lots of studies have been carried out by the researchers in designing efficient QCA memory cells, such as different structures for random access memory cell, well-optimized QCA architectures for flip-flops and counter designs. In addition, logical and arithmetical circuit designs have been extensively investigated in several studies.

It is worth pointing out that all the mentioned studies have completely dropped the importance of energy consumption in QCA architectures. The first accurate QCA power dissipation model among numerous performed studies has been proposed by Timler and Lent. According to the valuable results of this study, Srivastava et al. have proposed an upper bound power dissipation for QCA circuits. In 2011, QCA Pro tool was developed as an accurate power estimation tool based on the model by capability of presenting total energy consumption using two core terms called leakage energy and switching energy.

At nano regimes, computation is substantially different from conventional VLSI. In recent years, the so-called emerging technologies have been investigated to take advantage of extremely small feature size and high device density for implementing new computational paradigms at physical and logic levels for manufacturing, design and assembly. Among emerging technologies, quantum-dot cellular automata (QCA) relies on novel design concepts to exploit new physical phenomena (such as Coulombic interactions), and implement unique paradigms (such as memory-in-motion and processing-by-wire).

III. EXISTING METHOD

The main structural components for designing sequential circuits are flip-flops. Although the inherent capability of QCA technology makes each QCA cell a single D latch controlled by the clocking circuitry, it is important to design QCA flip-flops controlled by an enabling mechanism (independent of QCA clocking) such as conventional CMOS. Memory concept in QCA loop-based approach is realized by a loop containing four clock zones. This element can be
used for storing one bit data during one clock cycle employing feedback mechanism. In order to implement a high performance synchronous counter in QCA, designing well-optimized and high speed edge triggered flip-flops is the first vital issue. An early effort has made to implement QCA edge triggered flip-flops using innovative level converters and have designed n-bit synchronous counters based on different flip-flops.

One of the basic flip-flops, called T or trigger or toggle flip-flop has only a single data input, a clock input and two outputs. The T-type flip-flop is designed from a J-K flip flop by connecting its J-K inputs together. The term T comes from the ability to 'toggle' or complement its state and are also called single input JK flip-flop. Here we have assumed inputs J and K both as T and they are tied together.

The logic diagram of T flip flop is shown in fig.2. Evidently, this design is composed of four 3-input majority gates which are connected together to guarantee the correct functioning of the circuit. In the presented QCA implementation a well-organized two-input exclusive-or gate is clearly designed. After considering two four-phase feedback loops, data restoring mechanism is accomplished. The cost-effective implementation in Fig. 6b consumes 46 QCA cells in 0.06μm2 area.

When Clock and T signals take equal value of '1', Q output is inversed and while T or Clock signal takes '0', the out is remained unchanged.

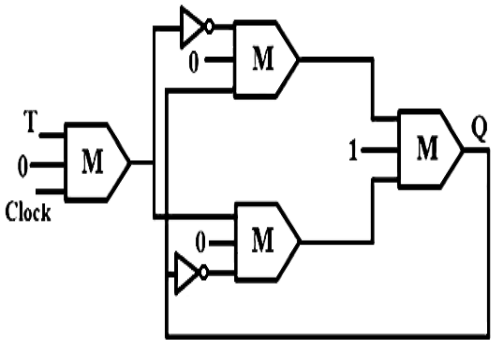

Fig .4. T flip flop by using majority gates

Synchronous counter design

T flip-flop is utilized as a fundamental building block of synchronous counters. In order to enable the edge detecting mechanism in the T flip-flop, a proper converter should be designed. As shown in figure, this circuit is comprised of a 2-input AND gate and an inverter.

By applying the inverted clock signal and one cycle delayed clock signal to the 2-input AND gate simultaneously, the proposed falling edge triggered converter operates. It is clear that only by a 1 to 0 transition of the clock; the output is set to 1. Fig 3.2 shows the 3 bit synchronous counter by using T flip flop. N-bit counter can be designed using n flip-flops counting 2n different states. Hence, the 3 bit synchronous counter counts from decimal 0 to 7. The waveform combination of three outputs (Q2 Q1 Q0) traces the following order 000-001-010-011-100-101-110-111.

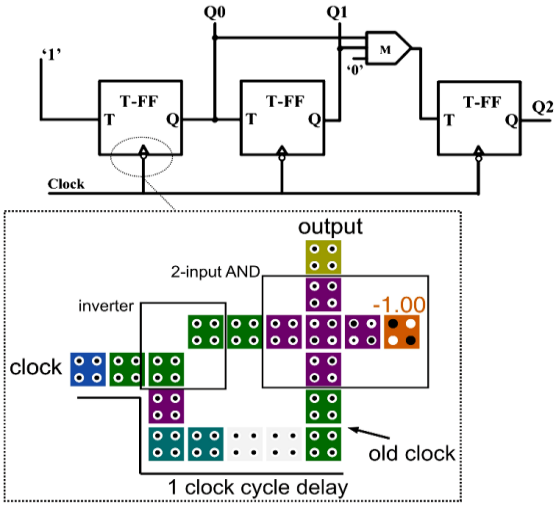

Fig .5. 3 bit synchronous counter

IV. PROPOSED SYSTEM

A quantum-dot cellular automaton (QCA) is one of the new nano electronics that has emerged in the last decade. QCA is being used as a new technique for computation. QCA is a good choice as a replacement for CMOS technology due to many aspects such as its ultra-high speed, small size, and low power consumption. It depends on electron configurations instead of voltage levels as in CMOS. The key issue in QCA is complexity reduction. Many papers have been presented on designing important digital circuits using QCA technology.

A counter is a type of sequential circuit constructed with a set of flip-flops connected in a suitable manner to be able to count sequence of inputted pulses. The counters are categorized into two types depending on the topology that is connected; asynchronous and synchronous. In the asynchronous counter, the output signal of one flip-flop represents a clock to the next one. As such, the time delay in this type of counter is the sum of all flip-flop's propagation delay. This drawback is overcome by the synchronous counter. In the synchronous counter, all flip-flops are connected to the same clock signal. As such, the time delay in this type of counter is the same propagation delay as a single flip-flop.

The synchronous counter is widely used in digital systems. It can count from 0–2N–1, where N is the number of the flip-flops used, or counter size. This project introduces a novel structure of the T flip-flop because the T flip-flop is widely used in digital counters, binary addition, and frequency divider circuits. As such, the designers looking for the optimal structure of the QCA flip-flop to obtain an optimal N-bit counter circuit.

The schematic diagram of the proposed T flip-flop is illustrated in fig 4.1a, while the QCA layout is shown in fig 4.1b. It is clear from the presented diagram that the T flip-flop was accomplished by using the XOR gate with the AND gate. The data storage was accomplished using a loop-based mechanism.

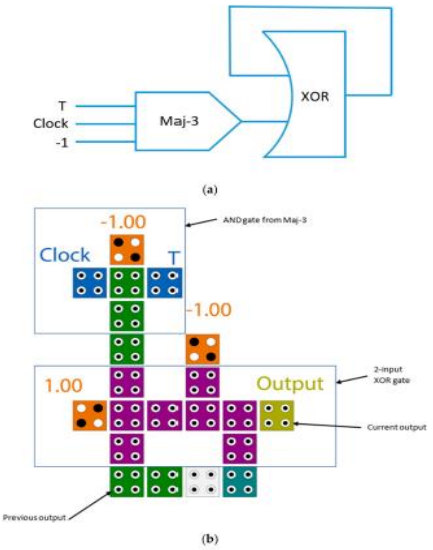

Fig .6. The proposed T flip-flop (LST-FF) (a) schematic diagram (b) QCA layout

Figure 6. illustrates the electron configurations inside cells for many cases of input and previous output. The proposed T flip-flop was level-sensitive and was constructed with only 21 cells with an area of 0.018 _m2. It was evident that the first significant waveform was obtained at the output after one clock cycle at clock phase 2, which was one clock phase faster than the best previously introduced counterparts. If the input signal (T) is 1 when the clock is available at a high level, the output will flip to the inverse state. Otherwise, the output will remain unchanged.

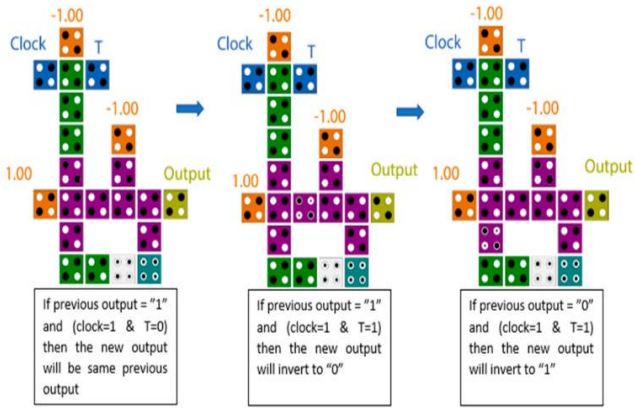

Fig .7. Electron configurations for many cases of input and previous output

Synchronous Counter

The novel LST-FF that was introduced in this project was utilized to design a new layout synchronous counter. The proposed counter used an optimal QCA circuit to accomplish a negative edge trigger. This edge detection circuit, as illustrated in fig 4.3, was constructed with an AND gate and inverter, and gave a high output only by the transition of 1–0.

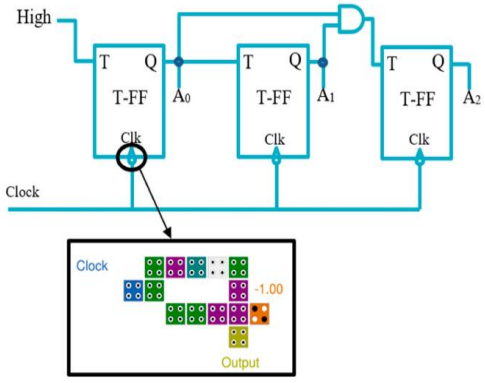

Fig .8. Synchronous 3-bit counter with negative edge-triggered QCA circuit

V. SIMULATION RESULTS

The following figures shows the QCA layout for T flip flop in both conventional and proposed methods with its timing diagram.

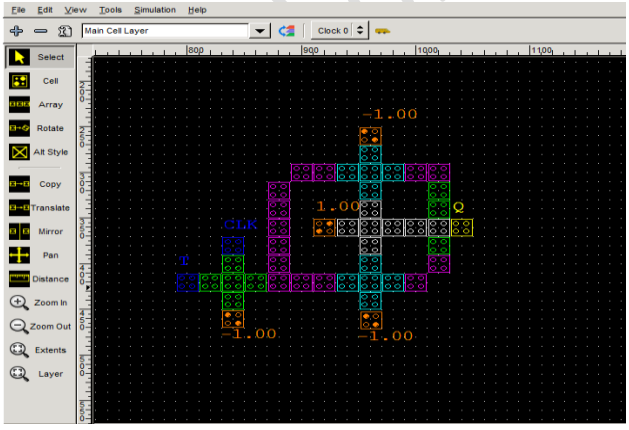

Fig 9: T flip flop (existing)

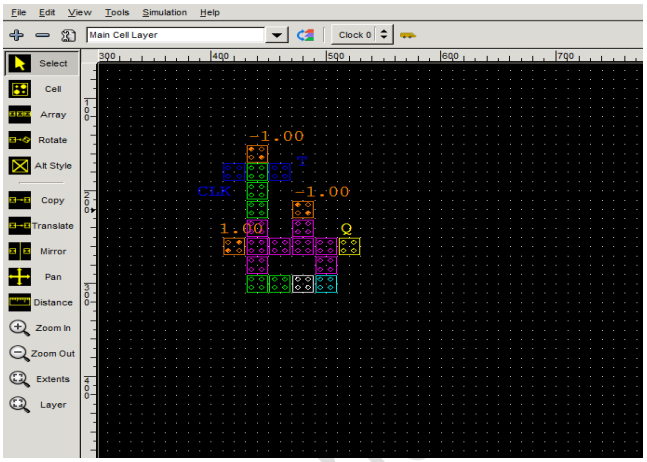

Fig 10: T flip flop (proposed)

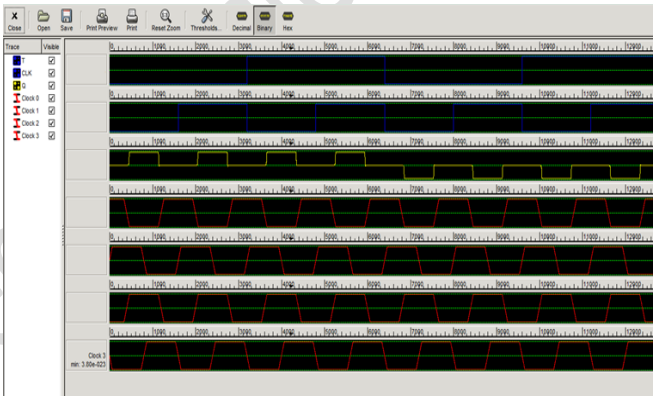

Fig 11: Timing diagram

The following figures shows the QCA layout for 3-bit synchronous counter in both conventional and proposed methods with its timing diagram.

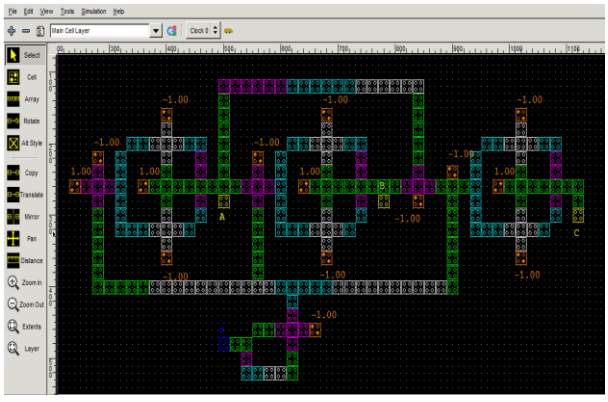

Fig .12: Existing synchronous counter

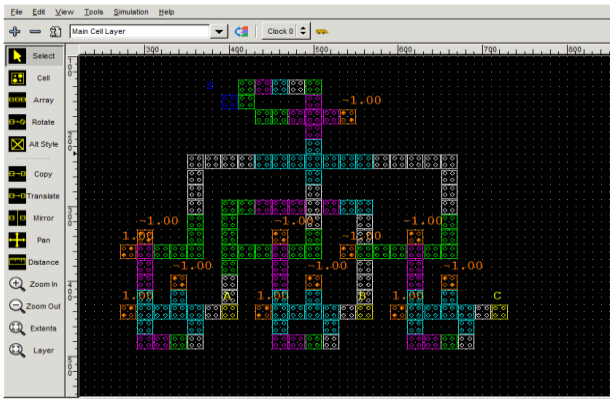

Fig 13: Proposed 3 bit synchronous counter

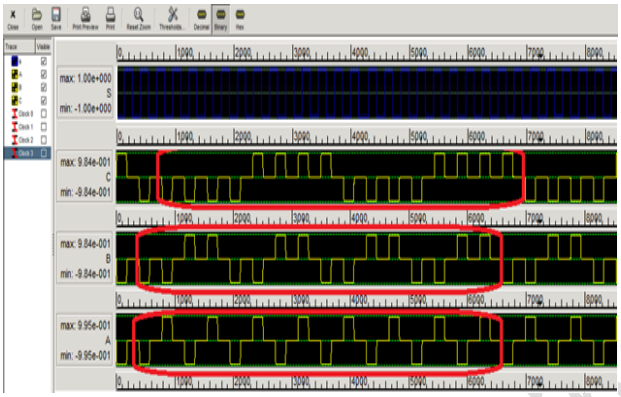

Fig 14: Timing diagram

Comparison:

The proposed T flip flop requires less number of cells and less area when compared to the conventional as shown in below table.

Table 5.1: Comparison results for T flip-flop

DESIGN	NUMBER OF GATES	CELL COUNT	AREA (µm2)
EXISTING	6	46	0.07
PROPOSED	2	21	0.03

The synchronous counter designed using proposed T flip flop requires less number of cells and is area efficient when compared to the conventional design.

Table 5.2: Comparison of synchronous counter designs

DESIGN	NUMBER OF GATES	CELL COUNT	AREA (µm2)
EXISTING	19	240	0.37
PROPOSED	7	140	0.17

ADVANTAGES

The advantages of the Synchronous counter is as follows

1. It's easier to design than the Asynchronous counter.
2. It acts simultaneously.
3. No propagation delay associated with it.
4. Count sequence is controlled using logic gates, error chances are lower.
5. Faster operation than the Asynchronous counter.

APPLICATIONS

Few applications where Synchronous counters are used

1. Alarm Clock, Set AC Timer, Set time in camera to take the picture, flashing light indicator in automobiles, car parking control etc.
2. Counting the time allotted for special process or event by the scheduler.
3. The UP/DOWN counter can be used as a self-reversing counter.
4. It is also used as clock divider circuit.
5. The parallel load feature can be used to preset the counter for some initial count.
6. Commons used in home appliances like washing machine, microwave own, Time schedule led indicator, key board controller etc.
7. They are also used in machine moving control.
8. Mostly used in digital clocks and multiplexing circuits.
9. They are used to generate saw-tooth waveform (Stair case voltage)
10. It is also used in digital to analog converters.

CONCLUSION

This project introduced an optimal form of the T flip-flop. The presented flip-flop was level-sensitive and was implemented with a noticeable area of 0.03 _m2 and at minimum complexity with only 21 cells. The unique proposed design of the flip-flop was utilized to implement synchronous counters with different sizes. However, only the 3-bit counter was reviewed in detail. This counter had the lowest number of cells and the smallest area. The verification of the proposed circuits was performed

using the QCA Designer software. A suitable converter with an optimal structure was designed to provide the counter with the ability to detect the edges of the clock signal.

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