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DESIGN OF LOW POWER VARIOUS MIXED LOGIC LINE DECODERS USING DSCH

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ABSTRACT: This brief introduces a mixed-logic design method for line decoders, combining transmission gate logic pass transistor dual-value logic, and static complementary metal-oxide semiconductor (CMOS). Two novel topologies are presented for the 2–4 decoder : a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power-delay performance. Both normal and inverting decoders are implemented in each case, yielding a total of four new designs. Furthermore, four new 4–16 decoders are designed by using mixed-logic 2–4 pre-decoders combined with standard CMOS post decoder. All proposed decoders have full-swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulations at 32 nm shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost all cases.

I. INTRODUCTION

In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines or fewer if the n-bit coded information has unused combinations. The circuits examined here are n-to-m line decoders, which generate the m = 2n minters of n input variables.

Static cmos circuits are used for the vast majority of logic gates in integrated circuits [1]. They consist of complementary N-type metal-oxide-semiconductor (nMOS) pulldown and P-type metal-oxide semiconductor (pMOS) pullup networks and present good performance as well as resistance to noise and device variation. Therefore, complementary metal-oxide semiconductor (CMOS) logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes [2]. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design.

Pass transistor logic (PTL) was mainly developed in the 1990s, when various design styles were introduced [3]–[6], aiming to provide a viable alternative to CMOS logic and improve speed, power, and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual nMOS/pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates.

The most conventional one is complementary CMOS full adder (C-CMOS) [9]. It is based on regular CMOS structure with pull-up and pull-down transistors and has 28 transistors. Another conventional adder is the Complementary Pass Transistor Logic (CPL) [10, 11, 12] with swing restoration which uses 32 transistors. CPL produces many intermediate nodes and their complement to make the outputs. The basic difference between the pass transistor logic and the complementary CMOS logic styles is that the source side of the pass logic transistor network is connected to some input signals instead of the power lines [13, 14]. A Transmission Gate Full-Adder (TGA) presented in [15] contains 20 transistors. Double pass transistor full adder cell has 48 transistors and operation of this cell is based on the double pass transistor logic in which both NMOS and PMOS logic networks are used.

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In present scenario, power reduction is a major issue in the technology world. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. The chip density and higher operating speed leads to the design of very complex chips with high clock frequencies. So designing of low power VLSI circuits is a technological need in these due to the high demand for portable consumer electronics products [2]. The development of electronic technology was started with the use of vacuum tube as active component in electronic series before semiconductor transistor replaces it. The development of microelectronic technology especially for those of mono-lyrical is able to produce interfaced circuit by combining all active and passive components in one chip [3]. High speed serialize/deserializers (SerDes) are now more and more widely used in communication systems for serial interconnections [4].

Decoders are used whenever an output or a group of outputs is to activated only on the occurrence of specific combination of input levels. These input levels are often provided by the outputs of a counter or register. When the decoder inputs come from a counter that is being continually pulsed, the decoder outputs will be activated sequentially, and they can be used as timing or sequencing the signals to turn devices ON or OFF at specific times. Decoders are widely used in memory systems of computers, where they respond to the address code input from the central processor to activate the memory storage location specified by the address code [1]. Low power consumption has been a priority and so pass transistor based tree decoders have been selected due to the lower leakage and dynamic switching currents. An asynchronous design would further help to reduce the dynamic power dissipation from the clock switching. Reliability has been the second important priority and design procedures for high read and write margins tolerant to process variations have been developed

DECODER

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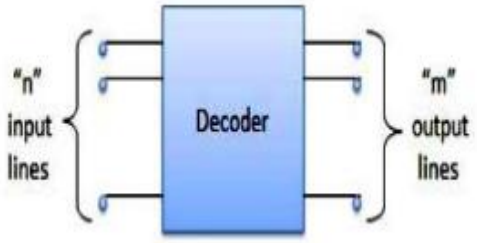

fig:1.General Block diagram of decoder

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The concept of digital data manipulation changes the society in attractive way even all the electronic gadgets are in digital formats. Due to invention of various digital IC technologies we are in VLSI era. These digital technologies have their own advantages and disadvantages. Due to invention of Bipolar Junction Technology (BJT) the first IC had been implemented that is TTL (Transistor- Transistor Logic). TTL logic provides higher packing density but slow turn off process. A new technology had been developed called ECL (emitter coupled logic) which is fastest logic but provides higher power dissipation. But unfortunately, in VLSI era, BJT is defeated by MOS technology. MOS provides lower power dissipation and high packing density than BJT. But again CMOS beat the MOS technology as it provides excellent static characteristics like lowest static power dissipation and highest Noise margin. But the problem with the CMOS ICs is their dynamic power dissipation and digital switching noise.

This problem is solved if we use differential amplifier. Because these amplifiers are not only less sensitive to noise but also enable us to bias amplifier and couple the amplifier stage together without the requirement for bypass and coupling capacitor. This born various technologies like SCL (source coupled logic), FSCL (folded Source Coupled Logic), MCML (MOS current Mode Logic). Static CMOS logic provides several advantages in designing digital circuit, that are low sensitivity to noise, good performance, low power consumption, etc. But it show some disadvantages while designing mixed mode ICs. In VLSI circuit, several logic gates switches simultaneously and resulting current causes switching noise. The mixed mode IC has both analog and digital circuit on single semiconductor die so this noise affect analog circuit through substrate coupling. This reduces speed and accuracy of mixed mode ICs. Various methods are used to reduce this noise in mixed mode ICs like separate analog and digital supply line, diffuse guard band, bonding pads etc. Source coupled logic(SCL) was developed to reduce this digital switching noise and it is most successful methods among all the constant current source technique

Now a day's power reduction is a major issue in the technology world. The low power design is major issue in high performance digital system, such as microprocessors, digital signal processors (DSPs) and other applications. Chip density and higher operating speed lead to the design of very complex chips with high clock frequencies. So designing of low power VLSI circuits is a technological need in these due to the

high demand for portable consumer electronics products. Decoder is a combinational logic circuit that converts a binary integer value to an associated pattern of output bits. Applications of decoders are wide; they include data de-multiplexing, memory address decoding, seven segment display etc. A decoder is a simple circuit that converts a code into a set of signals. It is named as decoder because it changes the big coded data into different simple combinations which can be used to drive any signal, but we will begin our study of encoders and decoders because they are simpler to design. Active instructions occur only within a sub-set of all instructions

Address decoder is essential elements in all SRAM memory block which respond to very high frequency. Access time and power consumption of memories is largely determined by decoder design. Design of a random access memory (RAM) is generally divided into two parts, the decoder, which is the circuitry from the address input to the word line, and the sense and column circuits, which includes the bit line to the data input/output circuits. Due to large amount of storage cells in memories it can be found various solutions of address decoder designs leading to power consumption reduction and performance improvement. Usually different kinds of pre charging dynamic decoders are used. Design of dynamic decoder is complex and having more probability of wrong sensing. Traditional static decoder gives more accurate result but it is having more number of transistors with large delay. Some solutions use hierarchical decoders with pre decoding and also implemented binary tree decoder built by De-multiplexers. Decoders plays a crucial role in memory applications so we introduce high-speed a mixed-logic design method for line decoders.

Address decoder using NAND-NOR alternate stages with pre decoder and replica inverter chain circuit is proposed and compared with traditional and universal block architecture, using 130nm CMOS technology. Delay and power dissipation is reduced in proposed design over existed design. Recently reported logic style comparisons based on full-adder circuits claimed complementary pass-transistor logic (CPL) to be much more power efficient than complementary CMOS. High speed multiplier is implemented with the help of Complementary Pass transistor Logic (CPL) is a family of CMOS design. Same CPL technique is used to implement Arithmetic and Logic Unit [ALU] in for increasing the design speed. Transmission switch theory is introduced which is used for CMOS digital circuit design. Complex logic gate is implemented in based on pass transistor dual voltage logic for low power applications. Paper describes about develop a Karnaugh map based method that can be used to efficiently synthesize pass transistor logic circuits, which have balanced loads on true and complementary input signals. The method is applied to the generation of basic two-input and three-input logic gates in CPL, DPL and DVL. The method is general and can be extended to synthesize any pass-transistor network. Above papers describes different techniques to implement logic designs which gives better results in terms of area, delay and power consumption. Three different decoder designs are implemented, they are AND–NOR, Sense–Amp, and the AND decoder. These pre charge based designs are analyzed the constraints (area, energy consumption and delay). AND based decoders

II. LITERATURE SURVEY

DECODER:

In digital systems, instructions as well as numbers are conveyed by means of binary levels or pulse trains. A decoder is a logic circuit that converts an N-bit binary input code into M output lines such that only one output line is activated for each one of the possible combinations of inputs. The decoder identifies or recognizes or detects a particular code. The N inputs can be a 0 or a 1, there are 2N possible input combinations or codes. For each of input combination only one of the M outputs will be active (HIGH), all other outputs will remain inactive (LOW). Some decoders are designed to produce active LOW output, while all the other outputs remain HIGH

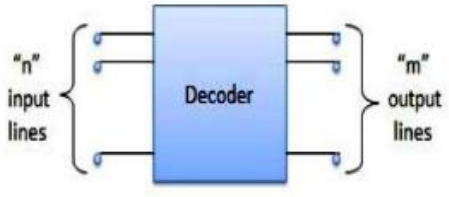


Fig.2. General Block diagram of decoder

2–TO-4 DECODER USING CMOS TECHNOLOGY:

In this paper, a 2-to-4 Decoder has been designed to reduce power consumption and surface area using 65nm, 45nm and 32nm complementary-metal- oxide semiconductor technology, which is then analyzed and comparative study has been done in account of the silicon surface area and power consumption. The proposed 2-to-4 Decoder using 32nm CMOS technology gives better results in terms of power and surface area as compare to 45nm and 65nm COMS technologies. The 2- to-4 decoder circuit size is 14.3 µm2 and typical power consumption is 0.172 µW at 32nm CMOS technology.

Comparison of proposed 2-to-4 Decoder is based on the performance parameters like surface area and power dissipation to achieve better performance using CMOS process by Micro wind 3.1 in 32nm, 45nm and 65nm technology. The proposed 2-to-4 Decoder circuit shown in figure 3, uses four 2-bit AND and two NOT logic gates.

Drawbacks:

- In this mainly disadvantage of the project different of technologies and different design construction

Low Power CMOS Full Adders Using Pass Transistor Logic:

The efficiency of a system mainly depends on the performance of internal components present in the system. The internal components should be designed in such a way that they consume low power with high speed. Lot of components is in circuits including full-adder. This is mainly used in processors. A new Pass transistor full adder circuit is implemented in this paper. The main idea is to introduce the design of high performance and based pass transistor full adders which acquires less area and transistor count. The high performance of pass transistor low power full adder circuit is designed and the simulation has been carried out on Tanner EDA Tool. The result shows that the proposed full adder is an efficient full adder cell with least MOS transistor count that reduces the high power consumption and increases the speed. In this paper CMOS full adder circuits are designed to reduce the power and area and to increase the speed of operation in arithmetic application. To operate at ultra-low supply voltage, the pass logic circuit that cogenerates the intermediate XOR and XNOR outputs has been improved to overcome the switching delay problem

III. EXISTING SYSTEM

In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n unique output lines or fewer if the n-bit coded information has unused combinations. The circuits examined here are n-to-m line decoders, which generate the m = 2n minters of n input variables.

2–4 Line Decoder:

A 2–4 line decoder generates the 4 minters D0−3 of 2 input variables A and B. Its logic operation is summarized in Table I. Depending on the input combination, one of the 4 outputs is selected and set to 1, while the others are set to 0. An inverting 2–4 decoder generates the complementary minters I0−3, thus the selected output is set to 0 and the rest are set to 1, as shown in Table II. In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency. A 2–4 decoder can be implemented with 2 inverters and 4 NOR gates Fig. 1(a), whereas an inverting decoder requires 2 inverters and 4 NAND gates Fig. 1(b), both yielding 20 transistors

Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g., SRAM) [7]–[9]. This brief develops a mixed-logic methodology for their implementation, opting for improved performance compared to single-style design. The rest of this brief is organized as follows: Section II provides a brief overview of the examined decoder circuits, implemented with conventional CMOS logic. Section III introduces the new mixed-logic designs. Section IV conducts a comparative simulation study among the proposed and conventional decoders, with a detailed discussion on the derived results. Section V provides the summary and final conclusions of the work presented.

TABLE I
TRUTH TABLE OF THE 2–4 DECODER

A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

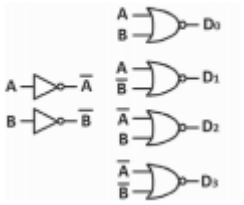


Fig:3.Noninverting NOR-based decoder.

Table: Truth table of the inverting 2–4 decoder

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

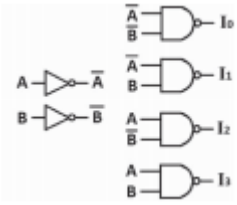


Fig: 4.Inverting NAND-based decoder

B. 4–16 Line Decoder :With 2–4 Predecoders

A 4–16 line decoder generates the 16 minters D0−15 of 4 input variables A, B, C, and D, and an inverting 4–16 line decoder generates the complementary minters I0−15. Such circuits can be implemented using a prerecording technique, according to which blocks of n address bits can be prerecorded into 1-of-2n prerecorded lines that serve as inputs to the final stage decoder [1]. Therefore, a 4–16 decoder can be implemented with 2 2–4 inverting decoders and 16 2-input NOR gates [Fig. 2(a)], and an inverting one can be implemented with 2 2–4 decoders and 16 2-input NAND gates [Fig. 2(b)]. In CMOS logic, these designs require 8 inverters and 24 2-input gates, yielding a total of 104 transistors each.

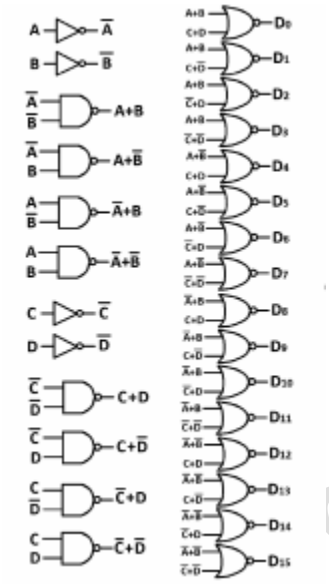


Fig:5.Noninverting decoder implemented with two 2–4 inverting pre decoders and a NOR-based post decoder

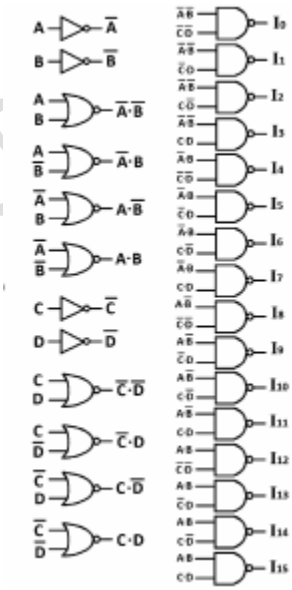


Fig: 6.Inverting decoder implemented with two 2–4 non inverting predecoders and a NAND-based post decoder

IV. PROPOSED SYSTEM

Transmission gate logic (TGL) can efficiently implement AND/OR gates [5], thus it can be applied in line decoders. The 2-input TGL AND/OR gates are shown in Fig. 3(a) and (b), respectively. They are full-swinging, but not restoring for all input combinations. Regarding PTL, there are two main circuit styles: those that use nMOS-only pass transistor circuits, like CPL [3], andthose that use both nMOS and pMOS pass transistors, like DPL [4] and DVL [6]. The style we consider in this work is DVL, which preserves the

full swing operation of DPL with reduced transistor count [10]. The 2-input DVL AND/OR gates are shown in Fig. 3(c) and (d), respectively. They are full swinging but non-restoring, as well.

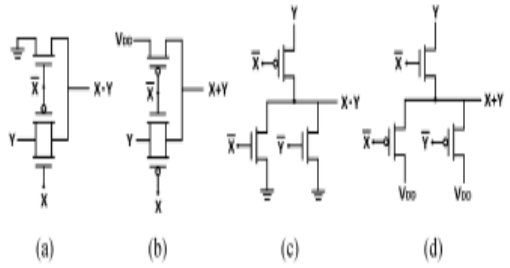


Fig. 7. Three-transistor AND/OR gates considered in this work. (a) TGL AND gate. (b) TGL OR gate. (c) DVL AND gate. (d) DVL OR gate.

Assuming that complementary inputs are available, the TGL/DVL gates require only 3 transistors. Decoders are high fan-out circuits, where few inverters can be used by multiple gates, thus using TGL and DVL can result to reduced transistor count. An important common characteristic of these gates is their asymmetric nature, ie the fact that they do not have balanced input loads. As shown in Fig. 3, we labeled the 2 gate inputs X and Y . In TGL gates, input X controls the gate terminals of all 3 transistors, while input Y propagates to the output node through the transmission gate. In DVL gates, input X controls 2 transistor gate terminals, while input Y controls 1 gate terminal and propagates through a pass transistor to the output. We will refer to X and Y as the control signal and propagate signal of the gate, respectively

Using a complementary input as the propagate signal is not a good practice, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the inhibition (A B) or implication (A + B) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND (AB) or OR (A + B) function, either choice is equally efficient. Finally, when implementing the NAND (A + B) or NOR (A B) function, either choice results to a complementary propagate signal, perforce.

4.1.14-Transistor 2–4 Low-Power Topology:

Designing a 2–4 line decoder with either TGL or DVL gates would require a total of 16 transistors (12 for AND/OR gates and 4 for inverters). However, by mixing both AND gate types into the same topology and using proper signal arrangement, it is possible to eliminate one of the two inverters, therefore reducing the total transistor count to 14. Let us assume that, out of the two inputs, namely, A and B, we aim to eliminate the B inverter from the circuit. The Do minterm (A B) is implemented with a DVL gate, where A is used as the propagate signal. The D1 minterm (AB) is implemented with a TGL gate, where B is used as the propagate signal. The D2 minterm (A B) is implemented with a DVL gate, where A is used as the propagate signal. Finally, The D3 minterm (AB) is implemented with a TGL gate, where B is used as the propagate signal. These particular choices completely avert the use of the complementary B signal therefore, the B inverter can be eliminated from the circuit, resulting in a 14-transistor topology (9 nMOS and 5 pMOS). Following a similar procedure with OR gates, a 2–4 inverting line decoder can be implemented with 14 transistors (5 nMOS and 9 pMOS) as well: I0 and I2 are implemented with TGL (using B as the propagate signal), and I1 and I3 are implemented with DVL (using A as the propagate signal). The B inverter can once again be elided. Inverter elimination reduces the transistor count, logical effort and overall switching activity of the circuits, thereby reducing power dissipation. The two new topologies are named “2–4LP” and “2–4LPI,” where “LP” stands for “low power” and “I” for “inverting.” Their schematics are shown in Fig. 4(a) and (b), respectively.

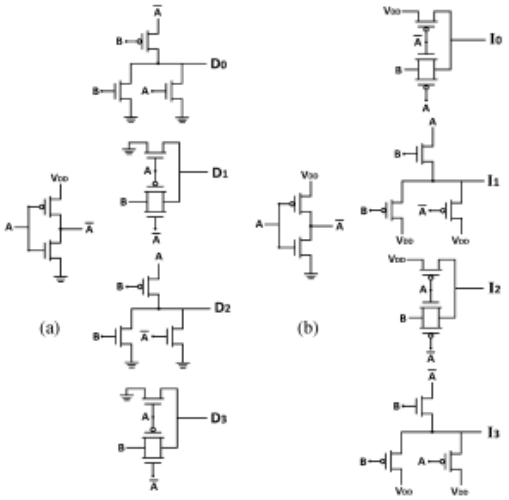


Fig. 8.New 14-transistor 2–4 line decoders.(a) 2–4LP. (b) 2–4LPI.

4.2. 15-Transistor 2–4 High-Performance Topology:

The low-power topologies presented above have a drawback regarding worst case delay, which comes from the use of complementary A as the propagate signal in the case of D0 and I3. However, D0 and I3 can be efficiently implemented using static CMOS gates, without using complementary signals. Specifically, D0 can be implemented with a CMOS NOR gate and I3 with a CMOS NAND gate, adding one transistor to each topology. The new 15T designs present a significant improvement in delay while only slightly increasing power dissipation. They are named "2–4HP" (9 nMOS, 6 pMOS) and "2–4HPI" (6 nMOS, 9 pMOS), where "HP" stands for "high performance" and "I" stands for "inverting." The 2–4HP and 2–4HPI schematics are shown in Fig. 5(a) and (b), respectively

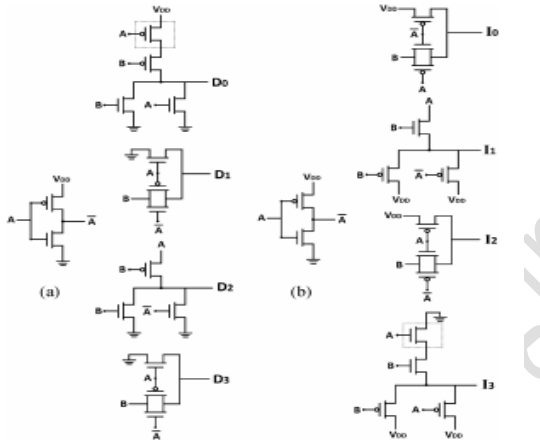


Fig. 9.New 15-transistor 2–4 line decoders.(a) 2–4HP. (b) 2–4HPI.

4.3.Integration in 4–16 Line Decoders:

PTL can realize logic functions with fewer transistors and smaller logical effort than CMOS. However, cascading PTL circuits may cause degradation in performance due to the lack of driving capability. Therefore, a mixed-topology approach, i.e., alternating PTL and CMOS logic, can potentially deliver optimum results.We implemented four 4–16 decoders by using the four new 2–4 as predecoders in conjunction with CMOS NOR/NAND gates to produce the decoded outputs. The new topologies derived from this combination are the following: 4–16LP [Fig. 6(a)], which combines two 2–4LPI predecoders with a NOR-based post decoder; 4–16HP [Fig. 6(b)], which combines two 2–4HPI predecoders with a NOR-based post decoder; 4–16LPI [Fig. 6(c)], which combines two 2–4LP predecoders with a NAND-based post decoder; and, finally, 4–16HPI [Fig. 6(d)], which combines two 2–4HP predecoders with a NAND-based post decoder. The "LP" topologies have a total of 92 transistors, while the "HP" ones have 94, as opposed to 104 with pure CMOS

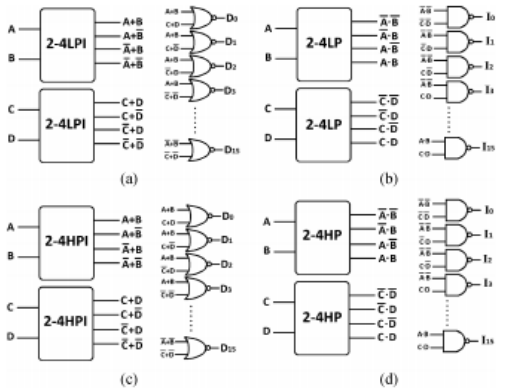


Fig. 10. New 4–16 line decoders. (a) 4–16LP. (b) 4–16LPI. (c) 4–16HP. (d) 4–16HPI

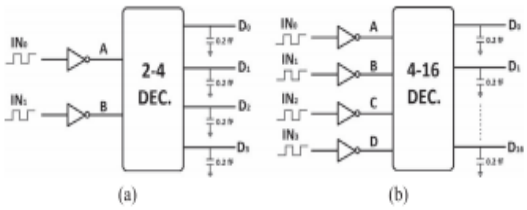


Fig.11.Simulation setup regarding input/output loading conditions.(a) 2–4 decoders. (b) 4–16 decoders.

We perform a variety of BSIM4-based spice simulations on the schematic level, in order to compare the proposed mixed-logic decoders with the conventional CMOS. The circuits are implemented using a 32 nm predictive technology model for low-power applications (PTM LP), incorporating high-k/metal gate and stress effect [11]. For fair and unbiased comparison we use unit-size transistors exclusively (Ln = Lp = 32 nm, Wn = Wp = 64 nm) for all decoders.

A. Simulation Setup

All circuits are simulated with varying frequency (0.5, 1.0, 2.0 GHz) and voltage (0.8, 1.0, 1.2 V), for a total of 9 simulations. Each simulation is repeated 5 times with varying temperature (−50, −25, 0, 25, and 50 ◦C) and the average power/delay is calculated and presented in each case. All inputs are buffered with balanced inverters (Ln = Lp = 32 nm, Wn = 64 nm, Wp = 128 nm) and all outputs are loaded with a capacitance of 0.2 fF, as shown in

Fig. 7. Furthermore, proper bit sequences are inserted to the inputs, in order to cover all possible transitions a decoder can perform. A 2–4 decoder has 2 inputs, which can generate 22 = 4 different binary combinations, thus yielding a total of 4 ∗ 4 = 16 possible transitions. The 2–4 decoders are simulated for 64 nanoseconds (ns), so that the 16-bit input sequences are repeated 4 times. Similarly, a 4–16 decoder has 4 inputs, 42 = 16 input combinations and 16 ∗ 16 = 256 possible transitions,therefore the 4–16 decoders are simulated for 256 ns to exactly cover all transitions once. Fig. 8 depicts the input/output waveforms of our proposed 2–4 decoders for all 16 input transitions, demonstrating their full swinging capability.

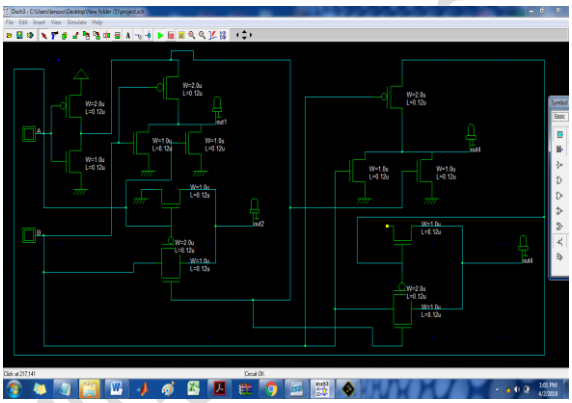
4.4.Performance Metrics Examined

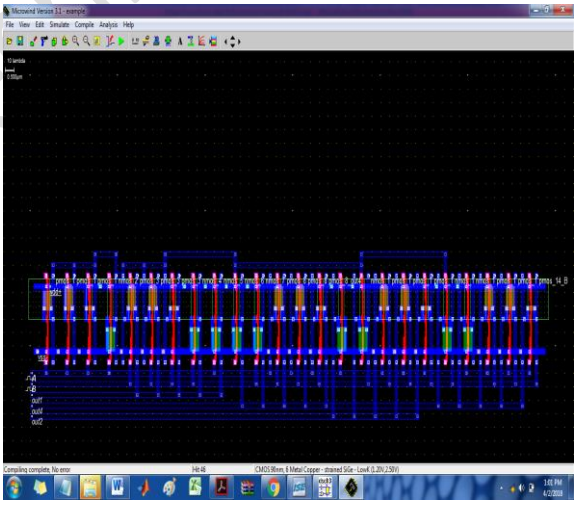
The metrics considered for the comparison are: average power dissipation, worst-case delay and power-delay product (PDP). With continuous sub-micron scaling and low voltage operation, leakage power has become increasingly important as it dominates the dynamic one [12]. In our analysis, both leakage and active currents are considered and the total power dissipation is extracted from spice simulation, measured in nanowatts (nW). Regarding delay, we note the highest value that occurs among all I/O transitions, measured in picoseconds (ps). Finally, PDP is evaluated as average power*max delay and measured in electronvolts (eV).

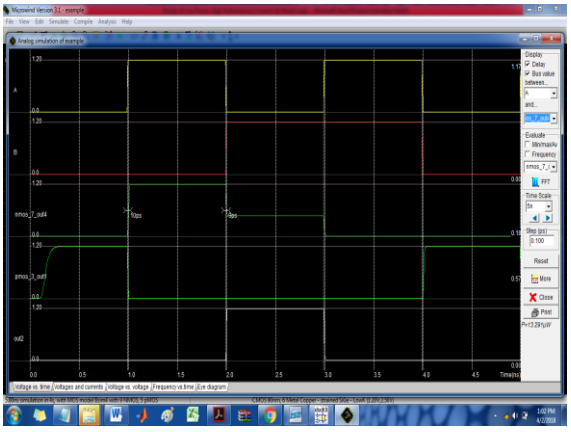
V. RESULTS

RTL & SIMULATION

The simulation results regarding power, PDP and delay are shown in Tables III–V, respectively. Each of the proposed designs will be compared to its conventional counterpart. Specifically, 2–4LP and 2–4HP are compared to 20T, 2–4LPI and 2–4HPI are compared to inverting 20T, 4–16LP and 4–16HP are compared to 104T and finally, 4–16LPI and 4–16HPI are compared to inverting 104T. According to the obtained results, 2–4LP presents 9.3% less power dissipation than CMOS 20T, while introducing a cost of 26.7% higher delay and 15.7% higher PDP. On the other hand, 2–4HP outperforms CMOS 20T in all aspects, reducing power, delay, and PDP by 8.2%, 4.3%, and 15.7%, respectively. Both of our inverting designs, 2–4LPI and 2–4HPI, outperform CMOS 20T inverting in all aspects as well. Specifically, 2–4LPI reduces power, delay, and PDP by 13.3%, 11%, and 25% respectively, while 2–4HPI does so by 11.2%, 13.2%, and 25.7%. Regarding the 4–16 simulations, the obtained results are similar. The 4–16LPI decoder, presents 6.4% lower power dissipation with the cost of 17.9% higher delay and 1.9% higher PDP than CMOS 104T. The rest of the decoders, namely, 4–16LP, 4–16HP, and 4–16HPI, present better results than corresponding CMOS decoders in all cases, which can be summarized.







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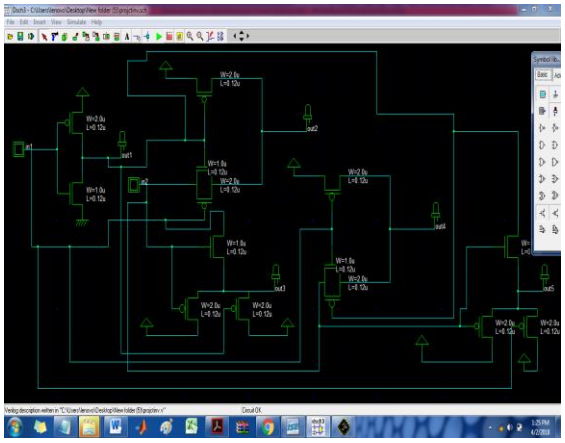

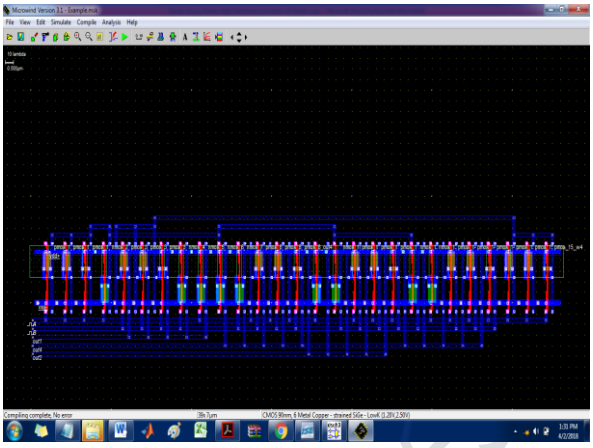

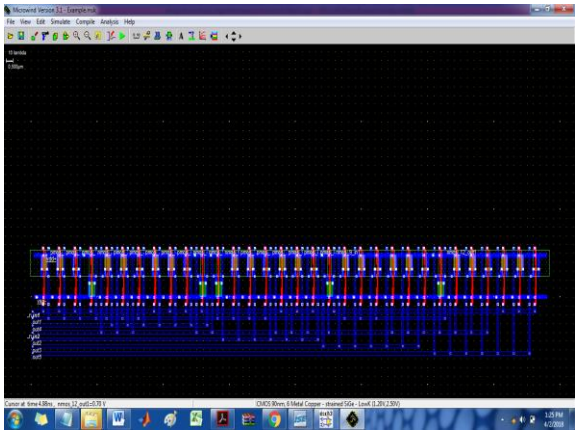

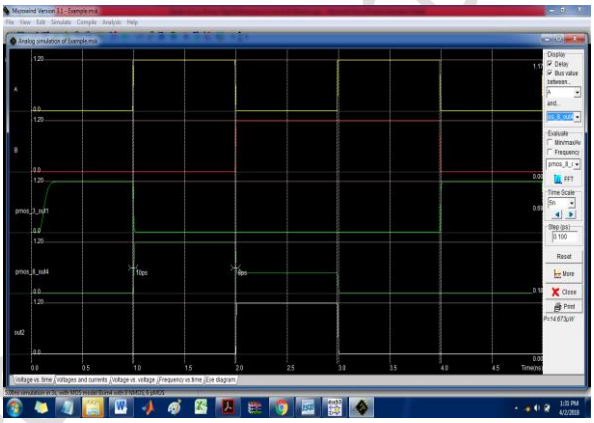

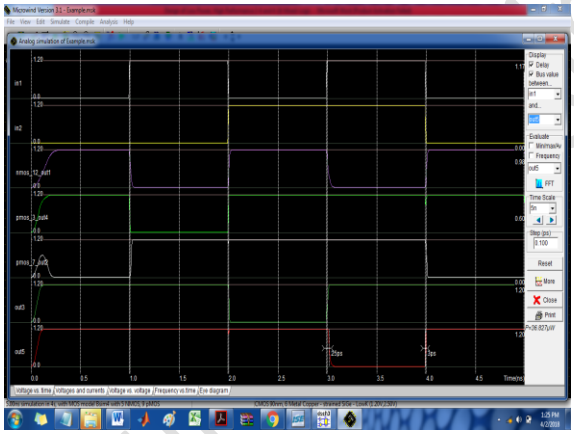

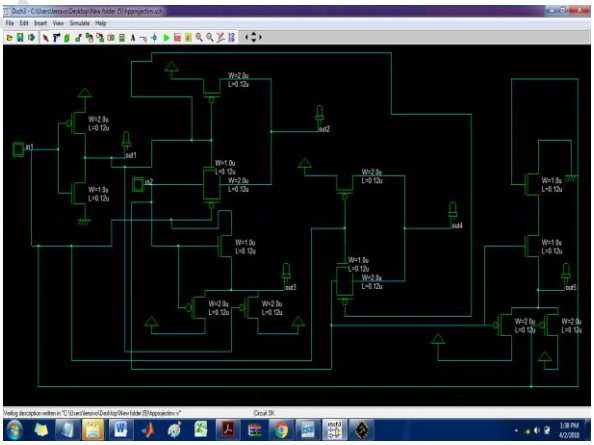

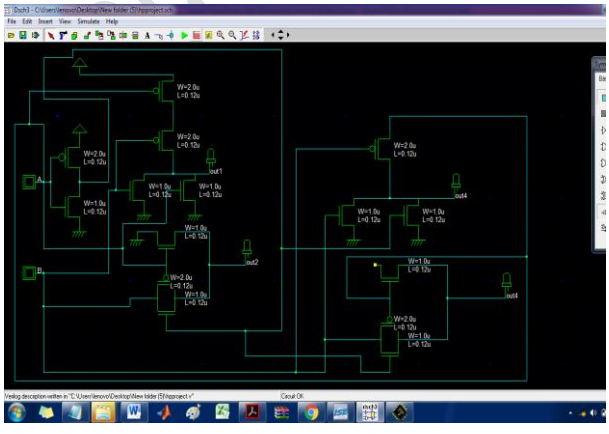

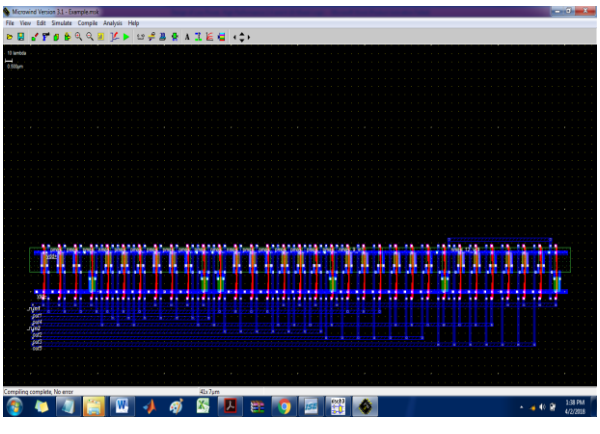

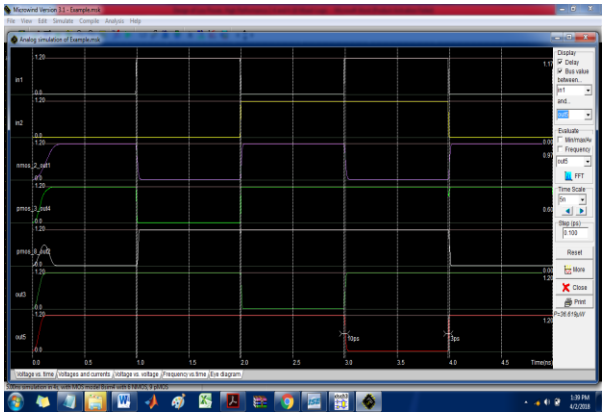

APPLICATIONS & ADVANTAGES

- Area should be decreased
- Power reduced
- Speed of operation increases

VI. CONCLUSION

This brief has introduced an efficient mixed-logic design for decoder circuits, combining TGL, DVL and static CMOS. By using this methodology, we developed four new 2–4 line decoder topologies, namely 2–4LP, 2–4LPI, 2–4HP and 2–4HPI, which offer reduced transistor count and improved powerdelay performance in relation to conventional CMOS decoders. Furthermore, four new 4–16 line decoder topologies were presented, namely 4–16LP, 4–16LPI, 4–16HP and 4–16HPI, realized by using the mixed-logic 2-4 decoders as predecoding circuits, combined with postdecoders implemented in static CMOS to provide driving capability. A variety of comparative spice simulations was performed at 32 nm, verifying, in most cases, a definite advantage in favor of the proposed designs. The 2–4LP and 4–16LPI topologies are mostly suitable for applications where area and power minimization is of primary concern. The 2–4LPI, 2–4HP, and 2–4HPI, as well as the corresponding 4–16 topologies (4–16LP, 4–16HPI, and 4–16HP), proved to be viable and all-around efficient designs; thus, they can effectively be used as building blocks in the design of larger decoders, multiplexers, and other combinational circuits of varying performance requirements. Moreover, the presented reduced transistor count and lowpower characteristics can benefit both bulk CMOS and SOI designs as well. The obtained circuits are to be implemented on layout level, making them suitable for standard cell libraries and RTL design.

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