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IMPLEMENTATION OF REVERSIBLE COMBINATIONAL MULTIPLXERS USING REVERSABLE GATES

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ABSTRACT

Reversible rationale has introduced itself as a conspicuous innovation which assumes a basic job in quantum computing. Quantum registering gadgets hypothetically work at ultra fast and expend imperceptibly less power. Research done in this paper means to use the possibility of reversible rationale to break the traditional speed-control exchange off, along these lines getting a bit nearer to acknowledge Quantum registering gadgets.

To verify this examination, different combinational and successive circuits are executed, for example, a 4-bit Ripple-convey Adder, (8-bit X 8-bit) Wallace Tree Multiplier, and the Control Unit of a 8-bit GCD processor utilizing Reversible doors. The power and speed parameters for the circuits have been shown, and contrasted and their traditional non-reversible partners. The near factual investigation demonstrates that circuits utilizing Reversible rationale in this way are quicker and control proficient. The outlines displayed in this paper were recreated utilizing Microwind.

I. INTRODUCTION

MUTLIPLEXER:

Multiplexer means many into one. A multiplexer is a circuit used to select and route any one of the several input signals to a signal output. An simple example of an non electronic circuit of a multiplexer is a single pole multi position switch.

Multi position switches are widely used in many electronic circuits. However circuits that operate at high speed require the multiplexer to be automatically selected. A mechanical switch cannot perform this task satisfactorily. Therefore, multiplexer used to perform high speed switching are constructed of electronic components.

Multiplexer handle two type of data that is analog and digital. For analog application, multiplexer are built of relays and transistor switches. For digital application, they are built from standard logic gates.

The multiplexer used for digital applications, also called digital multiplexer, is a circuit with many input but only one output. By applying control signals, we can steer any input to the output. Few types of multiplexer are 2-to-1, 4-to-1, 8-to-1, 16-to-1 multiplexer.

Following figure shows the general idea of a multiplexer with n input signal, m control signals and one output signal.

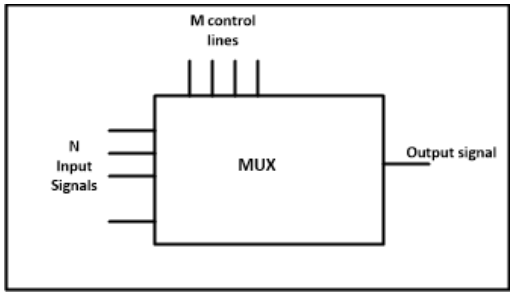


Fig 1.Multiplexer Pin Diagram

Advantages of multiplexer:

- Mux makes the transmission circuit economical and less complex
- Analog switching current is low of order 10mA-20mA. Due to such a low magnitude of the current, the heat dissipation is very low

DE-MULTIPLEXER:

De-multiplexer means one to many. A de-multiplexer is a circuit with one input and many output. By applying control signal, we can steer any input to the output. Few types of de-multiplexer are 1-to 2, 1-to-4, 1-to-8 and 1-to 16 de-multiplexer.

Following figure illustrate the general idea of a de-multiplexer with 1 input signal, m control signals, and n output signals.

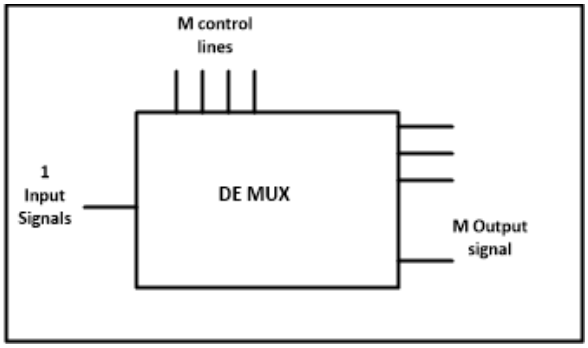


Fig 2. De-multiplexer Pin Diagram

Advantages of de-multiplexer:

De-multiplexer is used to separate the combined signals back into individual streams.

II. LITERATURE SURVEY

The present proposal means to add some new plans to the current information of amalgamation, streamlining, testing and utilizations of reversible circuits and quantum circuits. It is a fascinating and spurring subject since in later past reversible calculation has developed as a promising innovation having applications in low power CMOS, nanotechnology, optical registering, optical data preparing, DNA figuring, bioinformatics, advanced flag handling and so on. To build up the importance of reversible and quantum processing it would be justified to take note of that the VLSI business is moving at fast towards scaling down. With scaling down it faces two issues:

i) A lot of vitality gets disseminated in VLSI circuits
ii) The extent of the transistors are moving toward quantum limits where burrowing and other quantum marvels are probably going to show up. Therefore we require an unrivaled innovation that can beat these issues. Before we chat on the arrangement of the rest issue we might want to say few words in regards to a specific reason for control dispersal. In the traditional circuits, the rationale components are typically irreversible in nature and as indicated by Landauer's standard figuring with irreversible rationale results in vitality scattering.

III. EXISTING SYSTEM

3.1 REVERSIBLE LOGIC:

Boolean rationale is said to be reversible if the arrangement of information sources mapped have an equivalent number of yields mapped i.e. they have coordinated correspondence. This is acknowledged utilizing reversible entryways in the plans. Any circuit having just reversible doors is equipped for scattering no power.

R-gate is a 3x3 gate as shown in Fig.3. It has three inputs (A, B, C) and three outputs (P, Q, and R). The output is defined as P=A, Q=AB, R=A'B+AC having quantum cost of 4.

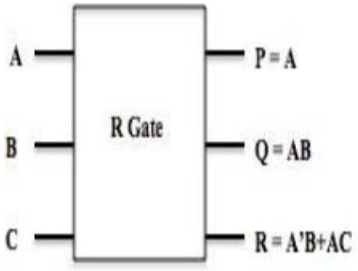


Fig.3.1 Block diagram of R gate

The truth table for particular gate is shown in table1 which maintains principle of reversibility. The advantages of R gate over other existing reversible gates lie in terms of quantum cost, garbage output, quantum depth and constant inputs and number of quantum gates.

3.2. FUNDAMENTAL THOUGHT OF BLAME MODELS AND TEST VECTORS:

Quantum circuits can be inclined to different sort of issues. Therefore, it is critical to confirm whether the circuit equipment is blemished or not. The methodical system to do as such is known as blame

testing. In customary reversible circuits testing is finished by giving an arrangement of legitimate info states and estimating the relating yield states and contrasting the yield states and the normal yield conditions of the ideal (blame less) circuit. This specific arrangement of information vectors are known as test set. In the event that there exist blame then the subsequent stage would be to end the correct area and the idea of the blame. This is known as blame confinement. A model that clarifies the legitimate or utilitarian blames in the circuit is a called blame model. Customary blame models incorporate (I) stuck at issues, (ii) connect issues and (iii) defer shortcomings. These blame models have been thoroughly examined for customary irreversible circuit. In any case, with the approach of reversible established processing and quantum figuring it has turned out to be imperative to amplify the area of the examination on test vectors. In the ongoing past individuals have understood this reality and have endeavored to give great reversible blame models which are autonomous of specific innovation. The current reversible blame models are

1. Single missing door blame (SMF) where a solitary entryway is absent in the circuit.

2. Different missing door blame (MMF) where numerous entryways are absent in the circuit.

3. Rehashed door blame (RGF) where same entryway is rehashed continuously commonly.

4. Incomplete missing door blame (PGF) which can be comprehended as an imperfect entryway.

5. Cross point blame where the control focuses vanish from an entryway or undesirable control focuses show up on other door.

6. Stuck to blame model which incorporates single stuck to blame (SSF) and numerous stuck to blame (MSF) for zero and one separately.

3.4 MULTIPLEXER USING R-GATE

Reversible multiplexer (MUX) is required to select certain inputs form various input source. we have presented a design of 4:1 multiplexer and de-multiplexer using R gate instead of FRG gate and improvement is achieved in terms of delay, quantum cost, number of gates, and garbage output and quantum depth over the existing best one. The design of 4:1 MUX has 2 selection lines (S0, S1)and4 input lines (I0,I1,I2,I3) requires three R reversible gates and output variable is denoted by Z. The design of4:1 multiplexer is shown in Fig.3.4 below. The reversible circuit requires total quantum cost of 12 as compared to15 quantum cost in the existing.

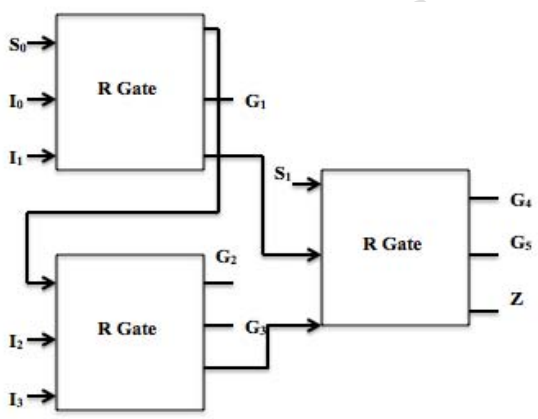


FIG : 3.4x1 MULTIPLEXER USING R-GATE

3.5 DE-MULTIPLEXER USING R-GATE

On the other hand, De-multiplexer (DEMUX) is the reverse of multiplexer. It is a device, which is taking a single input signal and selecting one of many output data lines, which is connected to the single input. 1:4 De-multiplexer design by using R-gate has been proposed has one data input I, two select lines(S0,S1) and four outputs(Z0,Z1,Z2,Z3), is shown in Fig. 3.5.

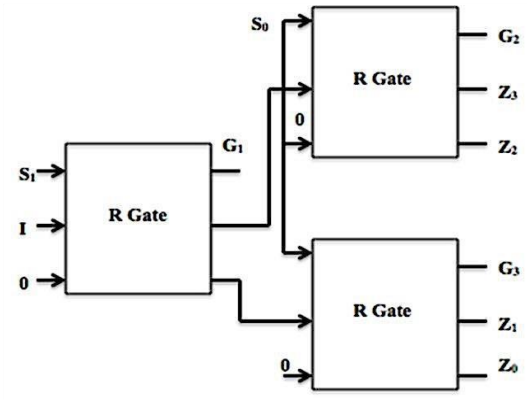


FIG 4: 1x4 DE-MULTIPLEXER USING R-GATE

Design can be extended up to nx1 multiplexer and vice versa.

III. PROPOSED SYSTEM

The Reversible Logic includes the utilization of Reversible Gates comprises of a similar number of sources of info and yields i.e., there ought to be balanced mapping between input vectors and yield vectors. What's more, they can be made to run reverse way too. Certain impediments are to be considered when planning circuits in view of reversible rationale

(I) Fan out isn't allowed in reversible rationale and

(ii) Feedback is likewise not allowed in reversible rationale. In Reversible rationale utilizing yields we can get full learning of information sources. Reversible rationale moderates data.

Some cost measurements like Garbage yields, Number of doors, Quantum cost, consistent sources of info are utilized to evaluate the execution of reversible circuits. Junk yields are the additional yields which help to make data sources and yields measure up to keeping in mind the end goal to look after reversibility. They are kept alone without playing out any tasks. Number of entryways check is certainly not a decent metric since more number of doors can be taken together to shape another door.

Quantum Cost is the quantity of basic or crude entryways expected to actualize the door. It is only the quantity of reversible doors (1×1 or 2×2) required to develop the circuit. Postponement is one of the vital cost measurements. A Reversible circuit configuration can be demonstrated as an arrangement of discrete time cuts and profundity is summation of aggregate time cuts. In Digital Electronics the twofold decoder is a combinational rationale circuit that believers the parallel number an incentive to the related yield design. Different recommendations are given to outline of combinational and successive circuits in the experiencing research.

Boolean justification is said to be reversible if the course of action of sources of info mapped have a comparable number of yields mapped i.e. they have composed correspondence. This is recognized using reversible passages in the plans. Any circuit having quite recently reversible entryways is fit for dispersing no power.

DESTINATIONS OF REVERSIBLE LOGIC:

A. Quantum Cost: Quantum cost of a circuit is the proportion of utilization cost of quantum circuits. Simply more precisely, quantum cost is described as the amount of simple quantum activities anticipated that would comprehend a gateway.

B. Speed of Computation: The time delay of the circuits should be as low as could sensibly be normal as there are different estimations that must be done in a structure including a quantum processor; thusly speed of count is a fundamental parameter while examining such systems.

C. Squander Outputs: Garbage yields are those yield signals which don't contribute in driving further squares in the arrangement. These yields get the chance to be overabundance as they are not required for figuring at a later stage. The garbage yields make the structure slower; consequently for better efficiency it is critical to limit the amount of junk yields.

D. Information: Looping is completely denied when arranging reversible circuits.

E. Fan-out: The yield of a beyond any doubt square in the arrangement can simply drive at most one piece in the blueprint.

There are various reversible entryways, for instance, Feynman, Toffoli, TSG, Fredkin, Peres. As the general passages in Boolean method of reasoning are Nand and Nor, for reversible justification, the comprehensive entryways are Feynman and Toffoli doors.

Feynman Gate: Feynman portal is a general entryway which is used for sign copying purposes or to obtain the supplement of the data flag.

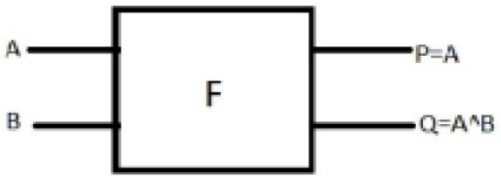


Fig .5: Feynman Gate

Fredkin Gate: It is an essential reversible 3-bit door utilized for swapping keep going two bits relying upon the control bit. The control bit here is A, contingent upon the estimation of A, bits B and C are chosen at yields Q and R. Whenever A=0, (Q=B, R=C) though when A=1, (Q=C, R=B). Its square graph is as appeared in fig. 2:

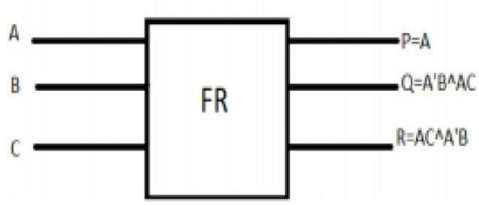


Fig .6: Fredkin Gate

Multiplexer using fredkin gate:

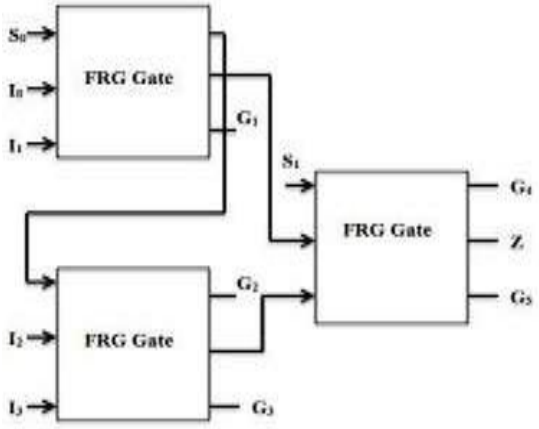


Fig .7: Multiplexer using fredkin gate

Peres Gate: It is a fundamental reversible entryway which has 3-sources of info and 3-yields having inputs (A, B, C) and the mapped yields (P=A, Q=A^B, R=(A.B)^C). The square graph is as appeared in fig. 3

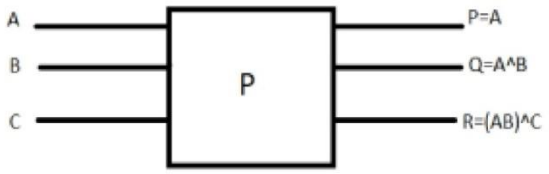


Fig .8: Peres Gate

Toffoli Gate: Toffoli entryway is an all inclusive reversible door which has three data sources (A, B, C) mapped to three yields (P=A, Q=B, R= (A.B)^C). The square graph of Toffoli door is appeared in fig. 4

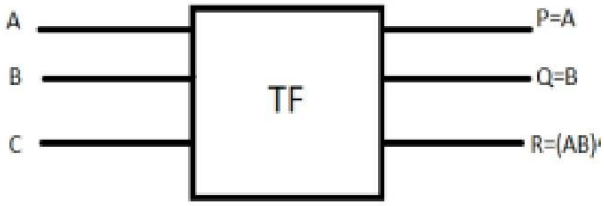


Fig .9: Toffoli Gate

TSG Gate: TSG door is a reversible entryway which has four information sources (A, B, C, D) mapped to four yields (P=A, Q=A^B, R=A^B^D, S=(A^B)^D^AB^C). The square chart of TSG Gate is appeared in fig. 5

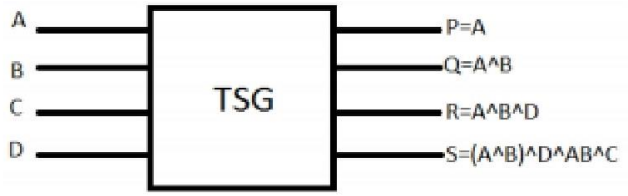


Fig .10: TSG Gate

REVERSIBLE N- BIT FULL ADDER/SUBTRACTOR:

The entryway utilized as a part of actualizing a reversible swell conveys full viper is the TSG door. The TSG entryway capacities like a full snake. A reversible swell convey snake is speedier than the non-reversible viper, since the calculation of convey in a reversible snake does not require the calculation of past stage convey (as showed in the basic ways). At the point when past stage convey is being sent in the reversible viper, the calculation of past stage convey and calculation with respect to entirety is done at the same time though in an irreversible snake the following stage convey can't begin any calculation till past stage convey is completely created. The basic ways of 4bit reversible and irreversible swell convey adders are as shown in FIG

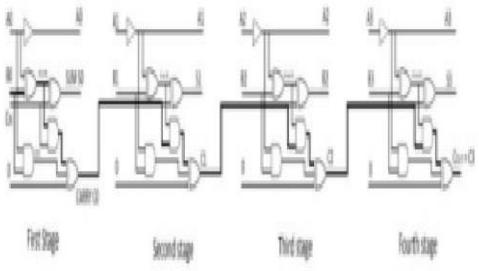


Fig .11: Critical path of 4-bit reversible adder

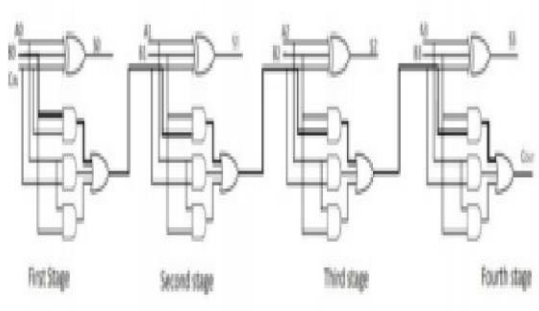


Fig .12: Critical path of 4-bit irreversible adder

Reversible registering was begun when the premise of thermodynamics of data preparing was demonstrated that ordinary irreversible circuits unavoidably create warm in light of misfortunes of data amid the calculation. The distinctive physical wonders can be misused to develop reversible circuits keeping away from the vitality misfortunes. A standout amongst the most alluring engineering prerequisites is to manufacture vitality lossless little and quick quantum PCs. A large portion of the entryways utilized in computerized configuration are not reversible for instance NAND, OR and EXOR doors.

A Reversible circuit/entryway can produce special yield vector from each information vector, and the other way around, i.e., there is a coordinated correspondence between the info and yield vectors. Hence, the quantity of yields in a reversible entryway or circuit has the same as the quantity of data sources, and regularly utilized conventional NOT door is the main reversible entryway. Every Reversible door has an expense related with it called Quantum cost. The Quantum cost of a Reversible door is the quantity of 2*2 Reversible entryways or Quantum rationale doors required in outlining. A standout amongst the most critical highlights of a Reversible door is its junk yield i.e., each contribution of the entryway which isn't utilized as contribution to other door or as an essential yield is called waste yield.

In computerized outline vitality misfortune is considered as an imperative execution parameter. Some portion of the vitality dissemination is identified with non-ideality of switches and materials. More elevated amounts of joining and new creation forms have significantly lessened the warmth misfortune in the course of the most recent decades. The power 2 dissemination in a circuit can be decreased by the utilization of Reversible rationale. Landauer's standard expresses that irreversible calculations creates warmth of K*Tln2 for all of data lost, where K is Boltzmann's consistent and T the outright temperature at which the calculation performed. Bennett demonstrated that if a calculation is done in Reversible rationale zero vitality dissemination is conceivable, as the measure of vitality dispersed in a framework is specifically identified with the quantity of bits eradicated amid calculation. The outline that does not result in data misfortune is irreversible.

Arrangements of reversible entryways are expected to plan reversible circuit. A few such entryways are proposed over the previous decades. Math circuits, for example, Adders, Subtractors, Multipliers and Dividers are the fundamental squares of a Computing framework. Devoted Adder/Subtractor circuits are required in various Digital Signal Processing applications. A few plans for twofold Adders and Subtractors are researched in light of Reversible rationale. Minimization of the quantity of Reversible entryways, Quantum cost and refuse inputs/yields are the focal point of research in Reversible rationale.

Reversible half Adder/Subtractor– Design III is executed with three Reversible entryways of which two are FG doors each having Quantum cost of one and a PG entryway with Quantum cost four is as appeared in the Figure 15. The quantities of Garbage yields is two i.e., g1 and g2, Garbage inputs are one meant by consistent zero and Quantum Cost is six.

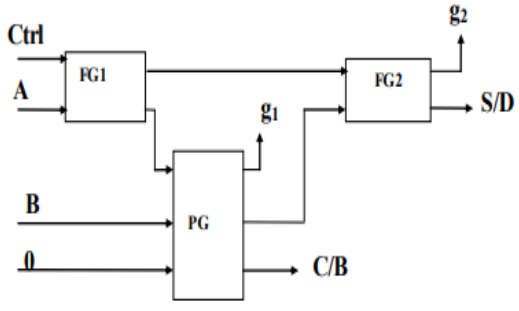


Fig 13: Reversible Half Adder/Subtractor

The Reversible Full Adder/Subtractor Design III comprises of two FG, two PG entryways, and their interconnections are appeared in the Figure 4.2.3. The three data sources are A, B, and Cin, The yields are S/D and C/B. For Ctrl esteem zero the circuit performs expansion and Subtraction for Ctrl esteem one. The quantities of Garbage inputs are 1 spoken to by legitimate zero. The Garbage yields are 3 spoken to by g1 to g3. The Quantum Cost for the outline is 10. A Quantum Cost favorable position of 11 is acquired when contrasted with Adder/Subtractor Design I and of 4 when contrasted with Adder/Subtractor Design II. Quantum Cost advantage is because of the acknowledgment of Arithmetic squares utilizing two PG doors as against two F and one TR entryway for Design I and two TR entryways for Design II.Figure16. Reversible Full Adder/Subtractor – Design III

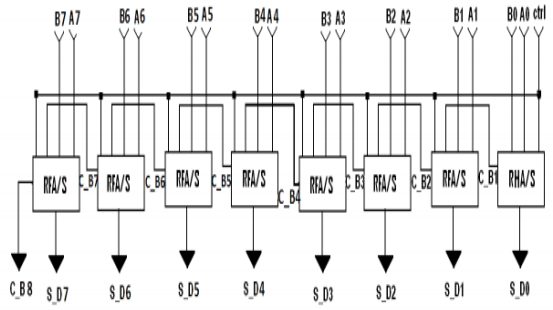


Fig 14: Reversible Eight-bit parallel Binary Full Adder/Subtractor

The Half and Full Adder/Subtractor Design I, Design II and Design III are utilized to develop Reversible eight-piece Parallel Binary Adder/Subtractor is appeared in the Figure 4.2.4 . The ctrl input is utilized to separate eight-piece expansion and subtraction capacities. The two eight-piece twofold numbers are A0 to A7 and B0 to B7. Convey/Borrow is gotten after Addition/Subtraction is spoken to by C_B1 to C_B7. The yields Sum/Difference and Carry are appeared as S_D0 to S_D7 and C_B8 individually. The execution requires seven Full Adder/Subtractor units and one half Adder/Subtractor units in which first stage is half Adder/Subtractor.

DECODER:

The Design of Combinational and Sequential Circuits has been progressing in look into. Different recommendations are given for the plan of combinational circuits like adders, subtractors, multiplexers, decoders and so forth., in the current strategy the creator has given a novel outline of 4x16 decoder whose Quantum Cost is not as much as the past plan. Swapping fredkin doors for planning 2×4 decoder reversible entryways like peres door, TR door, NOT door and CNOT door are utilized as appeared in figure4.4. The entire outline is finished utilizing Fredkin, CNOT, Peres entryways which give better Quantum Cost when contrasted with the other reversible Logic doors.

The quantity of doors required to plan 4x16 decoder are 18 in which there are 12 fredkin entryways, one peres entryway, one TR entryway, one NOT entryway and 3 CNOT entryways. The entirety of all the quantum expenses of each door gives add up to quantum cost of 4x16 decoder. Diverse Reversible Decoder circuits like 2×4, 3×8, 4×16 are planned utilizing Fredkin Gates (basically), Feynman entryways and Peres door. Some combinational circuits like comparator viper, subtractor, multiplexers and so forth, are outlined utilizing these decoders.

The idea of copying a solitary yield to required number of yields utilizing Feynman door is presented where Fan-out was not permitted in reversible calculation.

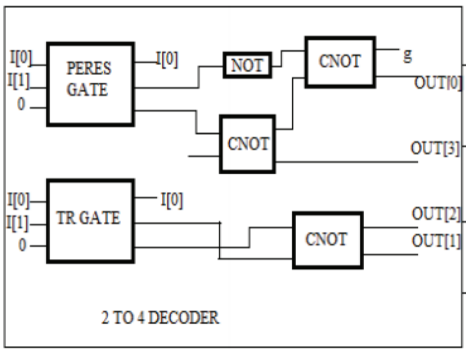
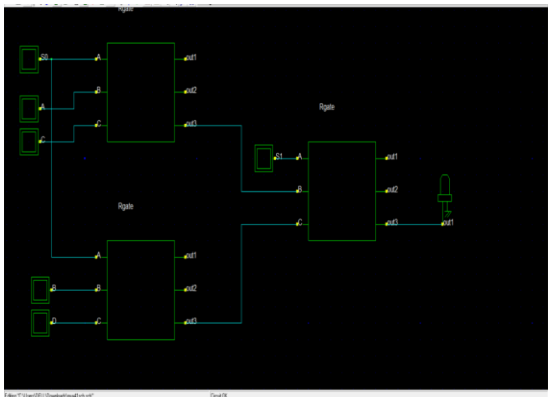


Fig 15: 2x4 Decoder using reversible gate

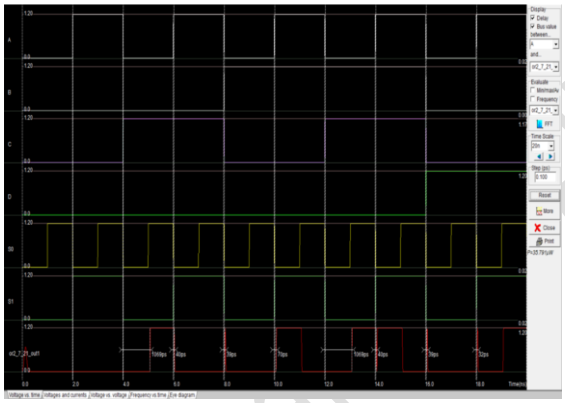
IV. RESULTS

MULTIPLEXER USING REVERSIBLE GATE

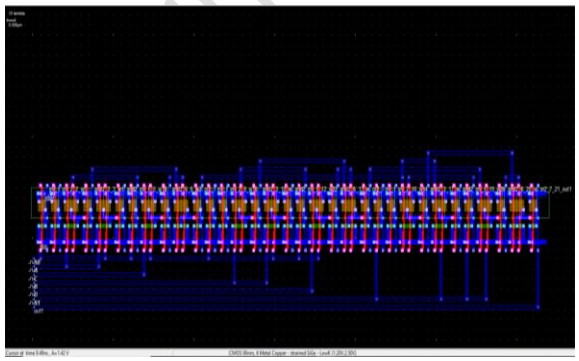
The multiplexer using reversible gate with its timing diagram and layout are shown in fig 6.1, 6.2, 6.3 respectively.



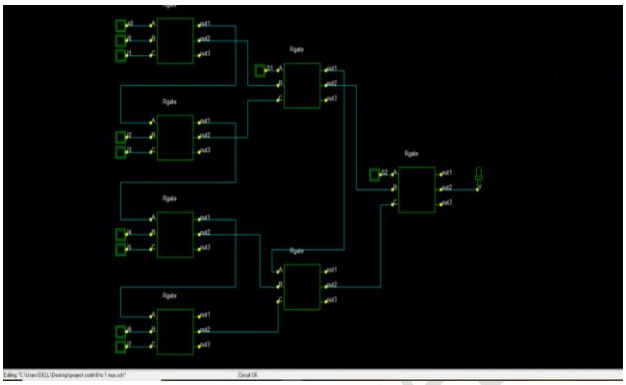
Multiplexer using Reversible gate



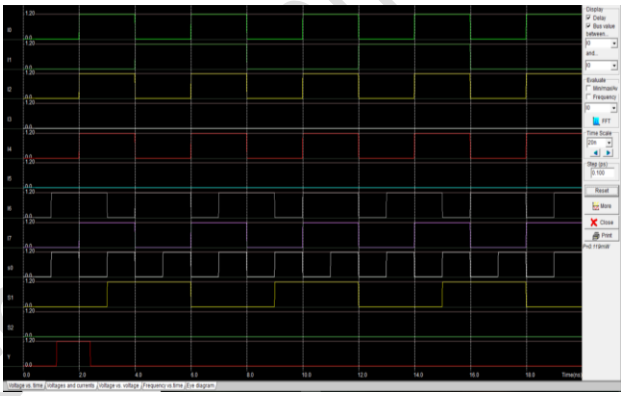
Output waveform



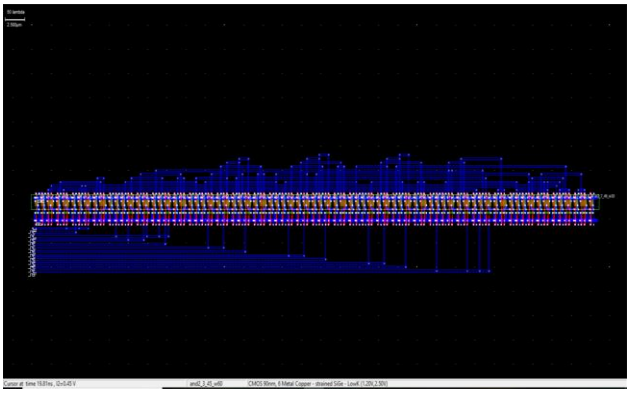
Layout Diagram



8x1 Multiplexer



Output Waveform



Layout Diagram

DE-MULTIPLEXER USING REVERSIBLE GATE

The de-multiplexer using reversible gate with its timing diagram and layout are shown in fig 6.7, 6.8, 6.9, 6.8, 6.9, 6.10,6.11, 6.12 respectively.

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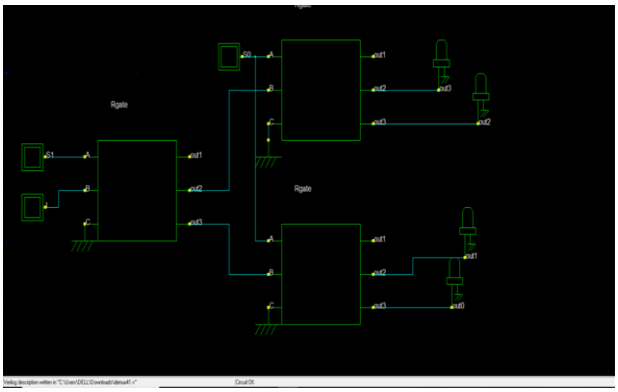
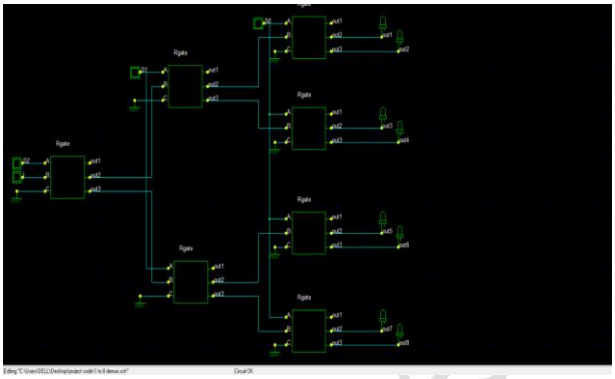
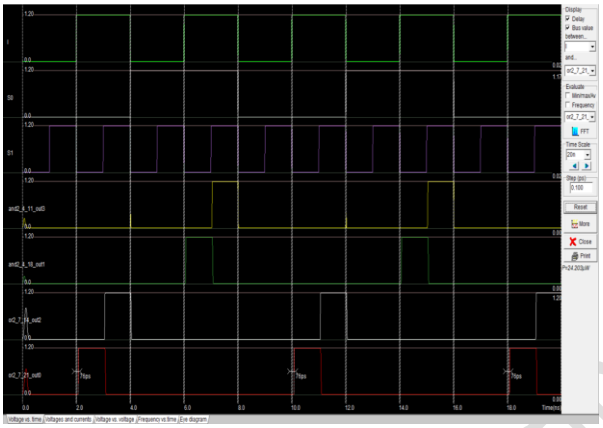


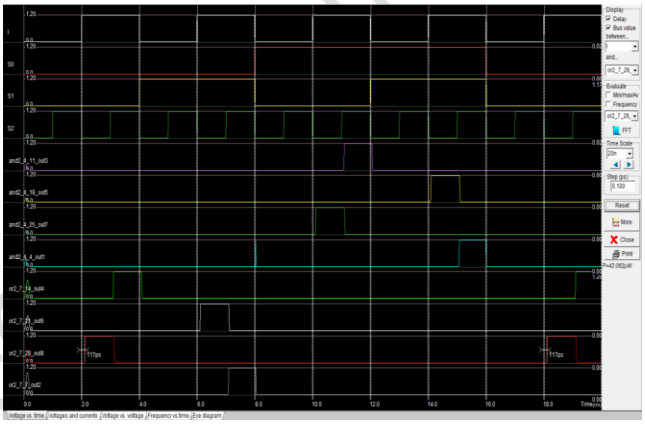
1x4 De-multiplexer using reversible gate



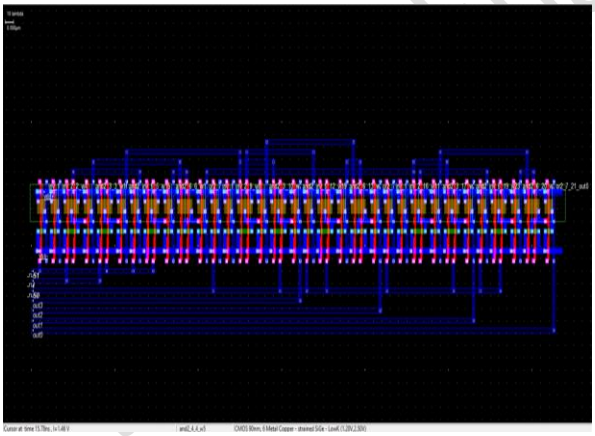
1x8 De-multiplexer using R-gate



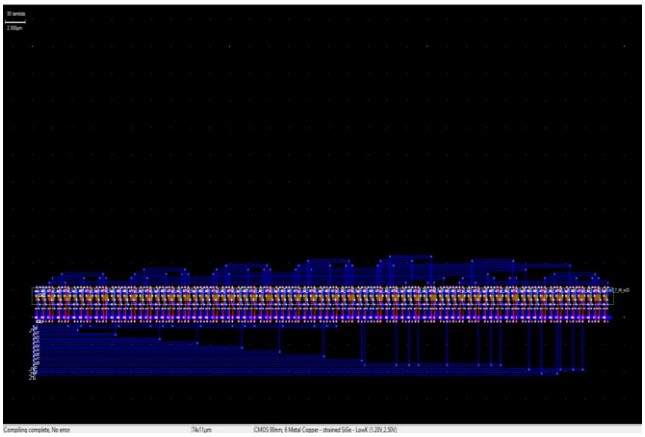
Output Waveform



Output waveform



Layout Diagram



Layout Diagram

DISCUSSION

The proposed multiplexer and de-multiplexer using R-gate is compared with the conventional circuit at 90 nm technology as shown in table 6.1. The proposed circuit is extended to 4x1 mux, de-mux 8x1 mux, demux and the parameters

PARAMRTER	EXISTING	PROPOSED
Power	0.509 mw(509uw)	70.64 uw
Delay	13ns	11.94ns
Current	1.4ma	1.1 ma
Voltage	1.19v	1.12v
Temperature	31ºc	27ºc

such as power, delay current, voltage, temperature is calculated and compared with the conventional mux and de-mux. From this analysis the proposed circuit provides less power.

Table 1: Simulation results at 90nm technology

2 T0 1 MUX AND DEMUX

PARAMRTER	EXISTING	PROPOSED
Power	0.201 mw(201uw)	11.264 uw
Delay	6ns	4.894ns
Current	1.234ma	0.987ma
Voltage	1.17v	1.14v
Temperature	31ºc	27ºc

4 T0 1 MUX AND DEMUX

PARAMRTER	EXISTING	PROPOSED
Power	0.34 mw(340uw)	43.46 uw
Delay	7.2ns	6. 914ns
Current	1.21ma	0.887ma
Voltage	1.18v	1.13v
Temperature	31ºc	27ºc

8 T0 1 MUX AND DEMUX

APPLICATIONS

Reversible rationale configuration discovers applications in different fields including Quantum figuring, Nano-registering, optical processing, Quantum Computing Automata (QCA: investigation of scientific items considered Abstract machines and the computational issues that can be settled utilizing them), ultra-low power VLSI outlining, Quantum speck cell and so forth. The eventual fate of PC chips is constrained by Moore's law; subsequently an option is to construct quantum chips. Our future research theme is outlining another reversible entryway and to actualize reversible rationale into a total Quantum processor equipped for ultra-fast and imperceptibly low power figuring.

ADVANTAGES

- The gate must run forward and backward that is the inputs can also be retrieved from outputs.
- When the device obeys these two conditions then the second law of thermo-dynamics guarantees that it dissipates no heat. Fan-out and Feed-back are not allowed in Logical Reversibility.
- Reversible Logic owns its applications in various fields which include Quantum Computing, Optical Computing, Nanotechnology, Computer Graphics, low power VLSI Etc., Reversible logic is gaining its own importance in recent years largely due to its property of low power consumption.

V. CONCLUSION

In this venture, it tends to be seen that the execution of computerized circuits can be upgraded utilizing reversible entryways and have thought about 8-bit swell convey reversible snake with an irreversible viper regarding velocity and power; subsequently inferring that reversible plans are quicker and control proficient. Moreover, this idea is reached out to combinational circuits, for example, a Wallace tree multiplier utilizing reversible

entryways, which were mimicked and separate outcomes approve earlier surmising. At that point a reversible consecutive control unit of a GCD processor was outlined. In this manner, every one of the outlines executed was contrasted and their irreversible partners and the speed and power parameters for the reversible plans were seen to have enhanced essentially.

In this venture, diverse combinational circuits like full viper, full subtractor, multiplexer, comparator circuits built utilizing reversible decoder are outlined. These circuits are intended for least quantum cost and least junk yields. The technique proposed for outlining the decoder circuit can be summed up. For instance, a 3×8 decoder can be planned utilizing a 2×4 decoder taken after by 4 fredkin doors, Similarly a 4×16 decoder can be outlined utilizing 3×8 decoder taken after by 8 fredkin entryways .The idea of copying the single yield to required number of yields is used to beat the fan-out impediment in reversible rationale circuits. This strategy for planning combinational circuit executes numerous advanced circuits with better execution for least quantum cost.

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