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# REDUCTION OF NOISE MARGIN OF VOLTAGE SWING 8T SRAM CELL FOR LOW POWER APPLICATIONS

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**ABSTRACT**

This project focuses on the DC noise margin analysis and read/write failure analysis of the proposed 8T low power SRAM cell. In the proposed structure two voltage sources, one connected with the Bit line and the other connected with the Bit bar line for reducing the voltage swing during the switching activity. These two extra voltage sources will control the voltage swing on the output node and improve the stability. DC noise margin has been calculated by using loop gain technique and comparison made with that of conventional 6T SRAM justify the efficacy of the superiority of the proposed SRAM structure. Read and Write failure analyses are also done by using DSCH and EXPORT MICROWIND in 90nm and 70 nm technology.

## I. INTRODUCTION

**R**ELIABILITY is one of the biggest challenges facing the microprocessor industry today. With continued technology scaling, processors are becoming increasingly susceptible to hard errors. Hard errors are permanent faults that occur due to the wearing out of hardware structures over time. These failures occur partly due to design-time factors such as process parameters and wafer packaging, as well as runtime factors such as the utilization of the hardware resources and the operating temperature. It is important to ensure that the reliability of the microarchitectural structures in the processor is maximized so that one can make use all the available hardware resources effectively over the entire service life of the chip. One important hard error phenomenon is negative bias temperature instability (NBTI), which affects the lifetime of pMOS transistors. NBTI occurs when a negative bias (i.e., a logic input of "0") is applied at the gate of a pMOS transistor.

The negative bias can lead to the generation of interface traps at the Si/SiO interface, which cause an increase in the threshold voltage of the device. This increase in the threshold voltage degrades the speed of the device and reduces the noise margin of the circuit, eventually causing the circuit to fail [11], [14]. One interesting aspect of NBTI is that some of the interface traps can be eliminated by applying a logic input of "1" at the gate of the pMOS device. This puts the device into what is known as the recovery mode, which has a "self-healing" effect on the device [1]. Memory arrays that use static random access memory (SRAM) cells are especially susceptible to NBTI. SRAM cells consist of cross-coupled inverters that contain pMOS devices. Since each memory cell stores either a "0" or a "1" at all times, one of the pMOS devices in each cell always has a logic input of "0." Since modern processor cores are composed of several
critical SRAM-based structures, such as the register file and the issue queue, it is important to mitigate the impact of NBTI on these structures to maximize their lifetimes.

**Previous work**

Previous work on applying recovery techniques to SRAM structures aim to balance the degradation of the two pMOS devices in a memory
cell by attempting to keep the inputs to each device at a logic input of "0" exactly 50% of the time .However, one of the devices is always in the negative bias condition at any given time. In this paper, we propose a novel technique called *Recovery Boosting* that allows *both* pMOS devices in the memory cell to be put into the recovery mode. The basic idea is to raise the ground voltage and the bitlines to when the cell does not contain valid data. The main contributions of this paper are given here. • We describe how SRAM cells can be modified to support recovery boosting and discuss several circuit and microarchitecture- level design considerations when using such cells to build SRAM arrays.

• We present the circuit-level design of two large SRAM arrays in a four-wide issue processor core—

the physical register file and the issue queue—that use the modified cells to provide recovery boosting. We verify the functionality of these designs and quantify their area and power consumption through SPICE-level simulation using the Cadence Virtuoso Spectre Circuit Simulator1 for the 32-nm process technology. We show that the modified SRAM structures impose only a 3%–4% area overhead over the baseline non recovery boost designs and that their maximum power consumption is less than 2% over the baseline.

• We then evaluate the performance and reliability of areaneutral designs of these modified structures at the architecture- level via execution-driven simulation using the M5

## II. LITERATURE SURVEY

This Chapter describes various attempts made by investigators to reduce the power dissipation in SRAM or to develop low power and energy efficient SRAM. These investigations cover SRAMs operated at low voltages reducing power dissipation, SRAMs using techniques like power gating in which the circuits are switched off when they are not needed , SRAMs (drowsy) where the power supply voltage is reduced to a lower value during standby mode and SRAMs based on adiabatic techniques. Lowering the power supply voltage reduces the dynamic power quadratic ally and leakage power exponentially. But power supply voltage scaling also limits signal swing and thus reduces noise margin. Further, aggressive technology scaling in the sub-100nm region increases the sensitivity of the circuit parameters to process variation (PV). Leakage currents are mainly due to gate leakage current and sub threshold leakage current. High K gate technology decreases the gate leakage current. Forward body biasing methods and dual Vt techniques are used to reduce sub threshold leakage current. In sub-threshold SRAMs, power supply voltage (VDD) is lower than the transistor threshold voltage (Vt) and the sub threshold leakage current is the operating current.

Tae-Hyoung Kim et. al [14] introduced various circuit techniques for designing robust high-density sub threshold SRAMs: (i) decoupled cell for read margin improvement, (ii) utilizing reverse short channel effect (RSCE) for write margin improvement, (iii) eliminating data- dependent bit line leakage to enable long bit lines, (iv) virtual ground replica scheme for improved bit line sensing margin, (v) write back scheme for data preservation during write, and (vi) optimal gate sizing based on sub threshold logical effort. To achieve all these operations the authors proposed 10T SRAM cell operating in sub threshold region that has an SNM of 76 mV at a supply voltage of 0.2V while that of a conventional 10T SRAM cell is 14mV.It improves the cell write ability without introducing a separate high VDD. Reverse short channel effect yields further advantages such as better sub threshold slope owing to the longer channel length and reduced impact of random doping fluctuation due to the increased gate area for equal drive current. A SRAM of 480 kb cells was fabricated in 0.13 µm CMOS technology. As per the measured results leakage current consumption is reported to be 10.2 µA at supply voltage equal to 0.20 V at 27 °C.

The normalized virtual ground voltage was found to rise significantly as the supply is reduced and the number of cells per bit line increased (i.e., 50% of VDD at 0.20 V, 1024 cells). A 6% change in virtual ground voltage was measured when the temperature is varied from 27 °C to 80 °C.

Jaydeep P. Kulkarni et.al [15] proposed Schmitt Trigger SRAM cell that incorporates a built-in feedback mechanism, achieving 56 % improvement in SNM, improvement in process variation tolerance lower read failure probability, low-voltage/low power operation, and improved data retention capability at ultra-low voltage compared to conventional 10T SRAM cell. They report that at iso-area and iso-read-failure probability the proposed memory bit cell operates at a lower (175 mV) VDD with 18% reduction in leakage and 50% reduction in read/write power compared to the conventional 10T cell. As per their simulation results, the proposed memory bit cell retains data at a supply voltage of 150 mV. Functional SRAM with the proposed memory bit cell was demonstrated at 160 mV in 0.13µm CMOS technology.

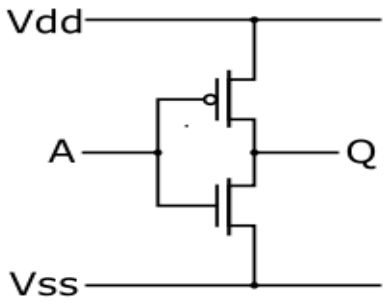
Naveen Verma et.al [16] introduced 8T bit-cell with buffered read which eliminates the read SNM limitation. Added to it the peripheral footer circuitry eliminates bit line leakage. The peripheral write drivers and storage-cell supply drivers designed by the authors interact to reduce the cell supply voltage during write operations. Sense-amp redundancy

provided produces a favorable trade-off between offset and area. The SRAM array built with 45nm technology was found to be functional at 350 mV and data correctly retained at 300 mV.

**III. Existing system**

**3.1.CMOS**

Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors ,microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors, data converters, and highly integrated transceivers for many types of communication. Frank Wanlass patented CMOS in 1967 (US patent 3,356,858). CMOS is also sometimes referred to as complementary-symmetry metal–oxide–semiconductor (or COS-MOS[1]). The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type andn-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.




CMOS inverter (NOT logic gate)

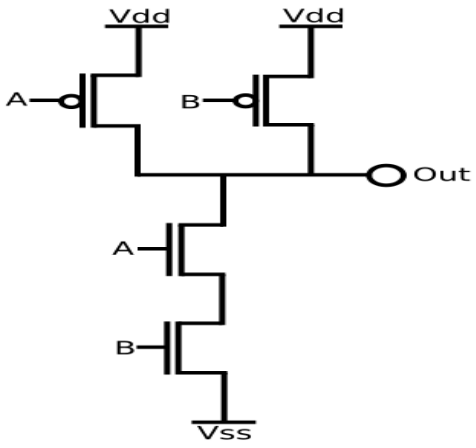
Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Significant power is only drawn while the transistors in the CMOS device are switching between on and off states. Consequently, CMOS devices do not produce as muchwaste heat as other forms of logic, for example transistor-transistor logic (TTL) or NMOS logic, which uses all n-channel devices without p-channel devices. CMOS also allows a high density of logic functions on a chip. It was primarily this reason why CMOS won the race in the eighties and became the most used technology to be implemented in VLSI chips.

The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Aluminum was once used but now the material is polysilicon. Other metal gates have made a comeback with the advent of high-k dielectric materials in the CMOS process, as announced by IBM and Intel for the 45 nanometer node and beyond.

**2.2. CMOS LOGIC**

More complex logic functions such as those involving AND and OR gates require manipulating the paths between gates to represent the logic. When a path consists of two transistors in series, then both transistors must have low resistance to the corresponding supply voltage, modeling an AND. When a path consists of two transistors in parallel, then either one or both of the transistors must have low resistance to connect the supply voltage to the output, modeling an OR.

Shown on the below circuit diagram of a NAND gate in CMOS logic. If both of the A and B inputs are high, then both the NMOS transistors (bottom half of the diagram) will conduct, neither of the PMOS transistors (top half) will conduct, and a conductive path will be established between the output and Vss (ground), bringing the output low.




NAND gate in CMOS logic

If either of the A or B inputs is low, one of the NMOS transistors will not conduct, one of the PMOS transistors will, and a conductive path will be established between the output and Vdd (voltage source), bringing the output high.

An advantage of CMOS over NMOS is that both low-to-high and high-to-low output transitions are fast since the pull-up transistors have low resistance when switched on, unlike the load resistors in NMOS logic. In addition, the output signal swings the full voltage between the low and high rails. This strong, more nearly symmetric response also makes CMOS more resistant to noise.

CMOS Scaling improves transistor density and functionality on a chip. Scaling helps to increase speed and frequency of operation and hence higher performance. At the same time power dissipation increases.

**.CONVENTIONAL 6T AND 11T SRAM CELL**

**A. Conventional 6T SRAM cell**

Figure 1 shows the circuit diagram of a conventional SRAM cell. Word line is used for enabling the access transistors T2 and T5 for write operation [12]. BLand BL lines are used to store the data and its compliment. For write operation one BL is high and the other bit line is on low condition. For writing "0", BL is Low and BL is high. When the word line is asserted high transistor T2 and T3 are on and any charge stored in the BL goes through T2-T3 path to ground. Due to zero value at Q, the T4 transistor is ON and T6 is OFF. So the charge is stored at Q bar line. Similarly in the write "1" operation, BL is high due to this T6 is ON and the charge is stored on theQis discharged through the T5-T6 path and due to this low value on theQ, T1 is ON and T3 is OFF, so the charge is stored on the Q.

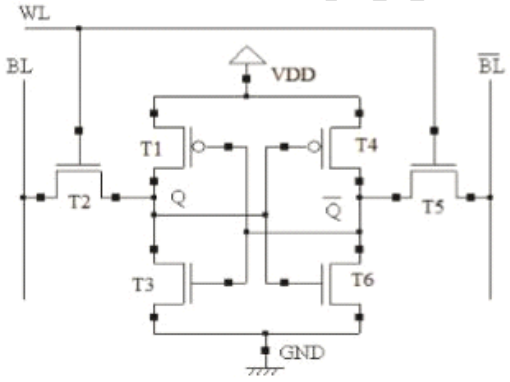



Figure 1. Conventional 6T SRAM cell.

Figure 1. Conventional 6T SRAM cell.

B. 11T SRAM cell An 11T SRAM cell is shown in Figure 2. The circuit consists of two cross coupled inverters along with an access transistor (N5) which is controlled by the read word line (RWL) for read operation and two more access transistors (N3 and N4) which are controlled by the write word line (WWL) for write operation [13]. Two other NMOS transistors, N6 and N8 are used during the read operation to reduce power dissipation while NMOS transistors, N7 and N9 are used during the write operation to reduce power dissipation of the cell. The two tail transistors, N7 and N9 are controlled by the bit lines, BLB and BL, respectively, while the read operation uses a single bit line RBL.

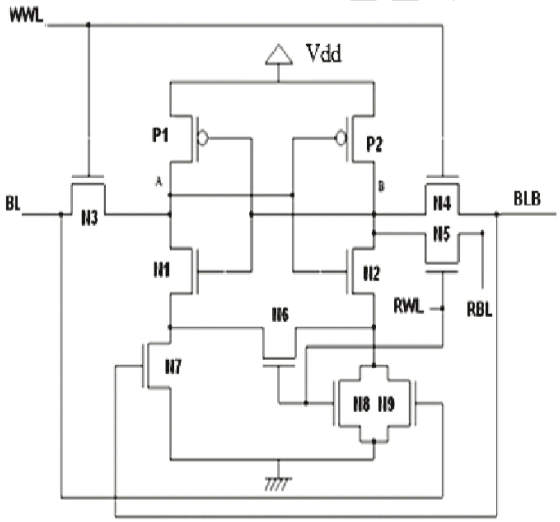



Figure 2. 11T SRAM Cell.

Figure 2. 11T SRAM Cell.

**NEGATIVE BIAS TEMPERATURE INSTABILITY (NBTI)**

Negative bias temperature instability (NBTI) is a key reliability issue in MOSFETs. It is of immediate concern in p-channel MOS devices, since they almost always operate with negative gate-to-source voltage; however, the very same mechanism affects also nMOS transistors when biased in the accumulation regime, i.e. with a negative bias applied to the gate too. NBTI manifests as an increase in the threshold voltage and consequent decrease in drain current and transconductance. The degradation exhibits logarithmic dependence on time.

In the sub-micrometer devices nitrogen is incorporated into the silicon gate oxide to reduce the gate leakage current density and

prevent theboron penetration. However, incorporating nitrogen enhances NBTI. For new technologies (32 nm and shorter nominal channel lengths), high-K metal gate stacks are used as an alternative to improve the gate current density for a given equivalent oxide thickness (EOT). Even with the introduction of new materials like hafnium oxydes, NBTI remains.

It is possible that the interfacial layer composed of nitrided silicon dioxide is responsible for those instabilities. This interfacial layer results from the spontaneous oxidation of the silicon substrate when the HK is deposited. To limit this oxidation, the silicon interface is saturated with N resulting in a very thin and nitrided oxide layer.

It is commonly accepted that two kinds of trap contribute to NBTI:

- first, interface traps are generated. Those traps cannot be recovered over a reasonable time of operation. Some authors refer to them as permanent traps. Those traps are the same as the one created by Channel Hot Carrier. In the case of NBTI, it is believed that the electric field is able to break Si-H bonds located at the Silicon-oxide interface. H is released in the substrate where it migrates. The remaining dangling bond Si- (Pb center) contribute to the threshold voltage degradation.
- on top of the interface states generation some preexisting traps located in the bulk of the dielectric (and supposedly nitrogen related), are filled with holes coming from the channel of pMOS. Those traps can be emptied when the stress voltage is removed. This Vth degradation can be recovered over time.

The existence of two coexisting mechanisms created a large controversy, with the main controversial point being about the recoverable aspect of interface traps. Some author suggested that only interface traps were generated and recovered; today this hypothesys is ruled out. The situation is clearer but not completely solved. Some authors suggest that interface traps generation is responsible for hole trapping in the bulk of dielectrics. A tight coupling between two mechanism may exist but nothing is demonstrated clearly.

With the introduction of High K Metal gates, a new degradation mechanism appeared. The PBTI for Positive Bias Temperature Instabilities affects nMOS transistor when positively biased. In this particular case, no interface states are generated and 100% of the Vth degradation may be recovered. Those results suggest that there is no need to have interface state generation to trapped carrier in the bulk of the dielectric.

## IV. Proposed system

**PROPOSED 8T SRAM CELL**

In order to overcome the problems associated with conventional 6T SRAM, this paper proposes novel 8T SRAM architecture to achieve very low power dissipation. In the proposed design two voltage sources S1 and S2 are used, one connected to the output of the bit line and the other with the bitbar line. Two NMOS transistor VN1 and VN2 are connected with inputs of bit line and bitbar line, respectively, directly to switch ON and switch OFF the power source supply during write “0” and write “1” operations, respectively. The proposed design has been illustrated in Figure 3. These power supply sources reduce the voltage swing at the 'out' node when write operation is being performed.

**A.** Write '0' operation During the write '0' operation, bitline is low and bit bar line goes high. So the transistor VN2 is ON and VN1 goes to the OFF condition. Thus the voltage source S2 forces to decrease the voltage swing at output of the bit bar line. And any charge stored on bitline discharge through the path N5-N1 and “0” is stored on bitline.

**B**. Write '1' operation When the write '1' operation is performed, transistor VN1 is ON and VN2 goes to OFF condition, so the voltage source S1 decreases the voltage swing at the bit line output and any charge stored on the bitbar line discharges through the transistors N6-N2.

Due to the decrease in voltage swing, dynamic power dissipation is almost constant even the frequency of the SRAM cell is increased.

The dynamic power may be expressed as

$$P_{dynamic} = \alpha C V_{dd} V_{Swing} f \quad (1)$$

where C = Load capacitance; α = Activity factor; f = Clock frequency; Swing V = Voltage

swing at output node; Vdd is the power supply voltage.

So, in the conventional VLSI design, as the frequency increases the dynamic power dissipation also increases because the dynamic power depends upon the operating frequency [12].

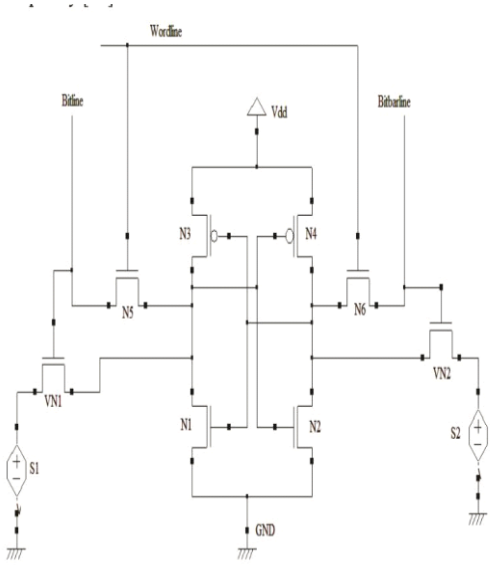



Figure 3. Proposed SRAM Cell.

During switching activity from "0" to "1" or "1" to "0" at bit line or bitbar line, swing voltage is required. This extra voltage increases the dynamic power dissipation. In the proposed 8T SRAM model voltage sources SI and S2 reduce the voltage swing and improve the switching activity during write "0" and write "1" operations. As the frequency increases, the switching activity will also be increased and this will increase the dynamic power dissipation. But voltage source reduces its voltage swing simultaneously at the output. So, at higher frequency the dynamic power dissipation is found to be almost constant. These two voltage sources also provide extra voltage during the write operation on the bit line, bit bar line and word line. This extra voltage will also provide the better noise margin on bit line and word line during write operations.

## IV. STATIC NOISE MARGIN (SNM) ANALYSIS

In this section, the static noise margins of proposed SRAM cell for read and write operation is discussed. The read static noise margins at different cell ratios are calculated. Cell ratio is the ratio between sizes of the driver transistor to the load transistor during the read operation [14]

$$CR = \frac{W / L_{N5}}{W / L_{N_1}} \qquad (2)$$

The write static noise margins at different pull up ratios are also calculated. Pull up ratio is the ratio between sizes of the load transistor to the access transistor during write operation [14].

2

$$PR = \frac{W / L_{N_6}}{W / L_{N_2}} \qquad (3)$$

Table I shows the static noise margins at different cell ratios for read operation. As the cell ratio increases the stability of SRAM also increases.

TABLE I. STATIC NOISE MARGIN VARIATION WITH CELL RATIO

| Cell Ratio | SNM Proposed 8T SRAM (mV) | SNM 11T SRAM (mV) | SNM 6T SRAM (mV) |
|---|---|---|---|
| 0.6 | 289 | 271 | 100 |
| 0.8 | 298.5 | 280 | 102.5 |
| 1.0 | 311.8 | 291 | 104.6 |
| 1.2 | 336.6 | 299 | 107 |
| 1.4 | 349.2 | 308 | 108 |
| 1.6 | 370.4 | 319 | 112 |
| 1.8 | 391.8 | 334 | 116.7 |
| 2.0 | 403.1 | 340 | 123 |

From Figure 4 it is evident that the proposed SRAM has better static noise margin at different values of cell ratios in comparison to both 6T and 11T SRAM cells. In Table II the variation of SNM with pull up ratio for proposed 8T, 11T and 6T has been shown. When the pull up ratio increases the write static noise margin also increases. Figure 5 shows that the proposed SRAM cell has more write stability than the other 6T and 11T SRAM cells.

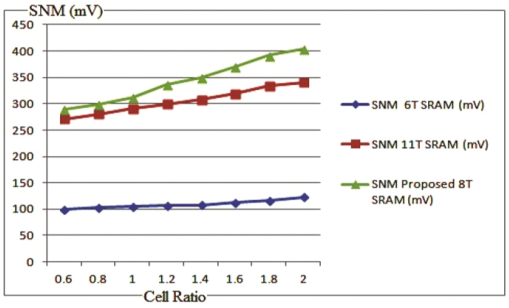



Figure 4. Cell ratio Vs Static Noise Margin.

TABLE II. STATIC NOISE MARGIN VARIATION WITH PULL UP RATIO

| Pull up Ratio | Write SNM Proposed 8T SRAM (mV) | Write SNM 11T SRAM (mV) | Write SNM 6T SRAM (mV) |
|---|---|---|---|
| 1.05 | 252.3 | 241 | 92.9 |
| 1.2 | 253.6 | 242 | 94 |
| 1.4 | 259.1 | 244 | 94.6 |
| 1.6 | 263.4 | 246 | 95 |
| 1.8 | 268 | 249 | 95.5 |
| 2.0 | 272.5 | 250 | 96 |
| 2.1 | 274 | 251 | 96.7 |
| 2.2 | 279.8 | 253 | 97.8 |
| 2.4 | 286.3 | 257 | 99.2 |
| 2.6 | 290 | 259 | 100.4 |
| 2.8 | 295.4 | 260 | 102.3 |
| 3.0 | 301.6 | 262 | 104 |

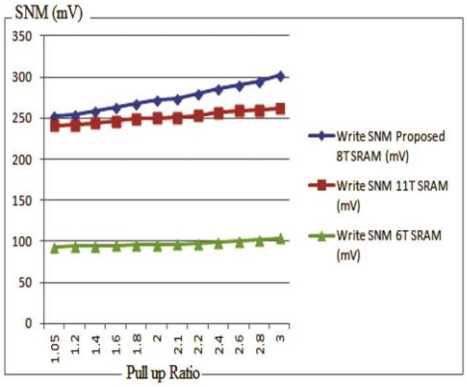



Figure 5. Pull up ratio Vs Static Noise Margin.

## V. POWER DISSIPATION ANALYSIS

The SRAM cell power consumption depends on the transistor widths, threshold voltages, supply voltage and bit line capacitances. In this section, the power analysis of proposed 8T SRAM cell has been done by varying parameters like Temperature, Supply voltage and Bitline capacitance. The results have been compared with those of the conventional 6T and 11T SRAM cells. The power analyzed here is the average power which consists of both static and dynamic powers. Variation of power dissipation with respect to temperature has been shown in Table III.

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Figure 6 shows that as the temperature increases power dissipation also increases. The proposed 8T SRAM cell dissipates less power in comparison to both 6T and 11T SRAM cells as the temperature increases. So, proposed 8T SRAM cell dissipates less power at high temperature.

TABLE III. VARIATION OF POWER DISSIPATION WITH TEMPERATURE

| Temperature ($^0$C) | Proposed 8T SRAM Power dissipation (pW) | 11T SRAM Power dissipation (pW) | 6T SRAM Power dissipation (pW) |
|---|---|---|---|
| 0 | 26.1732 | 39.5402 | 66.5688 |
| 5 | 27.0819 | 40.2024 | 66.4591 |
| 10 | 27.9182 | 41.0517 | 67.9243 |
| 15 | 28.6613 | 42.1322 | 68.0234 |
| 20 | 29.8731 | 43.5032 | 68.8615 |
| 25 | 31.0177 | 45.3026 | 69.7287 |
| 27 | 31.7611 | 46.1243 | 70.5036 |
| 30 | 32.1181 | 47.5201 | 72.9018 |
| 35 | 35.5132 | 50.3854 | 76.0813 |
| 40 | 38.7367 | 54.1782 | 80.9964 |
| 45 | 41.8153 | 59.3794 | 84.2878 |
| 50 | 43.1241 | 66.8385 | 89.2718 |

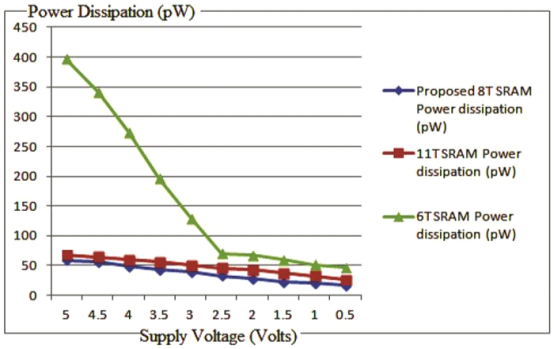



Figure 7. Supply voltage Vs Power dissipation.

Table IV shows the power dissipation variation with supply voltage. As the supply voltage decreases the power dissipation also decreases.

TABLE V. VARIATION OF POWER DISSIPATION WITH CAPACITANCE

| Capacitance (pF) | Proposed 8T SRAM Power dissipation (pW) | 11T SRAM Power dissipation (pW) | 6T SRAM Power dissipation (pW) |
|---|---|---|---|
| 5.0 | 198.67 | 209.4 | 267.9 |
| 4.0 | 151.01 | 167.9 | 240.19 |
| 3.0 | 101.98 | 125.2 | 213.32 |
| 2.0 | 89.11 | 103.7 | 198.82 |
| 1.5 | 70.57 | 85.1 | 174.24 |
| 1.0 | 54.80 | 69.3 | 139.42 |
| 0.8 | 49.23 | 61.5 | 118.45 |
| 0.5 | 42.39 | 55.08 | 99.67 |
| 0.1 | 32.88 | 46.2 | 70.5 |

TABLE IV. VARIATION OF POWER DISSIPATION WITH SUPPLY VOLTAGE

| Supply Voltage (Volts) | Proposed 8T SRAM Power dissipation (pW) | 11T SRAM Power dissipation (pW) | 6T SRAM Power dissipation (pW) |
|---|---|---|---|
| 5.0 | 59.1687 | 68.4357 | 396.5366 |
| 4.5 | 55.8921 | 64.7294 | 340.8164 |
| 4.0 | 49.5612 | 59.6143 | 274.1283 |
| 3.5 | 44.1181 | 55.6481 | 196.2356 |
| 3.0 | 38.8792 | 50.0972 | 129.9901 |
| 2.5 | 33.0132 | 46.1243 | 70.5036 |
| 2.0 | 28.6911 | 42.6591 | 67.3492 |
| 1.5 | 23.0982 | 37.2356 | 59.5460 |
| 1.0 | 20.2561 | 32.8437 | 51.4837 |
| 0.5 | 16.7115 | 26.3189 | 46.8218 |

Fig.shows that 6T SRAM power very sharply reduces with reduction in power supply. This sharp reduction in power dissipation shows the instability of 6T SRAM cell. The proposed SRAM cell dissipates less power at different power supply voltages in comparison to both SRAM cells.

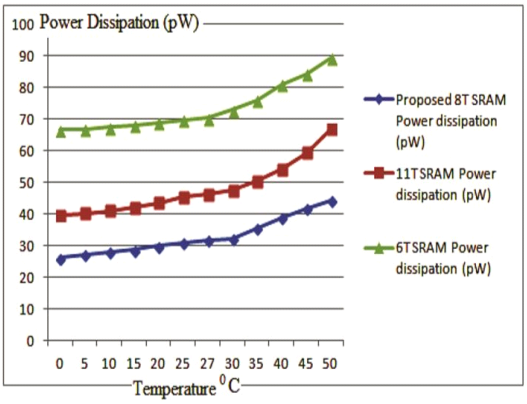



Figure 6. Temperature Vs Power dissipation.

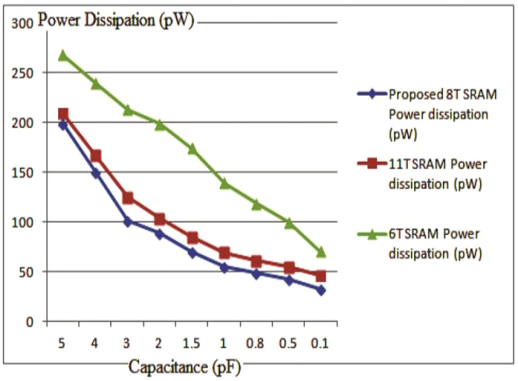


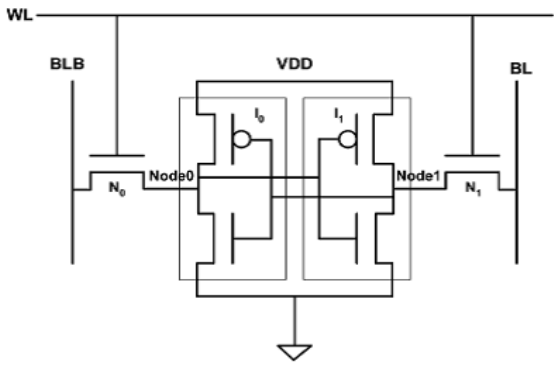

Figure 8. Bit line Capacitance Vs Power dissipation.

Figure 8 shows that proposed 8T SRAM dissipates less power at higher bit line capacitance in comparison to 6T and 11T SRAM cells.

**Loop Gain Technique**

Before we discuss loop gain technique, we first review the design and operation of a conventional 6-transistor (6T) SRAM cell. The design of the 6T cell is given in Fig. 1(a). The cell is composed of a wordline (WL), a pair of bitlines (BL, BLB),

two cross-coupled inverters , and two access transistors . The cross-coupled inverters store one bit of data. There are three basic operations that one can perform on this SRAM cell: read, write and hold. To read and write data, the cell is selected by raising WL to high. This activates the access transistors and connects the inverters in the cell to the bitlines. During a read operation, both bitlines are first precharged high. Based on the data stored in the cell, one of the bitlines is discharged. This change is detected by a sense amplifier (which is not part of the cell) to determine the value stored in the cell. During a write operation, one of the bitlines is raised high and the other is lowered depending on the value to be written to the cell. When the cell is not selected for read or write, it is expected to hold the data stored in it and is said to operate in the hold mode.




Since the SRAM cell has cross-coupled inverters, each inverter charges the gate of the pMOS or nMOS device of the other inverter. Therefore, at any given time, one pMOS device will always be in the stress mode. The goal of recovery enhancement

is to put the pMOS devices into the recovery mode by feeding input values to the cell that will transition them into that mode.

However, due to the cross-coupled nature of the inverters, only one of the pMOS devices can be put into the recovery mode. Therefore, previously proposed recovery-enhancement techniques attempt to balance the wearout of the two pMOS devices by putting each pMOS into the recovery mode 50% of the time by feeding appropriate input values [1], [11], [19].We propose a 6T SRAM cell design shown in Fig. 1(b) which is capable of normal operations (read, write, and hold) as well as providing an NBTI recovery mode (when the cell does not contain valid data) that we call the *recovery boost mode* where both pMOS devices within the cell undergo recovery at the same time. We refer to the period when the cell does not contain valid data that is never used by any other microarchitectural structure in the processor as "invalid period." The basic idea behind recovery boosting is to raise the node voltages (Node0 and Node1 in Fig. 1) of a memory cell in order to put both pMOS devices into the recovery mode.

This can be achieved by raising the ground voltage to the nominal voltage through an external control signal. The modified SRAM cell has the ground connected to the output of an inverter, as shown in Fig. 1(b). CRis the control signal to switch between the recovery boost mode and the normal operating mode. During the normal operating mode, CR has a value of "1" , which in turn connects the ground of the SRAM cell to a value of "0." With this connection, the SRAM cell can perform normal read, write, and hold operations. To apply recovery boosting, CR has to be changed to a "0" in order to raise the ground voltage of the SRAM cell to . This circuit configuration puts both pMOS
devices in the SRAM cell into the recovery mode. A cell can be put into the recovery boost mode regardless of whether its wordline (WL) is high or low. Unlike read and write operations on a cell, putting a cell into the recovery boost mode does not require an access to its wordline. The operations of the modified SRAM cell are shown in Table I.

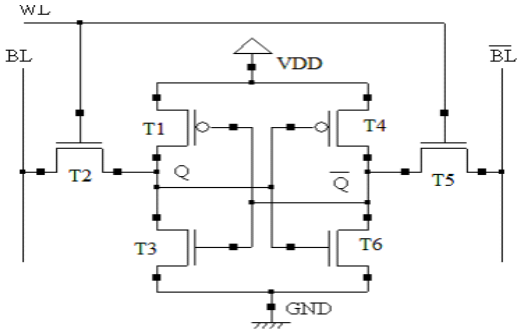



Figure 3. Conventional 6T SRAM cell.

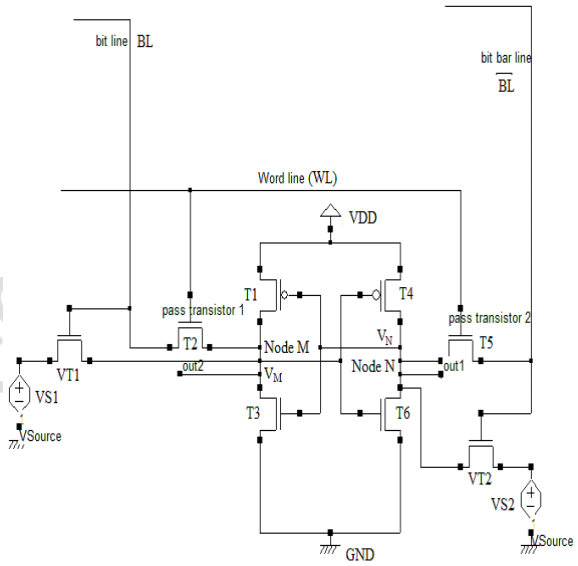



Figure 3. The Proposed 8T SRAM Cell.

TABLE I
MODIFIED SRAM CELL OPERATION

| CR | WL | BL | BLB | Node0 | Node1 | Operation |
|---|---|---|---|---|---|---|
| 1 | 0 | X | X | 0/1 | 1/0 | Hold |
| 1 | 1 | 1 | 1 | 0/1 | 1/0 | Read |
| 1 | 1 | 1 | 0 | 0 | 1 | Write '1' |
| 1 | 1 | 0 | 1 | 1 | 0 | Write '0' |
| 0 | X | X | X | 1 | 1 | Recovery Boost |

However, the drawback of this approach is that it can take a long time to raise both the node voltages to in a high-performance processor that operates at a high clock frequency. This is illustrated in Fig. 2, which presents the achieved pMOS gate voltages of a bitcell over time due to recovery boosting. The simulation is performed using the Cadence Virtuoso pectre circuit simulator for the 32-nm process using the Predictive Technology

Model.3 The operating temperature is 90 C, which is the average temperature in which the high-performance processors operate [12].We use this temperature value throughout the paper for all the experiments.We can observe that this approach achieves the desired gate voltage within 3.33 ns. For a processor which operates at 3-GHz frequency, it will take ten cycles to switch to the recovery boost mode.

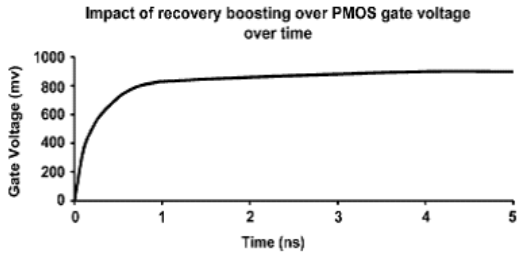


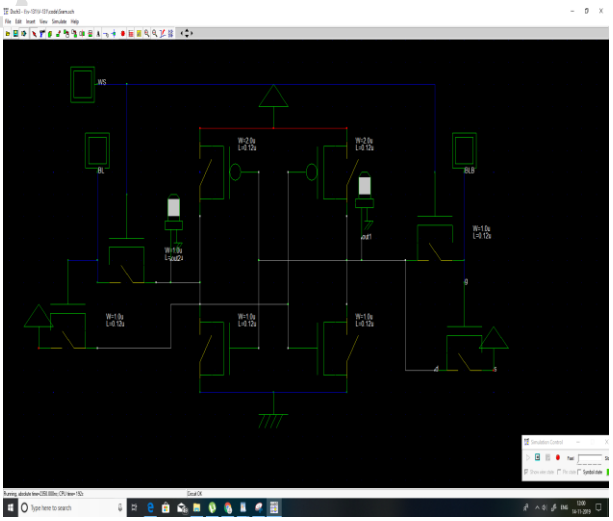

Fig. 2. PMOS gate voltages of an SRAM bitcell due to recovery boosting using the modified SRAM cell shown in Fig. 1(b) ($V_{dd} = 0.9$ V, $T = 90$ °C).

Similarly, it takes around ten cycles to go back to the normal operating mode from the recovery boost mode. However, our goal is to be able to switch between the recovery boost mode and the normal operating mode within a single cycle which is critical for a high-speed SRAM structure, such as the issue queue, where instructions need to be woken up and selected within a single clock cycle, in order to expedite the execution of dependent instructions. As mentioned before, recovery boost mode is applied when an entry of the structure holds data that is considered "invalid" at the architecture- level. Entries in the high-speed structures change their status between valid and invalid very frequently. For example, we find from architecture simulations that an issue queue entry
stays invalid for about 50 cycles before it changes its status to valid. In such scenario, the cell shown in Fig. 1(b) will take 20 cycles of the 50 cycles (40% of the invalid period) to shift between modes, given that shifting to the normal operating mode takes place during the end of the invalid period.

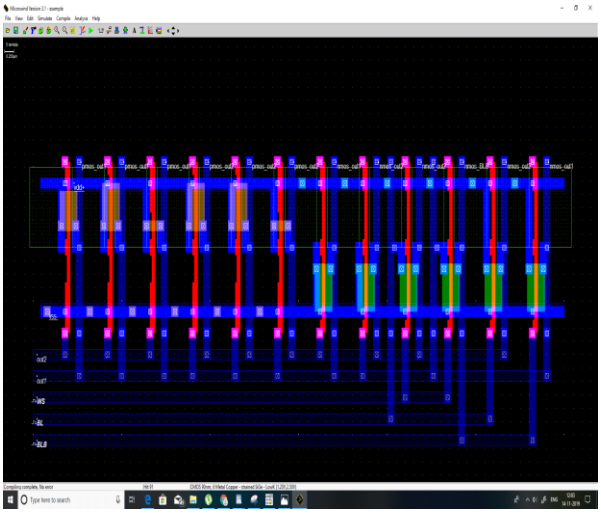
Thus, only 30 cycles could be utilized for the recovery process. On the other hand, if extra cycles are allocated to shift to the normal moperating mode after the invalid period, that would have negative consequences on the processor performance. Therefore, single-cycle switching is required for the high-speed structures in the processor for the maximum utilization of the invalid states for the recovery process without any performance loss. Such single-cycle switching can be achieved by raising the bitlines along with the ground voltage to . There are various ways of incorporating such cells into SRAM arrays, which we will discuss shortly. Recovery boosting can be provided at a fine granularity, such as for individual entries/rows of a memory array, or at a coarser granularity, such as for an entire array. We now discuss how the modified high-speed recovery boosting SRAM cells can be used in each of these scenarios and then discuss additional micro architectural issues related to implementing recovery boosting.

## V. RESULTS

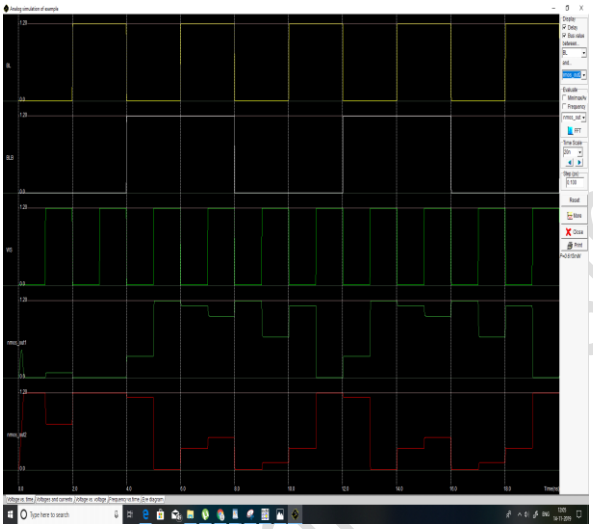
**Schematic diagram of proposed system**



**Layout of proposed system**



**Output of proposed system**



## VI. CONCLUSION

Power dissipation and stability are major issues in CMOS VLSI sub-micron technology. In this paper read and write static noise margins of proposed SRAM cell at different cell ratios and pull up ratios simultaneously are analyzed. The proposed SRAM cell has better read and write stability than 6T and 8T SRAM cells. The power dissipations at different temperatures, supply voltage values and bit line capacitances are analyzed. Power dissipation is much lesser for proposed SRAM cell than 6T and 11T SRAM cells for different temperatures, supply voltage values and bit line capacitances. This proposed SRAM cell has two voltage sources which are used for reducing the voltage swing during switching activity. The reduction in voltage swing results in reduction of dynamic power dissipation during the write/read operation. The extra voltage sources also provide the better static noise margin for the read and write operations in proposed SRAM cell. This proposed SRAM provides low power solution for battery operated devices like mobile phone, biomedical equipments etc.

**Future work**

This research contributes to better understanding of energy recovery SRAM. This work showed that the total energy and the energy during write cycle in particular will be saved in the proposed Adiabatic SRAM. Design is described using HSPICE code and functional simulation is carried out considering 65nm (BSIM level 54) models for transistors and JUNCAP1 diode model level 4 is used. The models describe the devices considering various sub 100nm process effects. Simulations are carried out and provisions of HSPICE commands to find energy, delay etc. are made use of.

- From the description, given in this thesis it may be noted that the effort is put in mostly to reduce the power dissipation and increase the efficiency of memory SRAM. In adiabatic SRAMs, the write delay has increased while the energy consumption has decreased. Although effort is put to optimize the performance parameters in Feat SRAM, there seems to be considerable scope for optimizing the 10T adiabatic SRAM circuit especially the bit driver circuit and the other components for reducing the write delay while sacrificing a little bit of power if it is necessary. Thus one may attempt at arriving at the designs with the tolerable delay and energy consumption. In this context one may resort to a figure of merit called power delay products and aim for lower power delay product.

- It may be noted that is work reported have concerns only with operational principles. However if this is to be realized in practice one has to draw the schematic using tools such as VIRTUOSO of CADENCE, verify the functionality, draw the layout based on specific technology libraries and carry out design rule (DRC) check, extract the circuit with parasitic components (RC extraction) and carrying out post layout simulations. The energy calculations can be done with the help of calculator tool. This post

layout simulation is especially important for sub-micron based technologies as the density of interconnects is high and their effect becomes prominent. Then the design can be prototyped by sending the design to the FAB.

- The design approach can be done at abstract level. Analytical models for energy consumption in deep submicron technology SRAMs and those for performance parameters should be developed so that optimization of one can be done with respect to the other.
- Further new topologies for SRAM cells and bit line architectures should be explored to minimize the energy consumption.
- This work concentrated on 65nm technology mode and the performance obtained is with respect to this technology. However if this concept is extended to further deep submicron technologies one can investigate the effect of the small feature size and threshold voltage

sizes on performance of SRAM which may get reflected through leakage power and short channel effects.

- The investigations reported in this thesis are for moderate memory size. However if bigger memories are to be realized, one has to look into memory organization problem from the point of writing, reading and hold mode.

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