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DESIGN AND IMPLEMENTATION OF SUM OF ABSOLUTE DIFFERENCE FOR VARIABLE BLOCK SIZE MOTION ESTIMATION IN VIDEO CODING

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Abstract- The paper implements the Sum Of Absolute Difference architecture for integer motion estimation as it employs numerous calculations and resources in the present day video coding. Unlike different hardware designs of SAD architecture , the paper introduces complement adders to enumerate the difference amongst the two pixel values of the current and the reference frames. An accumulation array unit is designed by using a 32-bit Brent Kung adder to produce the final output SADs for variable block sizes. The architecture is typically intended for block based video compression standards widely HEVC. The design exploits 4% of slice registers and 20% of slice LUTs in Xilinx Spartan 6 device. Also, the Performance analysis confirms that compared to alternative SAD architectures using carry select and carry skip adder, the proposed architecture reduces the area at no cost latency. In addition the video compression is performed in MATLAB software where the performance metrics essentially the compression ratio, peak signal to noise ratio and the mean square error are stated.

Keywords : Brent Kung Adder, HEVC , Sum Of Absolute Difference, Motion Estimation

I. INTRODUCTION

Video compression methods are utilized in majority of the commercial products, originally in the consumer electronic accessories which includes television sets, digital camcorders, cellular phones to internet broadcasting networks for applications like video chatting, video teleconferencing , multi-view videos, etc. In the view that these applications make video compression hardware device complex and inevitable for any commercial products. So as to upgrade video compression in real time design of video encoders. The International Standards for video coding are established these standards come up with add on video compression efficiency and several merits relevant to the previous video compression standards. The video compression methods are made convenient in distinct video encoders as they decline the storage space and transference bandwidth required for a video sequence.

HEVC is the presently effective Block-Based video coding standard realised by the joint collaborative video team of ITU-T and ISO-MPEG. It is also termed as H.265 video coding standard. This standard permits a pixel resolution of about 8192×4320 inclusive of 8K UHD resolutions. HEVC also imparts double compression efficiency, abates the bitrate by 50% with a consistent video quality as that of H.264. Exclusive of these details, HEVC is noted for its quadtree structure feature which comprises of a coding unit. The coding unit to a greater extent is parted into prediction units and transform units. The coding blocks in HEVC have substituted the conception of macroblocks used in H.264. Also, the highest coding block in HEVC is mainly 64×64 unit where transforms are applied.

Motion estimation procedure is the most immensely complicated segment in video encoders. The process deploys 90% of the complete encoding time. It also lists the motion vectors for each and every single block in the current frame to the best matched block in the reference frame.The Block Matching algorithm is the precise means of motion estimation considering that it lessens the temporal redundancy within two successive frames with great ease. It also acquires the displacement vectors

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between the current frame and one or more reference frames by utilizing the interframe coding technique.

In Block Matching algorithm each one frame of a given video sequence is partioned into a fixed number of block segments where for each and every specific block in the current frame the equivalent respective block in the reference frame is attained by choosing one of the varied distortion errors in particular the mean square error , mean absolute square error , and sum of absolute difference etc. Further to these varying distortion error benchmarks the Sum Of Absolute Difference called as SAD is regularly practiced as it assists to search out the best-matched block with great ease by computing the sum absolute difference amongst the pixel values of the current and reference frame. It is also implemented in the hardware in considerations to its simplicity, limited computations, and consistency. The usual formula to enumerate the SAD values between two coding blocks is detailed by a mathematical expression as stated below in equation (1).

$$SAD(m,n)=\sum_{i=0}^{m}\sum_{j=0}^{n}|X(i,j)-Y(i+m,j+n)$$

II. LITERATURE SURVEY

For the motion estimation measures, distinct VLSI architectures for SAD calculus are achievable in each of two ASIC and the FPGA implementation.

[2].The integer motion estimate theory of computing the SADs for variable coding blocks sizes extending from 4×4 to 32×32 is achieved by applying the processing element utilized in the design. Also the design exploits the concept of parallelism with fast search algorithm. The SAD valuates are computed using partial propogate SAD where every SAD is generated after four clock cycles. The number of clock cycles used in the implementation are huge which further degrades the functioning clock speed of the circuit.

[3]. It enumerates the SADs for the highest coding block size typically 64×64 coding unit using Wallace Tree Structure. The design utilizes larger area despite it evaluates the SADs of higher coding blocks by making use of lower coding block SAD which is a SAD $4 \times .4$.

III. PROPOSED SAD ARCHITECTURE

A. Sum Of Absolute Difference

In this section, we present the Sum Of Absolute Difference architecture for integer motion estimation unit. The design figures the SADs of the larger coding segment by combining the SADs of lower coding segments. It evaluates the SADs for the prediction units of HEVC for coding segments extending from 4×4 to 64×64. The Sum Of Absolute Difference algorithm is vitally inclusive of three steps basically the absolute difference computing, difference accumulation unit and the minimum SAD determination unit as shown in the Fig.1

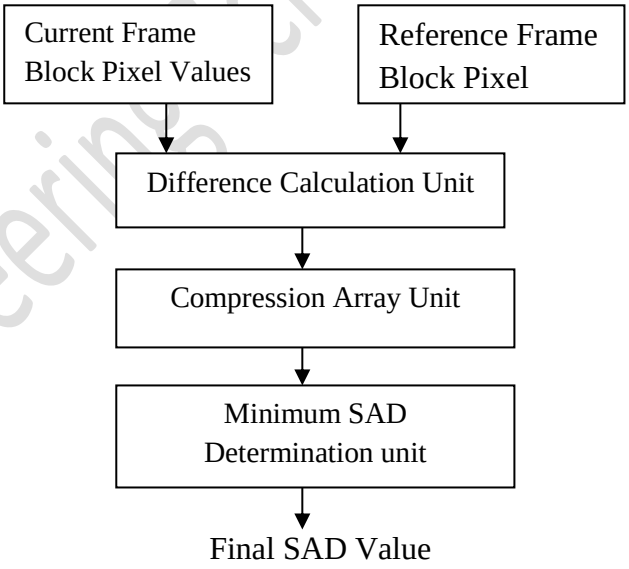

Fig.1: Sum of Absolute Difference Algorithm

- **Absolute Difference Circuit**

The difference computing circuit evaluates the absolute difference between the two-pixel values of the current frame and the reference frame by employing 2's complement method. The 2's complement means is preferred as it is the simplest and most obvious way of estimating the difference pixel values as shown in the equation (2).

$$|X-Y| = \{X + Y' + 1 \ if \ MSB = 1\}$$
$$\{X' + Y + 1 \ if \ MSB = 0\} \quad (2)$$

Where MSB is the Most Significant Bit , $X'$and Y'represent the complements of X and Y .In this method of complement addition the MSB is 1 if X is greater than Y. The Fig 3.2 shows the absolute

difference circuit for enumerating the difference of the pixel values for the given frames of a video series .

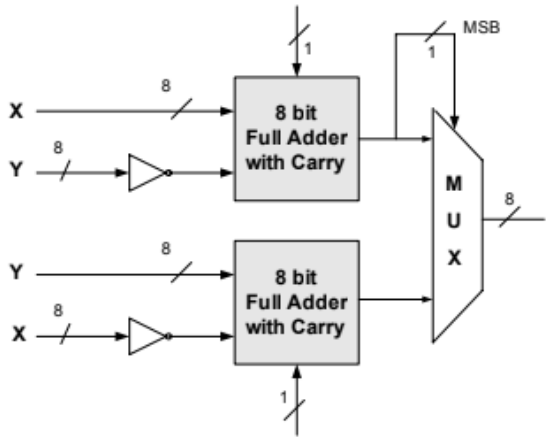

Fig.2: Absolute Difference Circuit

- **Difference Accumulation unit**

The difference accumulation unit includes an adder circuit to complete the addition of absolute difference pixel values obtained from absolute difference circuit to attain the final SAD estimates for a specified coding block size. The adder circuit utilized in the design is a 32- Bit Brent Kung Adder.This adder sums the two inputs and produces two outputs the ultimate sum and the carry out bit. The Brent Kung Adder has been exploited in the SAD architecture because it depletes the chip area simultaneously optimizes the performance of the design. The Brent Kung Adder has three phases basically the pre-processing phase, carry generate phase and lastly the post-processing phase also known as ultimate sum phase. The final post processing phase results the end sum and carry out bit as shown in the below mentioned equations.
Initially in the pre processing phase the generate and propagate signals are generated as shown in equations (3)

$$P_i = A_i \ xor \ B_i$$

$$G_i = A_i \ and \ B_i \qquad (3)$$

Next, in the following carry generate phase the carry generate and carry propagate signals are obtained by using the equations (4). They are represented as Black cells.

$$C_P = P_i \ and \ P_{i-1}$$

$$C_g = G_i \ or \ P_i \ and \ G_{i-1} \quad (4)$$

Whereas the carry generate represents grey cell. These cells are used to generate the final sum bit as shown in equation (5).

$$C_g = G_i \ or \ P_i \ and \ G_{i-1} \quad (5)$$

Lastly , the post processing phase generates the ultimate sum and the carry out bits as shown in the equations (6)

$$S_i = P_i \ xor \ C_{i-1}$$
$$C_i = G_i \ or \ P_i \ and \ C_{i-1} \quad (6)$$

The adder utilized in the design of SAD architecture proposed in the paper is shown in the Fig.3. The 32-Bit Brent Kung Adder is designed using two 16 -Bit Brent Kung Adders.

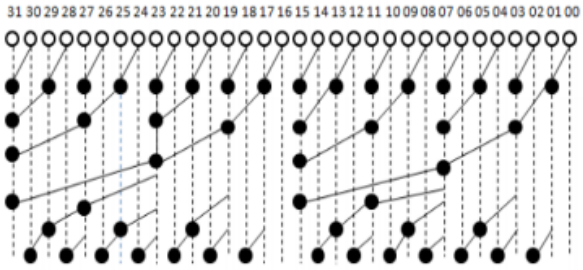

Fig.3: 32-Bit Brent Kung Adder

- **Minimum SAD Determination Unit**

The minimum SAD determination unit finds the lowest SAD value from the calculated SAD values for the stated coding block size.

B. Architecture and Working

The complete SAD unit calculates the SAD values based on the control unit output.The control unit determines which coding block should be used for computing the SAD values depending on the partition of frames for a given video sequence.The design includes a single 4x4 absolute difference calculation unit, and variable block sizes SAD evaluations extending from 4×4 to 64×64 coding block sizes of a prediction unit in HEVC.

Firstly, a set of 4x4 current block pixels and reference block pixels are transmitted to the 4x4 SAD unit through a system data bus. In every single clock cycle one 4x4 SAD, two 4x2 SADs and two 2x4 SADs are produced from 4x4 SAD unit. These SAD values are applied to produce the upper mode SADs. The 4x4 SAD values are saved in the registers and are also given to the 8x8 SAD unit .

After four clock cycles the 8x8 SAD unit produces one 8x8 SAD, two 8x4 SADs, two 4x8 SADs.These SAD values are further saved in the registers and are given to upper mode 16x16 SAD unit. The process continues up to 64x64 SAD unit. As there are no parallel stages, the total clock cycles to evaluate one 64x64 coding block can be computed using the equation (7).

$$\text{Delay} = 4^{d-p} + K \qquad (7)$$

Where d represents the maximum depth of SAD unit , p represents the number of parallel stages and finally k represents the controller delay.

While ignoring the controller delay, to processing one 64x64 SAD coding block a sum total of 256 clock cycles are required. As every one pixel comprises 8 bits a data bus of 256 bits is needed for computing one 4x4 SAD unit .

The architecture shown in Fig 3.4 calculates the SAD value for one 64x64 coding block .

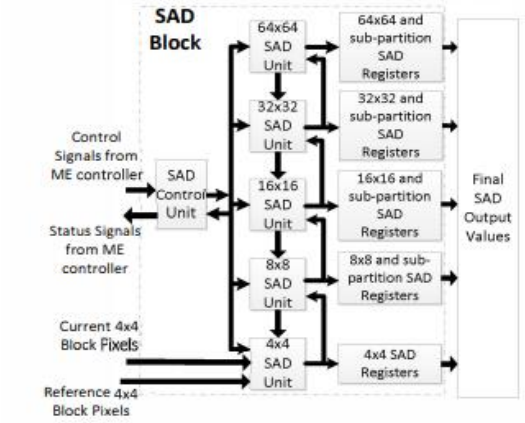

Fig.4: SAD Architecture For Motion Estimation

IV. SYNTHESIS RESULTS

The proposed architecture is implemented in Verilog HDL. In addition, the simulation and functional verification of the architecture is accomplished using Xilinx ISE 14.7 simulator. The architecture utilises 4% of slice registers , 20% of slice LUTs and a total of 256 clock cycles to calculate one 64× 64 SAD . Further, it operates at a clock frequency of 142.108 MHz by using the 2's complement difference circuit and a 32- bit Brent Kung Adder designed.Our synthesis results are shown in the Table.1.

It is stated that the Brent Kung Adder utilized in the compression array unit in our design outperforms in comparison to the carry select adder and the carry skip adder with unsigned difference circuit. Besides video compression is performed in MATLAB software using the Block- Based Sum Of Absolute Difference method where the performance metric parameters like compression ratio, peak signal to noise ratio and mean square error are noted down for variant video sequences as shown in the Table. 2.

A. Simulation Results OF Absolute Difference Circuit

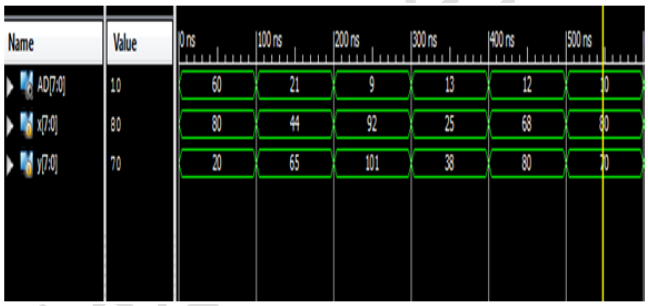

Fig.5: Simulation Results of Absolute Difference Circuit

B. Simulation Results OF 32- Bit Brent Kung Adder Designed

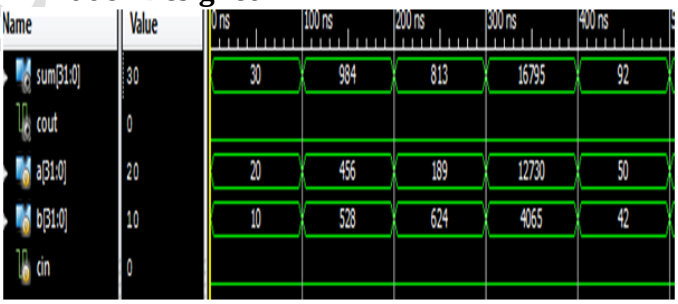

Fig.6: 32-Bit Brent Kung Adder Designed

C. Simulation Results OF SAD 4×4 Unit Using 32-bit Brent Kung Adder Proposed in the Design

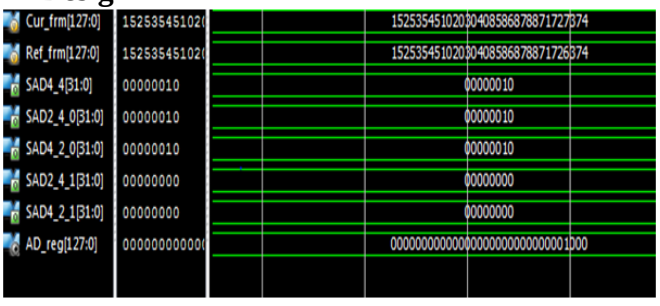

Fig.7: SAD 4×4 Unit

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D.Simulation Results Of SAD 64 × 64 Unit

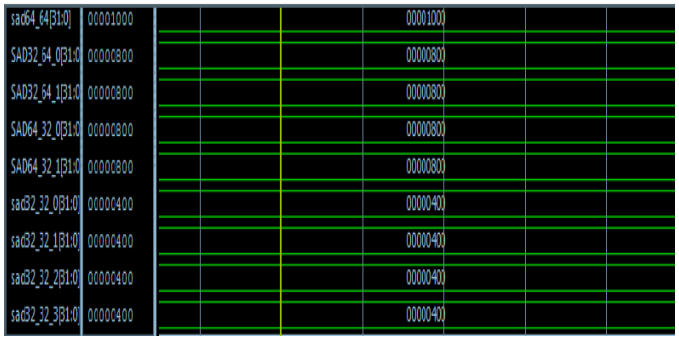

Fig.8 : SAD 64 × 64 Unit

Table.1 Comparison Results of SAD Architecture using 32-Bit Brent Kung Adder with 2's complement absolute difference circuit along with 32-Bit Carry Select and Carry Skip Adder using unsigned numbers absolute difference circuit which contains 1's and 2's comparator.

	SAD using CarrySelect Adder	SAD using CarrySkip Adder	SAD using BrentKung Adder (Proposed Design)
Number of Slice Registers (out of 18224)	3824	3824	842
Number of Slice LUTs(out of 9112)	6437	6440	1892
Number of Clock Cycles	256	256	256
On Chip Bus Width	256	256	256
Minimum Period	13.738 ns	13.636 ns	7.037 ns
Maximum Frequency	72.793 MHz	73.334 MHz	142.108 MHz

Table.2 Parameter Evaluations For Variant Video Sequences

	Parameters		
Video File Type	Compression Ratio	Mean Square Error	Peak Signal to Noise Ration
Nature.mp4	76.265	1.75	96.13
Traffic.mp4	53.28	30.75	68.14
Dance.mp4	58.67	34.71	65.88
Tennis.mp4	53.95	6.10	90.58
New York city.mp4	47.31	0.38	106.17

V. CONCLUSION

An effective SAD Design for integer motion estimation in video coding has been proposed. The circuit has been simulated and synthesized on Xilinx Spartan-6 device. The design uses the 4 x4 SAD coding blocks to calculate the SAD value for one 64 x 64 block. The VLSI architecture operates at a clock frequency of 142.108 MHz. The architecture increases the encoding speed and occupies less area as compared to other architectures using carry skip and carry select adder. The circuit can be adopted for various fast and full search algorithms utilizing Block Motion Estimation techniques.

VI. ACKNOWLEDGMENT

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