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IMPLEMENTATION OF APPROXIMATE DADDA MULTIPLIER WITH INEXACT COMPRESSORS

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ABSTRACT: Approximate computing of DADDA multiplier has significantly reducing the power consumption, delay and area. Multiplication plays an important role in a digital signal processing application which require lot of space, power and area so, that's why we go for an approximate multiplier for reducing complexicity. But, it dosen't give an exact results. In this paper we are analyzing and designing approximate 4:2 compressors and also we are 8*8 Dadda multiplier. Here it also provides simulation and synthesis results by using xlinxs 14.7 ISE software .In exact multiplication we are using 18 compressors where in case of approximate multiplication we are using 17 compressors.

Index Terms: Compressors, Dadda algorithm, 8*8 multiplier, approximate computing.

INTRODUCTION:

In the software program of digital signal processing actual results are not wanted always. Adders and multipliers play a high role in this software. Multiplication is a vital approach this is utilized in diverse digital sign packages. One-of-a-type styles of multipliers are Dadda, Wallace-Tree, Vedic and booth. Those are used for Multiplication in comparison to Wallace-tree, Vedic and sales space Dadda offers Better results in power consumption, excessive bandwidth .In proposed work a multiplier in its partial end result addition approach half of adder and 4: 2 compressors are used as a computational blocks.

This paper consists of chapter 1) literature survey 2) actual compressors format, 3) approximate compressors, 4) multiplication, 5) simulation results.

LITERATURE SURVEY:

Various sorts of multipliers are mentioned inside the literature to acquire energy and overall performance optimization. Multiplication is a essential hardware block in a digital signal processing to carry out a multiplication in a clean manner through the use of a one two input adder .In a multiplication technique for unsigned numbers two numbers are worried in a A multiplication are referred to as multiplicand and the multiplier. For n bit multiplicand and multiplier, the ensuing product may be 2n bits. Many packages including multimedia and picture processing can tolerate errors and impression in competition and still produce meaningful and beneficial outcomes accurate and unique model and algorithms are not constantly suitable green to be used on this utility. Column compression structure for immediate multiplication proposed by using Wallace gives a complete put off prapotional to word length of the multiplier. Column compression multipliers are quicker than array multipliers, due to the fact the put off in array multipliers very linearly with the operand word length. Error distance[ED] is defined as errneous and the correct one the suggest ED and normalized ED are proposed by way of thinking about the normalized averaging impact of multiple inputs and the normalization of a couple of bit adders the tradeoff between precision and energy has also been quantitatively evaluated . Dadda method for partial product discount uses only vital reduction decided by way of the Wallace table proven in beneath table .It uses a technique to boom the range of ha and to lower the overall partial merchandise reduction .Number discount levels according to range bits inside the column of partial product matrices.

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EXACT COMPRESSORS

Various forms of multipliers are existed for widespread overall performance optimization. In multi operand carry save addition or parallel multiplication is to minimizing n numbers to 2 numbers. (n-2) compressors are generally a slice of circuit that reduces n range to two numbers. The starting bit from the right position is denoted as Cin, the higher carry bit position is denoted as Cout.

The major aim of p1recise compressor is to provide a correct output however with power intake and delay. Basically four: Two compressors got here into life to replace the use of extra range of FA. There are varieties of implementation for the right compressor as follows:

• Using FA.

• Using XOR-XNOR module with multiplexer

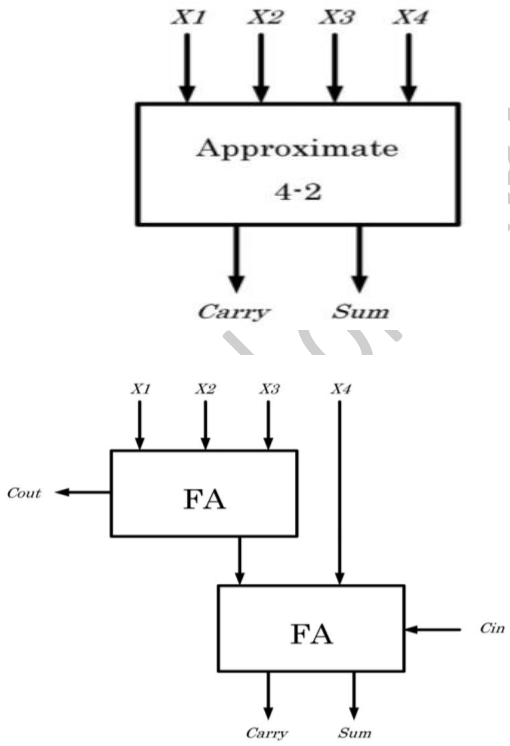


Fig1:Compressor using two full adder

$$Sum = x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin \quad (2)$$

$$Cout = (x1 \oplus x2)x3 + \overline{(x1 \oplus x2)}x1 \quad (3)$$

$$Carry = (x1 \oplus x2 \oplus x3 \oplus x4)Cin + \overline{(x1 \oplus x2 \oplus x3 \oplus x4)}x4. \quad (4)$$

Truth Table of 4-2 Compressor

c_{in}	X_4	X_3	X_2	X_1	c_{out}	carry	sum
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	1	0	0
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	1	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	1	0	1
1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

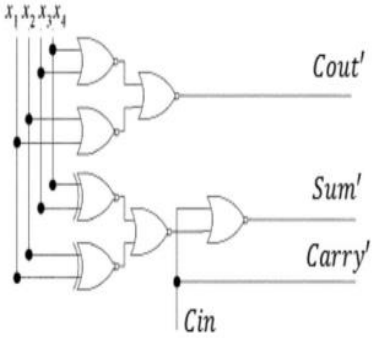
PROPOSED APPROXIMATE 4:2 COMPRESSOR

This consists of approximate compressors. It produces as a minimum 17 wrong outcomes out of 32 variable output, Error charge is calculated through the ratio of inaccurate outputs to the overall variety of output. Here two designs are proposed to reduce the complexity of the multiplier.

DESIGN 1

In exact compressors out of 32 states 24 states Cout is same as Cin. By changing the value of 8 outputs carry is made equal to Cin.

Fig: 2.logic diagram of design 1 compressor



c_{in}	X_4	X_3	X_2	X_1	c_{out}'	$carry'$	sum'
0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	0	0	1
0	0	1	0	0	0	0	1
0	0	1	0	1	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	1	1	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	0	0	1
0	1	1	0	1	1	0	1
0	1	1	1	0	1	0	1
0	1	1	1	1	1	0	1
1	0	0	0	0	0	1	0
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	1	0
1	0	1	0	0	0	1	0
1	0	1	0	1	1	1	0
1	0	1	1	0	1	1	0
1	0	1	1	1	1	1	0
1	1	0	0	0	0	1	0
1	1	0	0	1	1	1	0
1	1	0	1	0	1	1	0
1	1	0	1	1	1	1	0
1	1	1	0	0	0	1	0
1	1	1	0	1	1	1	0
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	0

$$Carry = Cin$$
$$Sum = \overline{Cin}(\overline{x1 \oplus x2} + \overline{x3 \oplus x4})$$
$$Cout = \overline{\overline{x1x2} + \overline{x3x4}}$$

Since the output carry gains the higher weight of a binary bit producing an error value at the output. The simplification of sum reduces complexity of the approximate compressor output . The presence of error in the sum will reduce the delay of approximate compressors and the overall delay of the design. In the last step the value of Cout may reduce the error distance of the approximate carry and sum also provide simplified design.

DESIGN 2

The second design of an approximate compressor is proposed to increase performance as well as reducing the error rate .since the carry and cout have the weight the proposed equations for the approximate carry and cout. The block diagram of this approximate 4*2 compressor is as show in below figure.

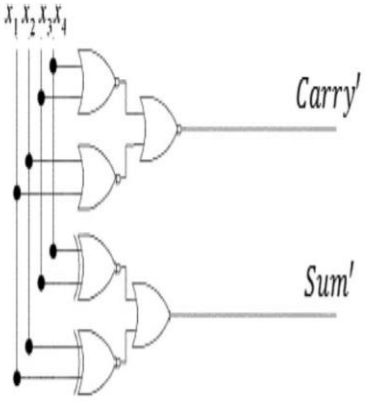


Fig: 3.Logic diagram of design 2 compressor

$$Sum' = (\overline{x1 \oplus x2} + \overline{x3 \oplus x4})$$

$$Carry' = \overline{(\overline{x1x2} + \overline{x3x4})}.$$

X_4	X_3	X_2	X_1	$carry'$	sum'
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	0	1
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	0
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	1	1	1
1	1	1	0	1	1
1	1	1	1	1	1

MULITIPLCATION

The impact of the usage of proposed compressor for multiplication is

investigated. A quick (precise) is commonly composed of three parts

• Partial product technology

• A carry store adder (CSA) tree to reduce the partial products matrices pleasant an addition of simplest two products.

• A carry propagation adder (CPA) for the very last computation of the binary outcomes.

For proposing approximate multipler four instances are required.

• In design 1 three 3:2 compressors,3HA and 18 4*2 compressors.

• In design 2 number of compressors requirement is minimized due to absence of Cin and Cout.in this multiplier we require 6 HA ,one 3:2

Compressors and 17 4:2 compressors .on circuitry a lower range of compressors .design 2 uses 6 ha , 1 FA and 17 compressors.

• design1 is used the (n-1) least significant columns. The other n maximum large columns actual 4*2 compressors, these are removing the error rate.

• In the design 2 four*2 compressor are used in the (n-1) least great columns ,which gives the approximate solution.

The below figure show the Dadda algorithm for design 1

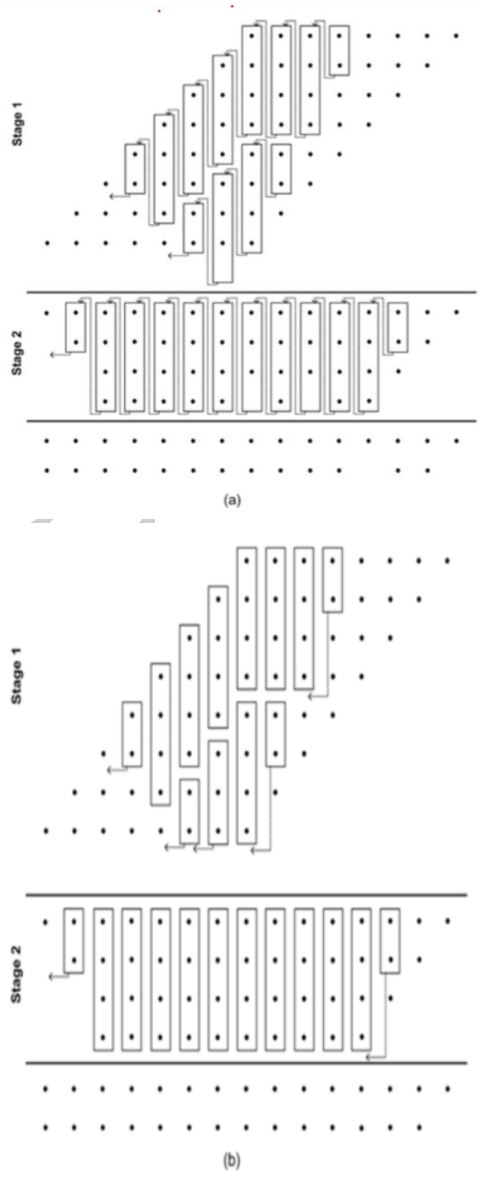


Fig: 4.Dadda algorithm for design 2

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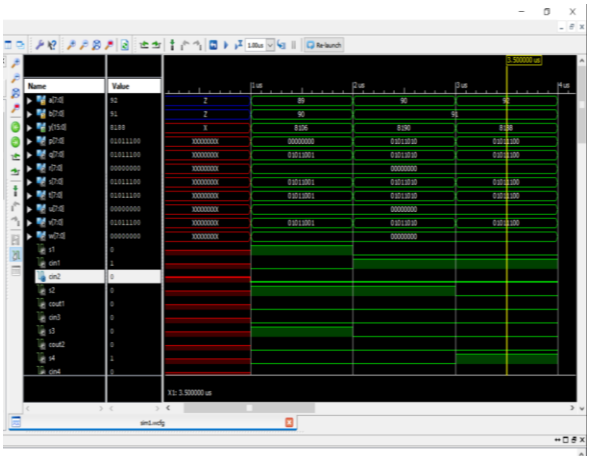
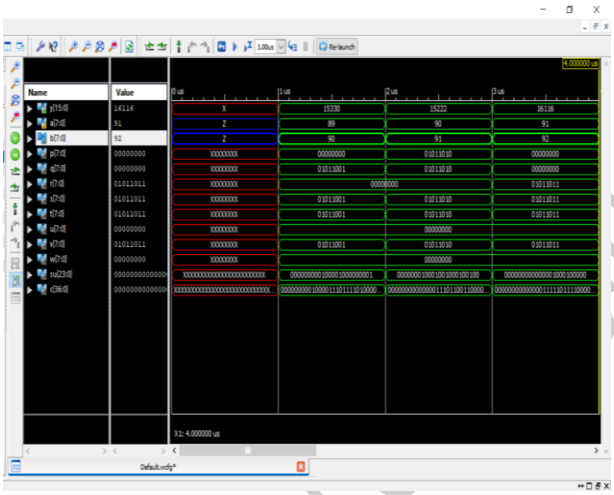
SIMULATION RESULTS:

For design1



For design2



CONCLUSION

Efficient multiple is designed using dada algorithm which has less number of transistors .the first and second multiplier have significant reduction on delay, area and power. This proposed multiplier can be applicable to image processing applications. For multiplying two images on pixel by pixel basis, therefore blending of two images into a single image with high PSNR.

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