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Design of a High Performance 16-bit Approximate Arithmetic Units

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ABSTRACT:

The research community in the last few years from the field of approximate computing has received significant attention, particularly in the context of different signal processing. Image and video compression algorithms such as JPEG, MPEG and so on, which can be exploited to realize highly power efficient implementations of these algorithms. However, existing approximate architectures typically fix the level of hardware approximations statically and are not adaptive to input data. This design reconfigurable adder/subtractor blocks, and subsequently integrate these blocks in the motion estimation and discrete cosine transform modules of the MPEG encoder. I propose two heuristics for automatically tuning the approximation degree of the RABs in these two modules during runtime based on the characteristics of each individual video. Dynamically adjusting the degree of hardware approximation based on the input video respects the given quality bound PSNR degradation across different videos while power saving a dual mode full adder is greater than the full adder, when compared to existing implementations.

Index terms: approximate circuits, low power design, approximate computing

1.INTRODUCTION:

Digital signal processing (DSP) blocks from the Backbone of various multimedia applications used in portable devices. Most of the DSP blocks implement image and video compression algorithms. Approximate computing architectures exploit the fact that a small relaxation in output correctness can result in significantly simpler and lower implementations. However, most approximate hardware architectures proposed so far suffer from the limitation that, for widely varying input parameters, it becomes very hard to provide a quality bound on the output, and in some cases, the output quality may be severely degraded. The main reason for this output quality fluctuation is that the degree of approximation (DA) in the hardware architecture is fixed statically and cannot be customized for different inputs. This paper adopts a different approach to addressing this problem by dynamically reconfiguring the approximate hardware architecture depending on the inputs. Following contributions are

1) I demonstrate that, for a fixed level of hardware approximation in an MPEG encoder, the output quality varies widely across different videos, often going below acceptable limits. This shows that setting the level of hardware approximation statically is insufficient.

2) I investigate, for this paper, the use of dynamically reconfigurable approximate hardware architectures that vary the degree of approximation during run-time across multiple computational cycles, depending on the inputs.

3) Toward this end , I propose the design of reconfigurable adder/subtractor blocks for four commonly used adder architectures, ripple carry adder , carry look ahead adder, carry bypass adder, and carry select adder, and subsequently integrate them into the MPEG encoder to enable quality configuration execution.

4) I propose a design methodology to adapt a degree of approximation dynamically based on the characteristics with the main aim of maintaining the output quality.

5) I have implemented the proposed architecture for an MPEG encoder on an Dual mode full adder (DMFA). My experimental results show that the proposed architecture results in power savings compare to a baseline approach that uses reconfigurable approximate architecture with the goal of maintaining a particular peak signal-to-noise ratio (PSNR) threshold for any video.

2.RELATED WORKS:

There has been a lot of effort in constructing energy-efficient video compression schemes. Different methods of power reduction include algorithmic modification [1], [2], voltage over scaling [3] and imprecise computation of metrics [4]. Approximate computing methods achieve a large

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amount of power savings by introducing a small amount of error or inaccuracy into the logic block. Different approaches for approximation include error introduction through voltage over scaling. [5],[6]. Intelligent logic manipulation [7] and circuit simplification using don't care based optimization techniques [8].

The methods in [9] and [10] introduce imprecision by replacing adders with their approximate counterparts. There also exist instances of approximations introduced in the MPEG encoder [5], [11] [13]. Most of them exploit the inherent error resilience of the motion estimation algorithm which results in minor quality degradation. For example [11] use a bit width compression technique to reduce power consumption video frame memory [12] and [13] use bit truncation to introduce approximations in the ME block of the MPEG encoder. Note that, a preliminary version of this paper appeared in [14]. Finally, we provide a comparative study of the power consumption of the different RAB s and also demonstrate how the DA is automatically regulated across different frames during runtime.

3.BACKGROUND:

MPEG is mostly preferred for the video compression scheme in modern video devices and applications. MPEG- 2/MPEG-4 standards are used to squeezed to very small sizes. MPEG uses both Interframe and Intraframe encoding for video compression. Intraframe encoding involves encoding the entire frame of data, while Interframe encoding utilizes predictive and interpolative coding techniques as means of achieving compression.

The inter-frame version exploits the high temporal redundancy between adjacent frames and only encodes the differences in information between the frames, thus resulting in great ratios. In this case, the encoding takes placed based upon the differences between the current frame and previous frame in the video sequence.

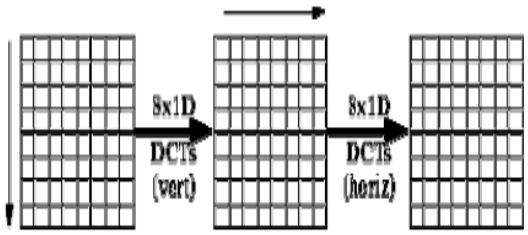

Fig 1: DCT Block Diagram

There are three kinds of frames used in MPEG encoding:

1. I-frames means intraframe encoded.

2. P-frames means predictive encoded.

3. B-frames means bidirectional encoded.

Every non encoded frame is divided into Macro blocks (MBs), such as 16 × 16 pixels. The Motion vectors (MVs) actually contain the information regarding the relative displacements of the Macro blocks (MBs) in the present frame in comparison with the reference.

4.PROPOSED ARCHITECTURE:

Reconfigurable Adder/Subtractor Blocks:

In degree of approximation is dynamically varied which can be done when each of the adder/subtracter blocks with one or more of its approximate copies. Reconfigurable Adder/Subtractor blocks is able to switch between them as per requirement and can include any approximation version of this blocks.

1-bit dual mode full adder is consists A, B, Cin are the inputs and outputs are Sum = A and Cout = A. When each full adder (FA) cell of the adder/subtractor with a dual-mode full adder (DMFA) from the proposed scheme. In which each full adder cell can perform operating either in fully accurate or in some approximation mode depending upon the state of the control signal APP. When operating in the approximate mode the full adder act as power gated.

Dual-mode full adder can operated in either the two approximation modes. Approximation was selected for its higher probability of giving the

accurate output result than the truncation. In which does not variably outputs 0 irrespective of the input.

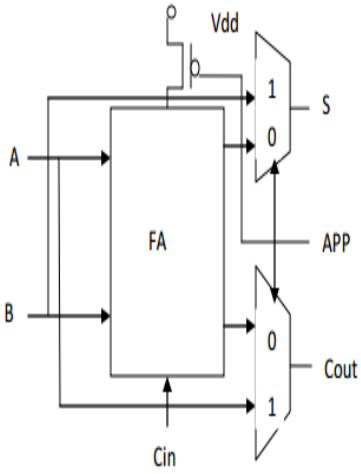

Fig 2: 1-bit DMFA

In addition, it is also consists of the approximation controller for generating the appropriate select signals for the multiplexers. From the point of controlling the approximation magnitude by using a Multimode full adder cell. Because multimode full adder cell would provide even a better alternative to the dual-mode full adder. It also improve the complexity in the decoder block, it is used for select the right signals to the multiplexers as well as logic overhead for the multiplexers themselves.

DMFA overhead

Dual-mode full adder is consists the power gating transistor and the multiplexers are design to incur the possible over head. Dual-Mode full adder experiments show that the switching power of the CMOS transistors contributes toward the most of the total power consumption of the full adder and dual-mode full adder blocks.

The additional overhead is used to switching of the power gating transistor can be rejected, hence it is switching algorithms. This is mainly due to the spatial and temporal locality of the pixel values across the consecutive frames.

The concept of the adder/subtractor blocks is extend to other adder architectures as well. Adder architecture is consists CBA and CSA, which also contain full adder as the fundamental building blocks, can be made accuracy configurable by direct substitution of the full adders with DMFAs.

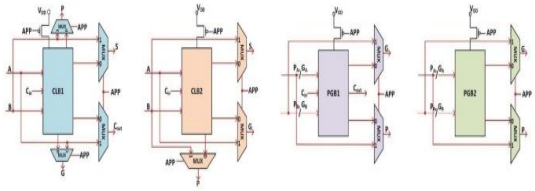

Fig 3: 1-bit dual mode carry propagate generate blocks

The difference among the CLB1 produces an additional Cout signal compared with CLB2. Their corresponding to the dual-mode versions, DMCLB1 and DMCLB2, have both sum S and propagate P approximated by input operand B and both Cout and generate G approximated by input operand A, as shown in figure 4. The basic blocks present in the higher levels of carry look ahead adder CLA hierarchy are represented as the configurable as propagate P and generate G blocks, PGB1 and PGB2.

In this case PGB1 generate an extra Cout output as compared with PGB2. As shown in figure 4, the configurable dual-mode versions, DMPGB 1 and DMPGB 2, use inputs Pa and Pb as approximations for outputs propagate and generate. These approximations ensuring that the ratio of the probability of match output to the additional circuit overhead for each of the blocks is large. Table 2 shows and realize the additional circuit overhead for each of the Dual-mode full adder blocks. When operating in either accurate or else approximate mode. Reconfigurable of Carry lookahead adder (CLA), Dual-mode carry lookahead blocks such as DMCLB1 and DMCLB2 blocks are approximated in according with the Dual-mode (DA).

However the Dual-mode propagate generator blocks such as DMPGB1 and DMPGB2 blocks approximated when each and every Dual-mode carry propagate generator blocks such as DMCLB1, DMCLB2, DMPGB1 and DMPGB2 block, which belongs to the transitive fan-in cones of the concerned block is approximated.

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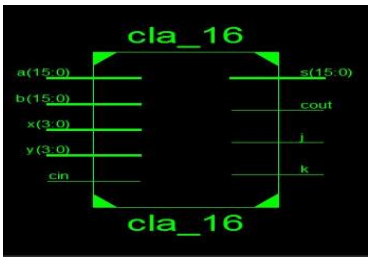

Fig 4: RTL schematic diagram of 16-bit cla

Fig 5. TTL diagram of 16-bit cla

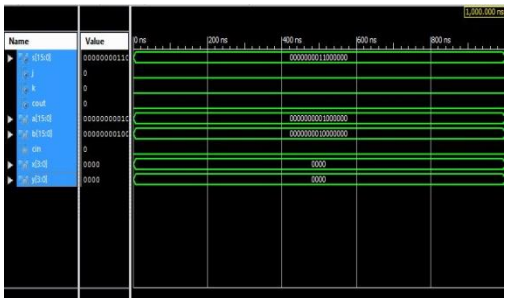

Fig 6: Simulation result for 16-bit cla

Otherwise, the block is performed in the accurate mode. For example, any Dual-mode propagate generator blocks (DMPGB) block at the second level of the carry lookahead adder (CLA) can be performed in approximate mode, and both of its constituent DMCLB1 and DMCLB2 blocks are performed in the approximate mode. In each DMPGB block can be approximated only when both of its constituent DMPGB1 and DMPGB2 blocks are approximated. This architecture can be realize extrapolated to other similar type Carry lookahead adders (CLAs), and so on

To the architecture of the carry save adders, where approximating each bit in the MSB results in power gating of two full adders compared with one full adder when the LSBs are approximated.

This is the point, where the savings due to the addition al multiplexers, power gating transistors, and controller. The inherent error resilience represented by the motion estimation ME and the small inputs to the DCT block gives sufficient opportunities for achieving a high degree of approximation (much greater than 5) and thereby high power savings.

5.CONCLUSION:

This paper proposed a reconfigurable approximate architecture for the MPEG encoders that optimize power consumption while maintain a output quality across different input videos. The proposed architecture is based on the input characteristics. It requires the user to specify only the overall minimum quality for videos instead of having to decide the level of hardware approximation. Our experimental results show that the proposed architecture results in power savings equivalent to a baseline approach that uses fixed approximate hardware while respecting quality constraints across different videos. Future work includes the incorporation of other approximation techniques and extending the approximations to other arithmetic and functional blocks.

REFERENCES:

[1] M. Elgamel, A. M. Shams, and M. A. Bayoumi, “A comparative analysis for low power motion estimation VLSI architectures,” in Proc. IEEE Workshop Signal Process. Syst. (SiPS), Oct. 2000, pp. 149–158.

[2] F. Dufaux and F. Moscheni, “Motion estimation techniques for digital TV: A review and a new contribution,” Proc. IEEE, vol. 83, no. 6, pp. 858–876, Jun. 1995.

[3] I. S. Chong and A. Ortega, “Dynamic voltage scaling algorithms for power constrained motion estimation,” in Proc. IEEE Int. Conf. Acoust., Speech, Signal Process. (ICASSP), vol. 2. Apr. 2007.

[4] I. S. Chong and A. Ortega, “Power efficient motion estimation using multiple imprecise metric computations,” in Proc. IEEE Int. Conf. Multimedia Expo, Jul. 2007.

[5] D. Mohapatra, G. Karakonstantis, and K. Roy, “Significance driven computation: A voltage-scalable, variationaware, quality-tuning motion estimator,” in Proc. 14th ACM/IEEE Int. Symp. Low Power Electron. Design (ISLPED), 2009.

[6] J. George, B. Marr, B. E. S. Akgul, and K. V. Palem, “Probabilistic arithmetic and energy efficient

embedded signal processing," in Proc. Int. Conf. Compil., Archit., Synth. Embedded Syst. (CASES), 2006.

[7] D. Shin and S. K. Gupta, "A re-design technique for datapath modules in error tolerant applications," in Proc. 17th Asian Test Symp. (ATS), 2008.

[8] S. Venkataramani, A. Sabne, V. Kozhikkottu, K. Roy, and A. Raghunathan, "SALSA: Systematic logic synthesis of approximate circuits," in Proc. 49th Annu. Design Autom. Conf. (DAC), Jun. 2012.

[9]V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan, and K. Roy, "IMPACT: IMPrecise adders for low-power approximate computing," in Proc. 17th IEEE/ACM Int. Symp. Low-Power Electron. Design (ISLPED), Aug. 2011.

[10] V. Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Lowpower digital signal processing using approximate adders," IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 32, no. 1, Jan. 2013.

[11] V. G. Moshnyaga, K. Inoue, and M. Fukagawa, "Reducing energy consumption of video memory by bit-width compression," in Proc. Int. Symp. Low Power Electron. Design (ISLPED), 2002.

[12] Z. He and M. L. Liou, "Reducing hardware complexity of motion estimation algorithms using truncated pixels," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), vol. 4. Jun. 1997.

[13] Z.-L. He, C.-Y. Tsui, K.-K. Chan, and M. L. Liou, "Low-power VLSI design for motion estimation using adaptive pixel truncation," IEEE Trans. Circuits Syst. Video Technol., vol. 10, no. 5, Aug. 2000.

[14] A. Raha, H. Jayakumar, and V. Raghunathan, "A power efficient video encoder using reconfigurable approximate arithmetic units," in Proc. 27th Int. Conf. VLSI Design, 13th Int. Conf. Embedded Syst., Jan. 2014.

[15] P. M. Kuhn, Algorithms, Complexity Analysis and VLSI Architectures for MPEG-4 Motion Estimation, 1st ed. Norwell, MA, USA: Kluwer, 1999.