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Switched Capacitor for Comparison of 17 Level Symmetric and Asymmetric Multilevel Inverters with Dynamic Loads

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ABSTRACT: This paper implements and compares a symmetric hybridized cascaded multilevel inverter and an asymmetric multilevel inverter utilizing a switched capacitor unit for 17 level inverters. The symmetric hybridized multilevel inverter topology consists of a modified H-bridge inverter, which results in an increase in the output voltage to five level from the three level by using a bi-directional switch at the midpoint of a dual-input dc source. In the proposed asymmetric multilevel inverter, dc sources are replaced with the switched capacitor unit, which in turn boosts the output voltage and produces twice the voltage levels at the loads. The proposed topology with the staircase modulation technique has been verified using MATLAB–SIMULINK. The results substantiate that these multilevel inverter topologies are better stabilized during load disturbance conditions with low total harmonic distortion, a lesser number of switches, and increased output voltage levels, and these topologies well suit for renewable energy applications.

INDEX TERMS: Multilevel inverter (MLI), staircase pulse width modulation technique (SPWM), switched capacitor unit (SCU), total harmonic distortion (THD), high output voltage levels.

I. INTRODUCTION

The multilevel inverters have been developed and utilized for higher voltage levels . In achieving higher voltage levels and power levels, cascaded multilevel inverters (MLI) are proven to be more flexible than conventional topologies. Its modularity property can be used to increase the power output of the inverter. Cascaded MLIs are constructed by linking in series output terminals of several H-bridge inverters . It is hence evident that this configuration supports high power levels with the use of low voltage rating components in inverters. In case of a fault in any one of the inverter cells, it can be easily and quickly replaced because of its modularity property. In order to maintain reliability in inverter output in the event of a fault in any inverter cell , a suitable control strategy can be used to bypass the faulty cell without disturbing the load . With advancements in multilevel inverters, the need for the design of new modulation methods for the same is increasing. As a result, many modulation schemes have been introduced. Based on converter topology and its domain of application, each modulation technique has its own advantages and disadvantages. The classification of modulation strategies for multilevel inverters has been proposed in based on the difference in high or low-frequency switching. High power applications utilize a frequency up to 1 kHz. The PWM switching is also suitable for Hybrid cascaded MLI . This facilitates charging and discharging time for storage elements used in multilevel inverters. PWM methods based on the carrier are classified into level shifted and phase shifted modulation schemes. Level shift modulation techniques are mostly employed in various applications to generate highquality output waveforms. In such techniques, carriers which can be used are triangular, saw-tooth and constant DC magnitude waveforms. The reference waveforms which can be used in PWM schemes are sinusoidal, sinusoidal injected with third harmonic and trapezoidal voltage waveforms. Currently, selective harmonics elimination which is also known as fundamental frequency switching has gained attention among researchers.

The cascaded MLI can be operated in both symmetric and asymmetric configuration. In the symmetric configuration, the magnitude of input DC sources is equal, due to which a number of output levels are less in addition to utilizing more number of switches with increased total harmonic distortion (THD). In contrast, asymmetric MLI input DC sources are unequal due to which different voltage levels can be generated. By combining such voltage levels more levels can be generated with a lesser number of switches with a consequent reduction in THD . In this research, two different 17 level symmetric and asymmetric multilevel inverters topologies are proposed, in the symmetric configuration, a new single phase hybridised cascaded multilevel inverter is proposed with stair-case modulation technique while the asymmetric multilevel inverter configuration is developed with

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switched capacitor unit. In addition, the comparison analysis between the inverter topologies are also taken up for detailed study .

II. LITERATURE SURVEY

Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control. This paper presents the most important topologies like diode-clamped inverter (neutral-point clamped), capacitor-clamped (flying capacitor), and cascaded multicell with separate DC sources. Emerging topologies like asymmetric hybrid cells and soft-switched multilevel inverters are also discussed. This paper also presents the most relevant control and modulation methods developed for this family of converters: multilevel sinusoidal pulsewidth modulation, multilevel selective harmonic elimination, and space-vector modulation. Special attention is dedicated to the latest and more relevant applications of these converters such as laminators, conveyor belts, and unified power-flow controllers. The need of an active front end at the input side for those inverters supplying regenerative loads is also discussed, and the circuit topology options are also presented. Finally, the peripherally developing areas such as high-voltage high-power devices and optical sensors and other opportunities for future development are addressed.

III. MULTI LEVEL INVERTER

The need of multilevel converter is to give a high output power from medium voltage source. The multi level inverter consists of several switches .Higher voltage can be generated using the devices of lower rating. Increased number of voltage levels produces better voltage waveform. Switching frequency can be reduced for the PWM operation.

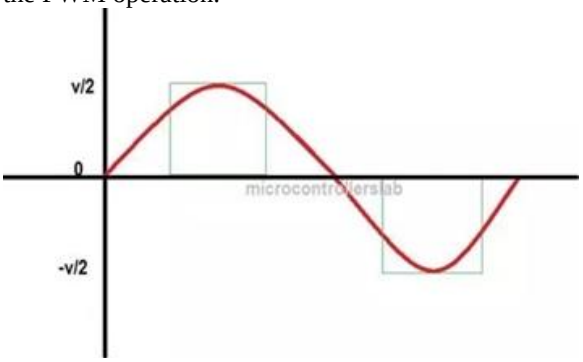

Fig1:output voltage waveform to two level inverter

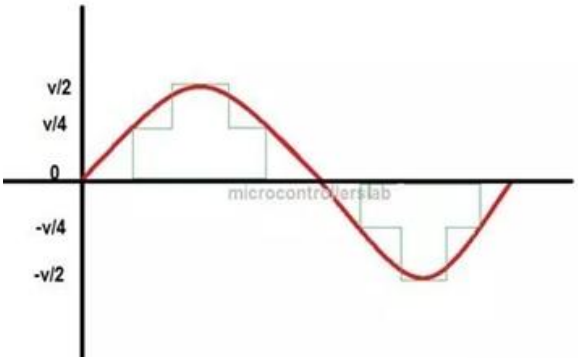

Fig 2:output voltage to five level inverter

How multilevel inverters Works:

The most common type of inverter which is used to generate AC voltage from DC Voltage is two level inverter. A two-level Inverter creates two different voltages for the load i.e. suppose we are providing *V* as an input to a two level inverter then it will provide + *V*/2 and – *V*/2 on output. In order to build an AC voltage, these two newly generated voltages are usually switched. Although this method of conversion of voltage is effective but it has some limitations as it causes disturbance in the output voltage. Normally this method works but in some applications it creates problems specifically where high distortion in the output voltage is not required. The concept of multilevel Inverter (MLI) is kind of modification of two-level inverter. In multilevel inverters we don't deal with the two level voltages instead in order to create a smoother stepped output waveform, more than two voltage levels are combined together. Smoothness of the waveform is directly proportional to the voltage levels, as we increase the voltage level, the waveform becomes more smoother but the complexity will be increased.

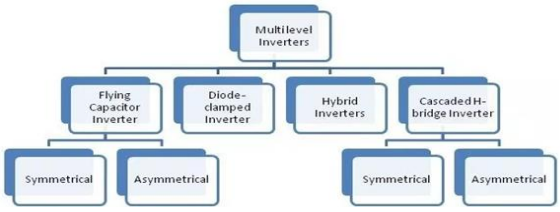

Fig3: Types of Multilevel Inverters

IV. HARMONICS

The typical definition for a harmonic is "a sinusoidal component of a periodic wave or quantity having a frequency that is an integral multiple of the fundamental frequency". Some references refer to "clean" or "pure" power as those without any harmonics. But such clean waveforms typically only exist in a laboratory. Harmonics have been around for a long time and will continue to do so. In fact,

musicians have been aware of such since the invention of the first string or woodwind instrument. Harmonics (called "overtones" in music) are responsible for what makes a trumpet sound like a trumpet, and a clarinet like a clarinet.

Electrical generators try to produce electric power where the voltage waveform has only one frequency associated with it, the fundamental frequency. In the North America, this frequency is 60 Hz, or cycles per second. In European countries and other parts of the world, this frequency is usually 50 Hz. Aircraft often uses 400 Hz as the fundamental frequency. At 60 Hz, this means that sixty times a second, the voltage waveform increases to a maximum positive value, then decreases to zero, further decreasing to a maximum negative value, and then back to zero. The rate at which these changes occur is the trigometric function called a sine wave, as shown in figure 1. This function occurs in many natural phenomena, such as the speed of a pendulum as it swings back and forth, or the way a string on a voilin vibrates when plucked.

The frequency of the harmonics is different, depending on the fundamental frequency. For example, the 2nd harmonic on a 60 Hz system is 2*60 or 120 Hz. At 50Hz, the second harmonic is 2* 50 or 100Hz..300Hz is the 5th harmonic in a 60 Hz system, or the 6th harmonic in a 50 Hz system.
Figure 5.2 shows how a signal with two harmonics would appear on an oscilloscope-type display, which some power quality analyzers provide.

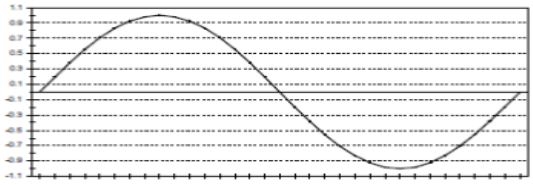

Fig4. Sine wave

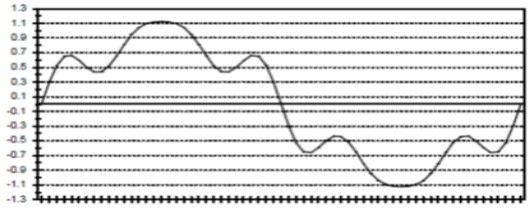

Figure5.. Fundamental with two harmonics

V. PROJECT DISCRIPTION AND CONTROL DESIGN

5.1 PROPOSED SYMMETRIC HYBRIDESED CASCADED MLI TOPOLOGY :

The hybridised H-bridge circuit topology utilized as a part of the development and implementation of the 17-level symmetric inverter is, as shown in Figure.. The operation of appropriate topology can be interpreted in terms of two-stages. In the first stage, the output levels +V1, 0, −V1 is delivered by the association of bidirectional switch to the second leg on H-bridge while in the second stage, the output levels +2V1, 0, −2V1 are generated. The generated five-level output voltage using symmetric basic hybridised cascaded MLI topology is depicted in Figure.2. The switching states representing the status of the basic MLI are given in Table 1

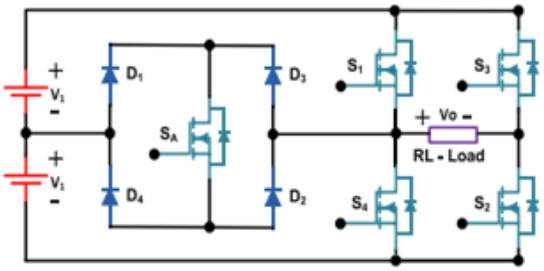

Fig 6: Basic Hybridised H-bridge topology.

Output voltage levels	Switching States				
Switches	S_1	S_2	S_3	S_4	S_A
+2 V	1	1	0	0	0
+1 V	0	1	0	0	1
0 V	0	1	0	1	0
0 V	1	0	1	0	0
-1 V	0	0	1	0	1
-2 V	0	0	1	1	0

TABLE:1Stable table of proposed basic hybridised MLI

A. CALCULATION OF CIRCUIT PARAMETERS

The following section discusses the choice of the number of sources, switches, and output voltage levels. In the symmetric hybridised and asymmetric multilevel inverters, the values of the dc sources are unequal so that number of output levels can be generated using a number of switches. It is assumed that the kth cell and pk are the same DC sources. In the proposed symmetric hybridised multilevel inverter the input DC sources are equal and the inverter equations can be written as follows

Vd1 = Vd2 = · · · · · · = Vdk = Vd (1)

The number of levels that can be determined is as follows where m is the no cell and n is the number of dc sources in each cell

N_{Levels} = 2mn + 1 (2)

The switches can be estimated as

N_{switch},k = 2pk + 1 (3)

The maximum output voltage can be estimated as

Vo = mnVd (4)

For the proposed asymmetric multilevel inverter the input DC sources are unequal and the equation can be written as

Vd1 = V1 = Vd (5)

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TABLE 2. Switching state table of 17-level symmetric MLI.

V_O	1	2	3	4	5	6	7	8	0		-1	-2	-3	-4	-5	-6	-7	-8
S_1	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S_2	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_3	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_4	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
S_5	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
S_6	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_7	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_8	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
S_9	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
S_{10}	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_{11}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_{12}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
S_{13}	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
S_{14}	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
S_{15}	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
S_{15}	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
S_A	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
S_B	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
S_C	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0
S_D	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0

TABLE2:Switching stable table of 17-level symmetric MLI

The proposed 17-level symmetric hybridized cascaded MLI is illustrated in Figure.3. In this topology, the operation of every H-bridge is similar to the basic Hybridised H-bridge topology as indicated in Figure. In this symmetric inverter, pulses are generated using staircase modulation scheme for obtaining different output voltage levels. The pulses are generated individually and fed to the first, second, third and fourth stage respectively and finally, all the outputs of the individual stages are combined to obtain the required output voltage. The control states of the power switches are illustrated in Table 2. In this proposed topology, all the input voltage sources are fixed as V = 25 V for acquiring the maximum peak to peak voltage of 200 V at the load ends. The loads used for testing are 100 ☐ resistor and 175 mH inductor respectively. The voltages at various stages, output voltage and current are shown in Figure

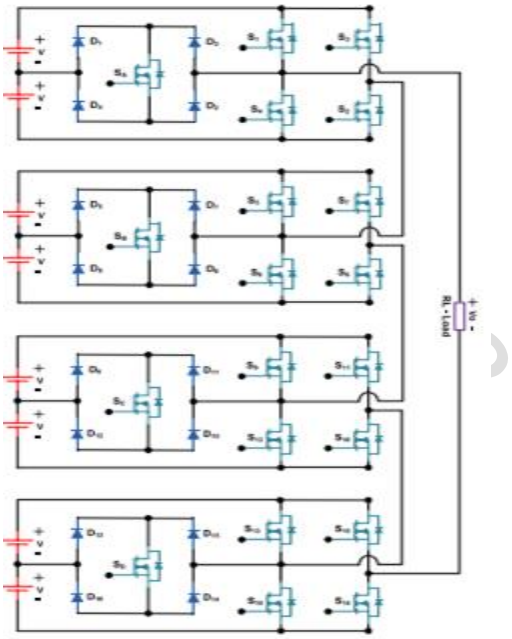

Fig7: Proposed 17-level symmetric MLI.

5.2 PROPOSED ASYMMETRIC SWITCHED CAPACITOR MLI TOPOLOGY

The basic proposed switched capacitor topology is as shown in Figure.5 (a). The proposed topology consists of switched capacitor unit, diode, supply voltage and two switches. The switched capacitor doubles the input voltage at the load ends. When the input voltage is applied to circuit the capacitor 'C' will charge through the S2 switch and discharge through S1, the proposed topology produces +V and +2V voltage levels at the load ends with a lesser number of switches. Figure.5 (b) shows the switching patterns for the switches S1 & S2, voltage across the capacitor during

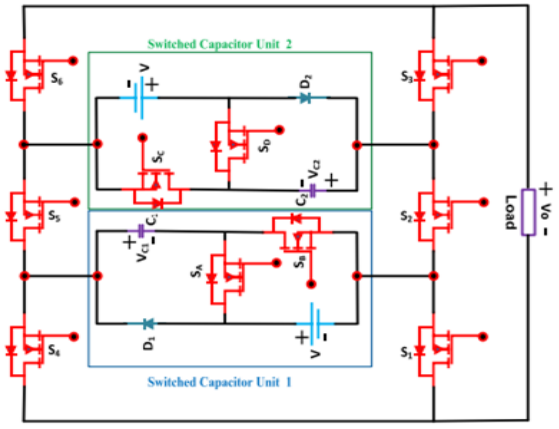

FIG8: Proposed 17-level aymmetric switched capacitor MLI

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TABLE 3. Switching state table of 17-level asymmetric inverter.

V_O Level	S_1	S_2	S_3	S_4	S_5	S_6	S_A	S_B	S_C	S_D	Output voltage level expression	Output Voltage (V)
1	1	0	1	0	1	0	1	0	0	1	$4V+V_{c1}+V_{c2}$	100
2	1	0	1	0	1	0	0	1	0	1	$4V+V_{c2}$	87.5
3	0	0	1	1	1	0	0	1	1	1	$3V+V_{c2}$	75
4	1	0	1	0	1	0	1	0	1	0	$4V+V_{c1}$	62.5
5	1	0	1	0	1	0	0	1	1	0	4V	50
6	0	0	1	1	1	0	0	1	1	0	3V	37.5
7	1	0	0	0	1	1	1	0	0	0	$V+V_{c1}$	25
8	1	0	0	0	1	1	0	1	0	0	V	12.5
9	1	1	1	0	0	0	0	1	1	0	0	0
10	0	1	1	1	0	0	0	1	0	0	$-V_2$	-12.5
11	0	1	1	1	0	0	1	0	1	0	$-V-V_{c1}$	-25
12	1	1	0	0	0	1	0	1	1	0	-3V	-37.5
13	0	1	0	1	0	1	0	1	1	0	-4V	-50
14	0	1	0	1	0	1	1	0	1	0	$-4V-V_{c1}$	-62.5
15	1	1	0	0	0	1	0	1	0	1	$-3V-V_{c2}$	-75
16	0	1	0	1	0	1	0	1	0	1	$-4V-V_{c2}$	-87.5
17	0	1	0	1	0	1	1	0	0	1	$-4V-V_{c1}-V_{c2}$	-100

Table:3:Switching stable table of 17-level asymmetric inverter

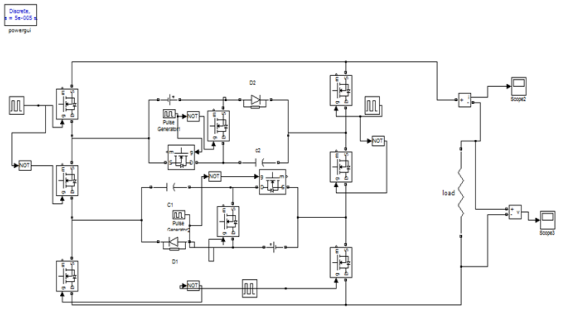
Type of inverter configuration	Output Parameters							
	Type of Load	Output Peak-Peak voltage (Volts)	Output RMS voltage (Volts)	Output Peak-Peak current (Amps)	Output RMS Current (Amps)	Frequency (Hz)	Output Power (Watts)	THD (%)
17-level Symmetric	R -load	200	67.92	4	1. 404	50	95.35	5.41
17-level Symmetric	L -load	200	67.91	3.5	1.156	50	77.07	
17-level Asymmetric	R -load	200	72.72	2	0.7	50	50.9	4.54

Table4: Output experimental results

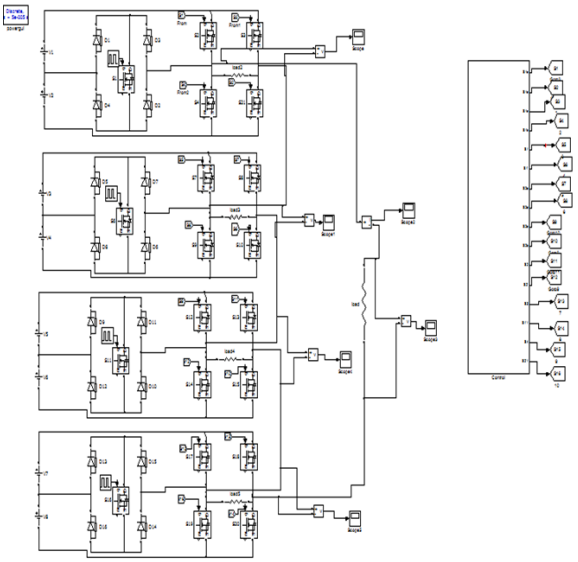
VI.SIMULATION RESULTS

The simulation results for 17 level inverter systems has been implemented and tested in simulation. The proposed multilevel inverter prototype model is shown in Figure. The staircase modulation PWM technique is used to generate gate pulses and the same is implemented in MATLAB and the Simulink block sets are dumped into dSPACE RTI 1104 digital I/O ports. The digital I/O ports have 20 output pins for real-time interfacing application. The generated pulses from the dSPACE RTI 1104 is given to input as TLP 250 driver. The gate driver will boost the PWM pulse pattern from 5 V to 15 V because 15 V pulses will be more appropriate to turn on the power switches. The simulation model specifications are given in Table.4. The results are validated at steady state, load disturbance conditions and also performed with resistive & inductive loads and THD which are shown in Figure.

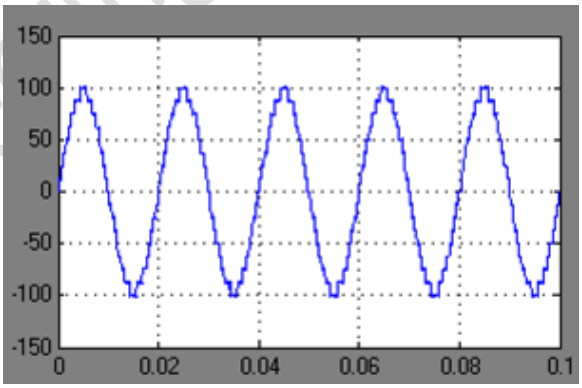
6.1 ASYMMETRICAL 17 LEVEL MLI FOR R LOAD



6.2 SYMMETRICAL 17 LEVEL MLI FOR R LOAD:



7.4 SIMULATIONWAVEFORMS



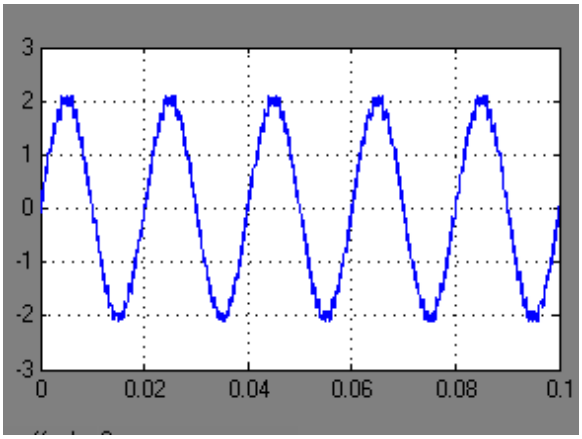


Fig9: voltage and current wavefoems of symmetrical 17 level mli for r load

On & off period of the switch and the output voltage across the load, whenever the capacitor charges, the load voltage is equal to the input voltage and capacitor also charges to the input voltage i.e. 12.5 v. During discharge time, the load voltage is the sum of the input voltage and capacitor voltage which will be 25 v. The results show that the output voltage is doubled during capacitor discharge time. Using this topology more output voltage can be obtained for multi-levels with the minimum input voltage. The proposed 17 level switched capacitor topology is shown in figure.6. The proposed topology consists of two switched capacitor unit, having two capacitors, two diodes, two supply voltage sources and ten switches. The proposed switched capacitor units generate 17 levels at load end with 200 v (peak to peak). The pulses are generated individually and fed to the switched capacitor units and finally, all the outputs of the individual units are combined to obtain the required output voltage. The switching logic is as given in table.3. For the proposed switched capacitor unit 1 and 2 waveforms and output voltage and current waveforms are shown in figures.7(a),(b) & (c) respectively. The proposed 17 level inverter voltage expression and level voltages are presented in table. 3.

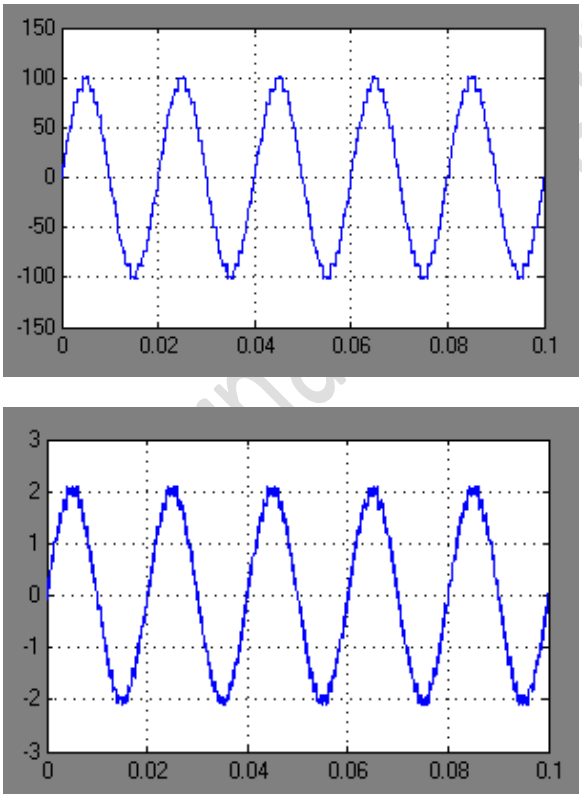


Fig10: total voltege and current waveforms of symmetrical 17 level mli for rl load

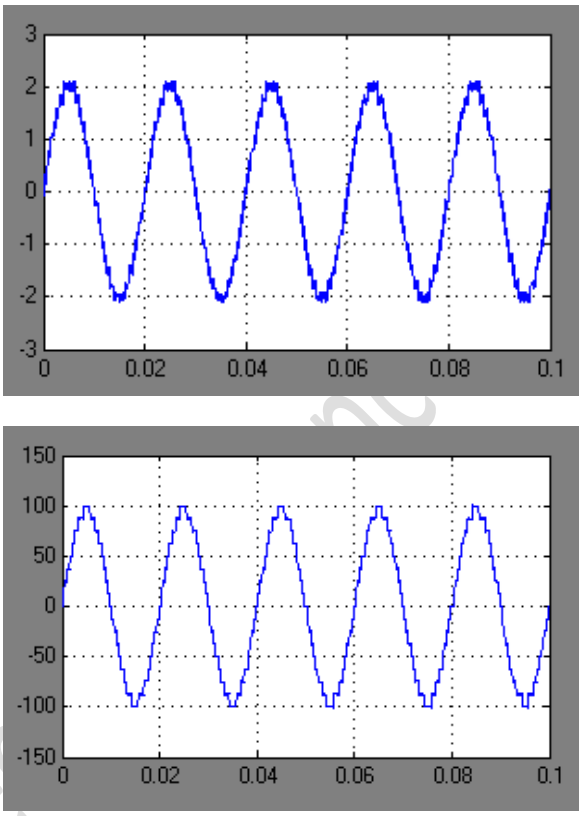


Fig11: total voltage and current waveform of asymmetrical 17 level mli for r load

VII. CONCLUSIONS

This research presents the implementation and analysis of a 17 level symmetric and asymmetric multilevel inverters. The proposed 17 level inverter systems have been effectively tested with unity and lagging power factor loads. In case A, testing has been carried out under steady-state condition, load disturbance conditions and analysis of THD with 17 level symmetric inverter output were presented. It is inferred from case A results that the system is readily adaptive and maintains a stable output voltage with 5.41 % THD for the aforesaid conditions while in case B, a THD with 4.54 % has been achieved, which is on par with IEEE standards. During load disturbances, the proposed topology is suitable for sudden load variant applications also. Due to low THD, these topologies inherently utilize a lesser number of switches and a minimum number of dc input voltage sources; hence, the volume density of the proposed inverter is observed to have improved. From case A and B results it can be inferred that the proposed topology multilevel inverters are suitable for renewable energy-fed applications.

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