Journal of Engineering Sciences
Vol 10, Issue 9, Sept /2019
ISSN NO:0377-9254

DESIGN OF EFFICIENT BCD ADDERS IN QUANTUM DOT CELLUAR AUTOMATA

[1]NANDIGRAMA DATTA PRABHAKAR RAO, [2]E.NAGESWAR RAO
[1]M.Tech Student,[2]Associate Professor
Department of ECE
KAKINADA INSTITUTE OF TECHNOLOGICAL SCIENCES (KITS), RAMACHANDRAPURAM.

Abstract: Among the emerging technologies recently proposed as alternatives to the classic CMOS, Quantum-dot cellular automata (QCA) is one of the most promising solutions to design ultra lowpower and very high speed digital circuits. Efficient QCA-based implementations have been demonstrated for several binary and decimal arithmetic circuits, but significant improvements are still possible if the logic gates inherently available within the QCA technology are smartly exploited. This brief proposes a new approach to design QCA-based BCD adders. Exploiting innovative logic formulations and purpose designed QCA modules, computational speed significantly higher than existing counterparts are achieved without sacrificing either the occupied area or the cells count.

Keywords: QCA, CMOS, BCD

I. INTRODUCTION

Quantum-dot cellular automata(QCA) has been recognized as one of the technologies that may replace field-effect transistor (FET)-based computing devices at the nano-scale level. Current complementary metal oxide semiconductor technology is going to approach a scaling limit in deep nanometer technologies. The current silicon transistor technology faces challenging problems, such as high-power consumption and difficulties in feature size reduction. Nanotechnology is an alternative to these problems, and the international technology roadmap for semiconductors (ITRS) report summarizes several possible technology solutions. Quantum-dot cellular automata(QCA) is a nanotechnology that offers a new method of computation and information transformation

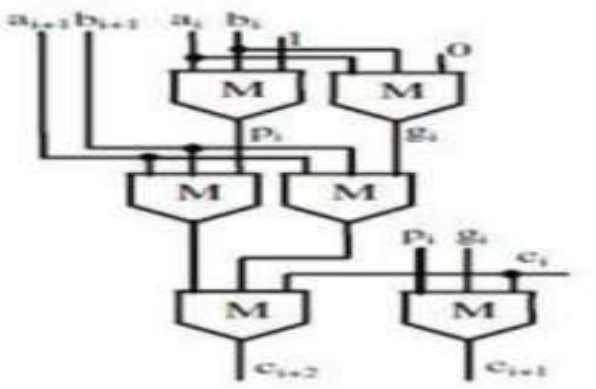


Fig 1: Novel 2-bit QCA module.

The main objective of this paper is to perform both BCD addition and BCD subtraction in a single circuit with minimum number of garbage gate count and constant input. To achieve the operation of reversible BCD addition and subtraction in a single circuit two new gates are proposed which are optimized such that it doesn't possess any restrictions of reversible gates as mentioned above. It has been proved that the proposed reversible BCD arithmetic circuit is better than the existing logics in the literature; in terms of number of garbage outputs, constants inputs and the gate count

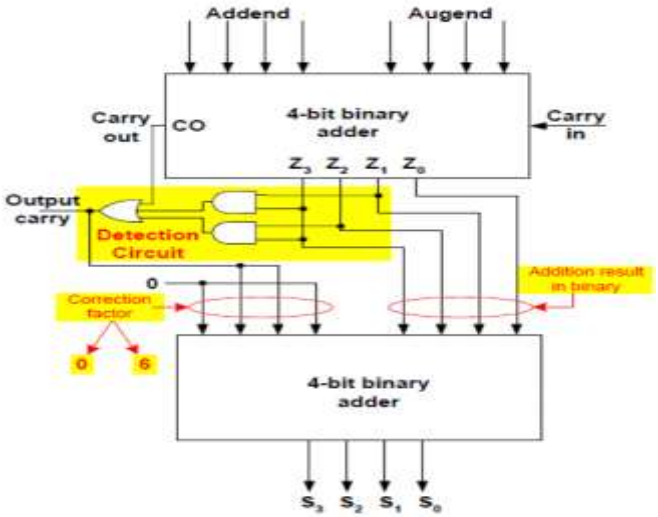
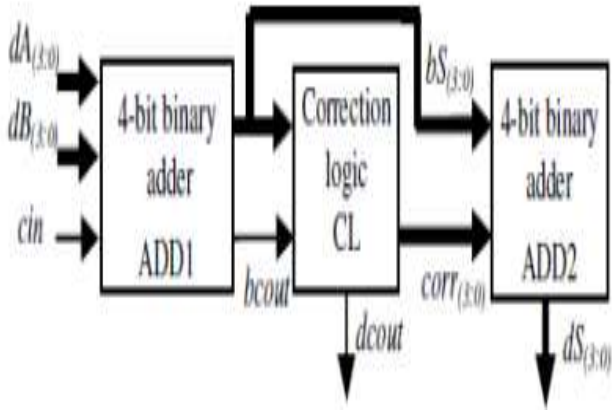


Fig 2: The conventional block diagram of BCD.

II. RELATED WORK

The QCA BCD adders proposed earlier in [12], [13] use a top level architecture shown in Fig. 5. In this first block adds two input numbers in binary format, carry is evaluated by a logic function in sum, carry output of the 4-bit adder block and then perform conversion from binary result to BCD number by adding 6 to the result if the binary sum in the

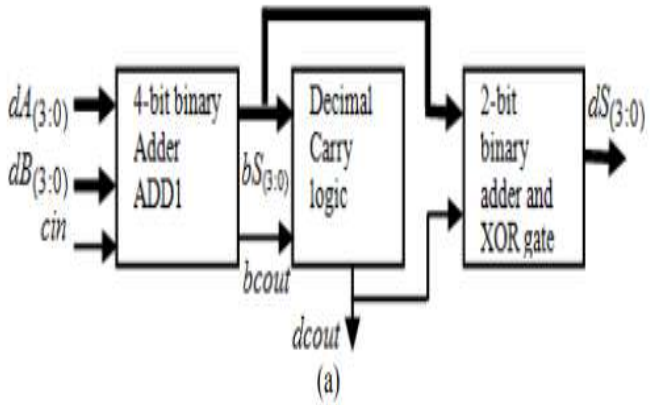
first block is greater than 9, otherwise 0. A ripple carry adder is used to implement binary addition in [13], whereas two types of implementations presented in [12] make use of a carry flow adder [9] and a carry-look-ahead adder [7]. A serial decimal adder demonstrated in [11] using the Johnson-Mobious Code (JMC).

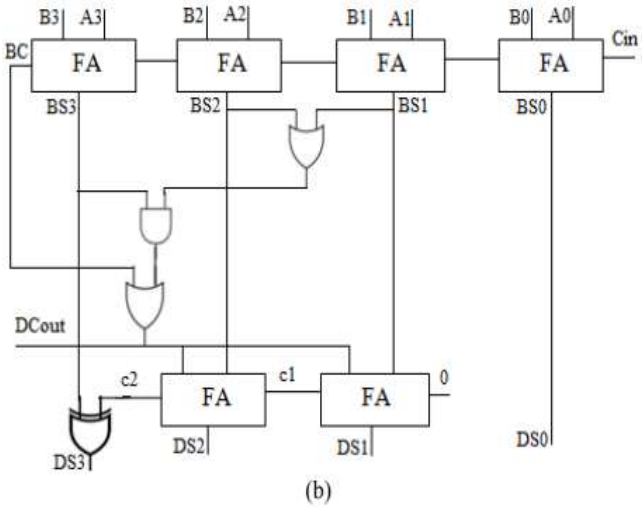


Block diagram of 1-digit BCD adder

III. PROPOSED SYSTEM

The architecture of the 1-digit BCD adder proposed in this paper is depicted in Fig.6(a), in this the first block is a 4-bit binary adder (ADD1), which adds two input BCD numbers along with input carry and produce binary sum and carry bS(3:0) and DCout respectively. From the result of ADD1 the decimal carry expression is given in (11). A 2-bit binary adder and an XOR gate are used to convert the binary sum bS(3:0) and decimal carry output DCout to decimal sum dS(3:0). The logic functions for converting binary sum to decimal sum are given in (12). The digital logic circuit of BCD adder using (11) and (12) is depicted in Fig. 6(b). The binary sum is denoted as BS0, BS1, BS2, BS3, carry of ADD1 as BC, decimal sum DS0, DS1, DS2, DS3, decimal carry DCout and internal carries of decimal are c1,c2.





BCD adder: (a) Architecture, (b) logic diagram

$DCout = (BC, (bS3, M(bS2, bS1, 1), 0), 1)\ (11) = BC + bS3\ (bS2 + bS1)$

$dS0 = bS0$

$c1 = (DCout, bS1, 0)$

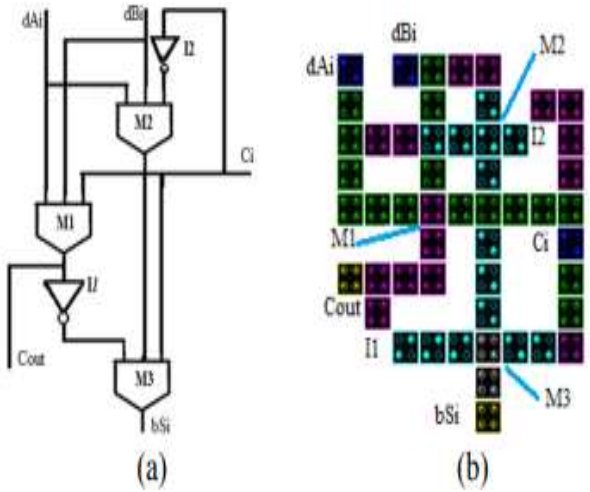
$dS1 = (\overline{c1}, (DCout, dS1, 1), 0)$

$c2 = (DCout, bS2, c1)$

$dS2 = (\overline{c2}, (DCout, bS2, 1), 0)$

$dS3 = ((bS3, c2, 0)\overline{\ }, M(bS3, c2, 1), 0)$

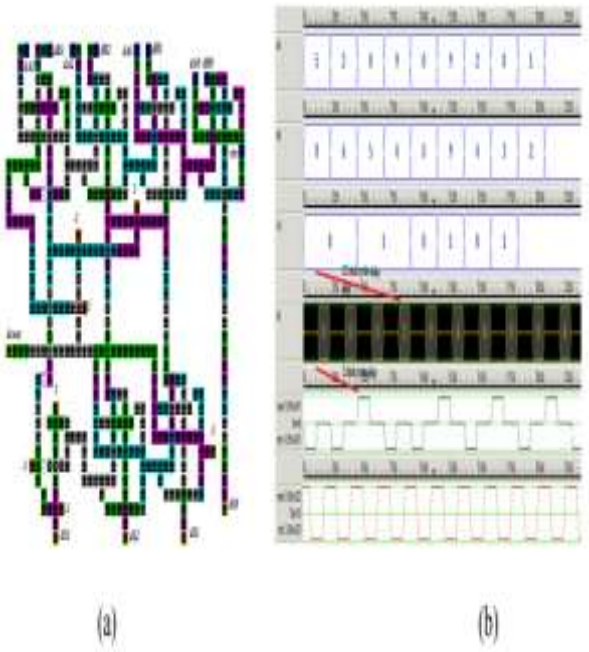
Design of an Optimal Decimal Adder in Quantum Dot Cellular Automata



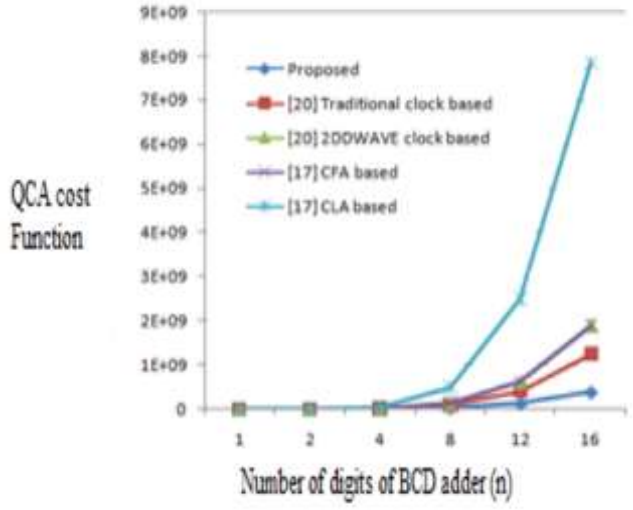
Area optimized full adder: (a) block schematic, (b) QCA layout.

QCA Implementation of 1-Digit BCD Adder

A QCA layout of 1-digit BCD adder is designed for the novel BCD adder architecture given in Fig. 6(a) is implemented using six area optimized full adders, one XOR gate and three majority gates for carry logic given in eq. (4) and eq. (5). The QCA layout is depicted in Fig. 8(a), designed with 526 cells, it occupies 0.57µm2 area, the delay of the output carry is 2 cycles and delay the delay of decimal sum is 3.5 clock cycles. The layout is simulated in QCA design tool, QCADesigner [8]. The simulation results of the 1-digit BCD adder are depicted in Fig. 8(b), the delay of the output sum and carry are shown in the simulation waveforms. The results obtained in this proposed adder are compared with its existing counterparts in section 5.



BCD adder: (a) QCA layout, (b) simulation results

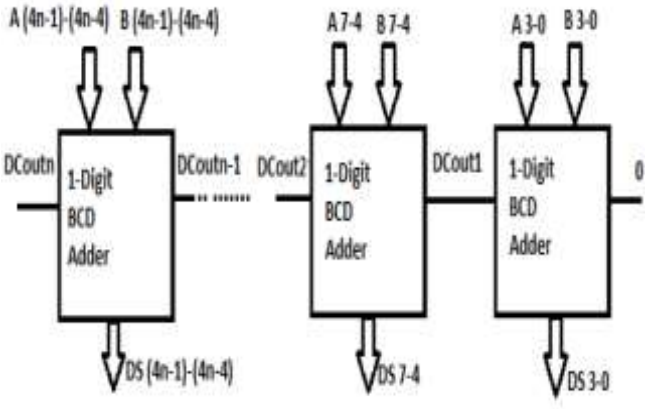


Comparison of QCAcost functions of different n-digit BCD adders.

IV. ALGORITHM

Architecture of Proposed n-Digit BCD Adder

An efficient n-digit BCD adder is designed by cascading n one digit BCD adders. In the proposed design a 1-digit adder produce output carry with two clock cycles delay, and output sum with 3.5 clock cycles delay, this is an early carry generation. In an ndigit BCD adder design before finding sum digit, it propagates carry to the next digit with that it reduces the total delay of an n-digit adder. The delay of 1-digit BCD adder is 3.5 clock cycles, but the delay of a 2-digit BCD adder is only 5.5 clock cycles. Therefore the delay of an n-digit BCD adder can expressed as 2n + 1.5 number of clock cycles. The architecture of an n-digit BCD adder is depicted in Fig. 10, input digits are represented with A, B, output digits represented with DS and output carry of n th digit adder is represented with DCoutn.



Top level architecture of n-digit BCD adder.

V. COMPARISON OF RESULTS

In this section results obtained from the proposed novel QCA BCD adder are compared with the results of different existing counterparts [10-14]. In the proposed design the coplanar wire crossovers are preferred to reduce the circuit complexity. In a QCA design number of clock cycles, area and number cells are the design metric before defining QCA cost function [10]. The comparison of clock cycles, area and number of cells in proposed 1-digit BCD adder with its existing counterparts are given table 1. There is significant reduction in area and number of QCA cells with optimum number of clock cycles. The area of proposed design is reduced by 36% to 75%, further the QCA cell count is reduced by 43% to 71%. The design performance can be compared with QCA cost function [10] in eq. (1), selected l = 2, k = 2 and p = 2. To evaluate the cost function of a 1-digit BCD adder here considered the number of majority gates is M, number of inverters is I, number of coplanar wire crossovers Ccp, the number of multilayer crossovers Cml and the number of clock cycles T. The proposed BCD adder design require M = 24, I = 13, Ccp = 12, Cml = 5 and its delay T = 3.5 clock cycles. A BCD adder design presented in [20] using traditional clocking scheme needs M = 29, I = 8, Cml =27 and its delay T = 3 clock cycles, whereas using 2-D wave clocking (2DDWAVE) [20] it needs M = 29, I = 8, Cml =29 and its delay T = 3.5 clock cycles. A BCD adder presented in [17] using Carry Flow Adders (CFA) requires M = 24, I = 14, Cml = 18, its delay T = 3.5 clock cycles and using Carry Look-ahead Adders (CLA) it requires M = 35, I = 13, Cml = 56, its delay T = 2.5 clock cycles. And a BCD adder presented in [19] requires M = 27, I = 16, Cml = 27, its delay T = 8 clock cycles. These design metrics used to find QCA cost function in eq. (1) [11]. The results of cost function for different 1- digit BCD adders are given in table 2. The QCA cost function evaluated from proposed 1-digit BCD adder shows significant improvement, the cost function is reduced by 75% to 95% with existing designs. The QCA cost function of n-digit BCD adders for n = 1, 2, 4, 8, 12 and 16 are estimated by the cost function given in eq. (1) [10], and plotted in Fig. 9, shows there is a reduction in QCA cost function, for 16-digit BCD adder cost function is reduced by 69% to 95% in comparison with existing designs [11-14]. The increase in cost function of proposed designs are linear for numbers digits (n) where increase for other designs is very high and nonlinear as shown in

Table 1: Area, Cell count and Clock cycles Comparison of 1-digit QCA BCD Adders

BCD Adder	No. of cells	Area (μm^2)	No. of clock cycles
[14] Traditional clock based	1065	0.89	3
[14] DDWAVE clock based	1196	1.36	3.5
[12] CFA based	932	1.36	4.75
[12] CLA based	1838	1.86	2.5
[11] Serial adder	1130	1.77	10
[13] Ripple carry BCD adder	1348	2.28	8
Proposed	526	0.57	3.5

Table 2: QCAcost Function Comparison of 1-digit BCD Adders

BCD Adder	QCA_{cost} function
[14] Traditional clock based	66,690
[14] 2DDWAVE clock based	103,120
[12] CFA based	79,104
[12] CLA based	184,137
[13] Ripple carry BCD adder	467,584
Proposed	16145

VI.. CONCLUSION

In this paper, design of an area efficient BCD adder is presented. To optimize the BCD adder an area optimized QCA full adder is used to perform the binary addition. The QCA layout is designed and simulated using the tool QCADesigner. The results of the proposed design shows, there is significant improvements in terms QCA design metrics. Finally, the results confirm that the proposed design reduced the complexity, area and cell count, without compromising in the delay, in comparison with existing designs. In QCA technology there is a future scope to design complex combinational, sequential circuits, memories, ALU and different processors using proposed area optimized full adder. The efficient BCD adder proposed in this paper can be used to implement ALU.

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