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DESIGN OF PARALLEL PREFIX ADDER AND SUBTRACTOR USING MAJORITY LOGIC FORMULATIONS

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ABSTRACT: The New Technology is quantum dot cellular automata at Nano metric scale, which has more focal points like lower area(PLBs) requirement and low Power Consumption. , Transistors can't lesser than their present size .The QCA rationale approach speaks to one of the potential arrangements in beating this physical edge, level. Using this QCA innovation we created AND gate, OR gate and NOT gate. we can perform any Digital Logic Function, With the avail of Universal gates In this paper ,fast adders like Brent-Kung adder(BKA), Kogge-Stone Adder(KSA) and ladner fischer adder by utilizing Majority gates that has all best in class contenders and accomplishes the best area-delay tradeoff. At last looked at the changed properties like delay (speed), power utilization, area, ADP and PDP.

Keywords - Adders, quantum-dot cellular automata (QCA), Delay, power consumption, Majority gates (MG)

1.INTRODUCTION

The QCA are an appealing rising innovation reasonable for the improvement of ultra-thick low-control elite advanced circuits. Hence, over the most recent couple of years, the plan of productive rationale circuits in QCA has gotten a lot of consideration. Exceptional endeavors are coordinated to number-crunching circuits, with the primary intrigue concentrated on the twofold expansion that is the essential activity of any advanced framework. Obviously, the models regularly utilized in customary CMOS plans are viewed as a first reference for the new structure condition. RCA, CLA, and restrictive whole adders. The CFA was an advanced RCA that moderated effects of impending cables. Parallel prefix structures have been dissected and updated in QCA including Bent kung adder, kogge-stone adder and Han Carlson adder. For the CLA and RCA ,increasingly effective structures have been proposed. In this short, an inventive procedure is introduced to execute fast low-zone adders in QCA. Theoretical definitions displayed for CLA and parallel-prefix adders are here mishandled for the affirmation of a novel 2-piece extension cut. The last empowers the bring to be multiplied through two following piece positions with the deferral of just a single larger part MG. Similarly, the sharp top level building prompts traditionalist configurations, as needs be avoiding unnecessary clock stages as a result of long interconnections. A viper arranged as proposed continues running in the RCA style, yet it shows a computational concede lower than all condition of the-workmanship contenders and accomplishe.s the most decreased ADP.

2.ESSENTIALS OF QUANTUM-DOT CELLULAR AUTOMATA

QCA cells are coulombically represented by partners with adjacent cells to influence the polarization of each other. In review some direct ,yet main, QCA rational contraptions in continuing with subsections: a larger portion of the entrance, QCA cables and gradually complicated QCA cell blends. The main contraction in QCA is a QCA cell that allows data to be computed and transmitted. A QCA cell has a hypothetical square room that includes four electronic regions and two electrons .The goals of the contraptions called dots and address the area that electrons can have. The bits are combined by impediments to quantum mechanical tunneling and electrons can tunnel through them depending on the structures state. Unequivocally two flexible electrons are stacked in the phone and can move to different quantum touches in the QCA cell by strategies for electron tunneling. Tunneling ways are addressed by

the lines partner the quantum spots in Figure 1. Coulombic repulsiveness will cause the electrons to include only the sides of the QCA cell achieving two unequivocal polarizations.. Electron tunneling is thought to be total controllable by potential barriers that can be raised and brought down by strategies for capacitive plates between nearby QCA cells.

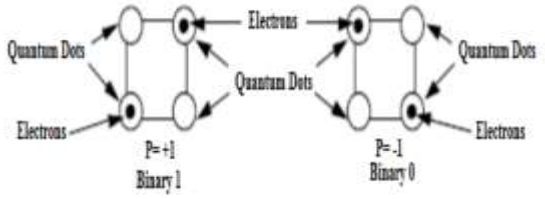

Figure 1. QCA cell polarizations and representations of binary 1 and binary 0

There are two vigorously irrelevant approaches of two electrons in the QCA cell for an evacuated cell, expected cell polarization P=+1 and cell polarization P=-1.while Cell polarization P=+1 alludes to parallel 1 while cell polarization P=-1 alludes to relating 0.In expansion, this thought is graphically potrayed in figure - 1.It is additionally colossal that there is an unpolarized state as well. In an unpolarized state, potential points of confinement between contact are diminished which diminishes the exhibit generally zero polarization and the two electron wave limits have been delocalized over the telephones appeared in Figure 2

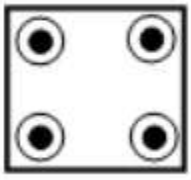

Fig 2.unpolarized cell

The numbering of specks signified by I in the phone goes clockwise beginning from the dab on the upper appropriate with I =1, base right dab I =2, base left spot I =3, and upper left dab i=4. The polarization P in a cell is characterized as Where Pi means the electronic charge at speck I. The polarization estimates the charge design for example the degree to which the electronic charge is appropriated among the four dabs.

The basic QCA sensible circuit is the three-input greater part rationale door that shows up in Figure 2.4 from which progressively complex circuits can be fabricated. The fundamental dominant part entryway is acquired by setting four neighboring cells bordering to a gadget cell, which is in the center. Three of the side cells are utilized as data sources, while the staying one is the yield. The gadget cell will consistently expect the lion's share polarization is where there will be at least electron aversion between the electrons in the three information cells and the gadget cell.

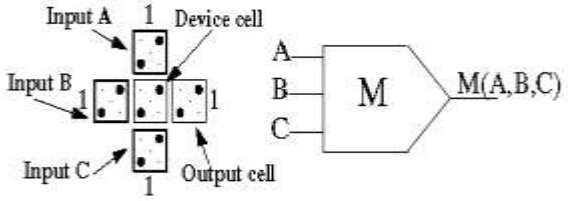

Fig 3.Majority gate using QCA

Consider the coulombic interface between cells 1 and 4,cells 2 and 4,cells 3 and 4 to perceive how the contraption cell accomplishes its most minimal imperativeness state (and from now on P=+1 in figure2).Typically, coulombic association between electrons in cells 1and 4 would make 4 change its polarization in light of electron stun. (expecting cell 1 is a data cell). In any case, cells 2 and 3 in like manner sway the polarization of cell 4 and have polarization P=+1. Along these lines, in light of the way that the greater part of the cells influencing the contraption cell have polarization 1 P , it additionally will moreover expect this polarization because the forces of Coulombic association are more grounded for it than for 1.

3. EXISTING METHOD:

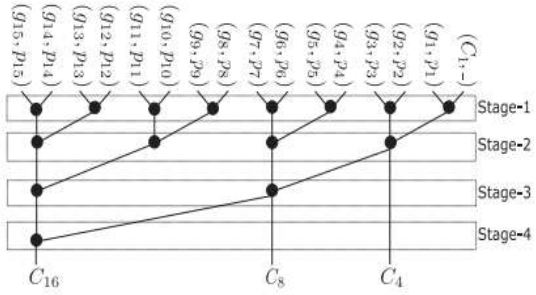

Fig.4. Conventional prefix graph of carry C16.

$$(g_i, p_i) \circ (g_j, p_j) = (g_i + p_i p_j, p_i p_j)$$

$$(C_4, \_) = (g_3, p_3) \circ (g_2, p_2) \circ (g_1, p_1) \circ (C_1, \_).$$

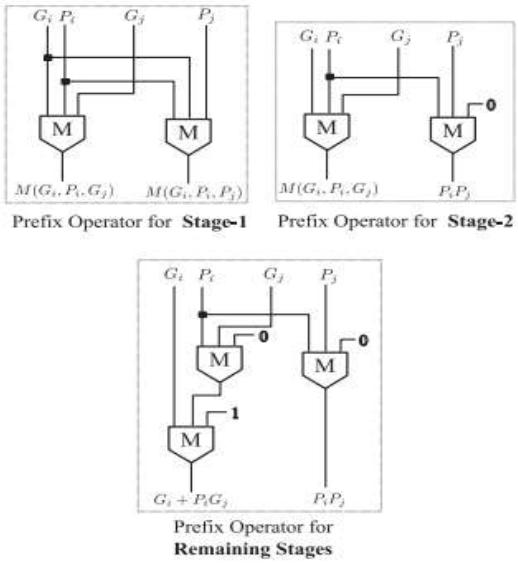

Fig.5. Prefix-Adder associative operator.

The carry C16 is figured utilizing the prefix affiliated operator with the end goal that produce gi= ai.bi and engender pi = ai+ bi. Fig. 4 demonstrates its prefix diagram. In this segment, another acquainted operator is introduced as far as lion's share rationale for acquiring a structure with decreased intricacy (regarding number of doors and postponement in the adder plan)

The motivation for this new administrator's importance is as per the following. The present administrator needs three greater parts ,has deduced crisp qualities to diminish the quantity of prevailing lion's share entryways for this current administrator. All things considered, this can be additionally upgraded on the premise that it lessens the measure of greater part entryway for the viper's just explicit stages. Each prefix activity in the plan (fig 4) needs two lion's share entryways for stage - 1 and stage-2 each, while the rest of the stages require three greater part entryways each.In all phases of prefix advancement, the proposed plan needs just two lion's share entryways.. The proposed arrangement requires only two larger part doors in all periods of prefix development and thoroughly decreases the measure of the checks of gi and pi.

4. PROPOSED ADDERS:

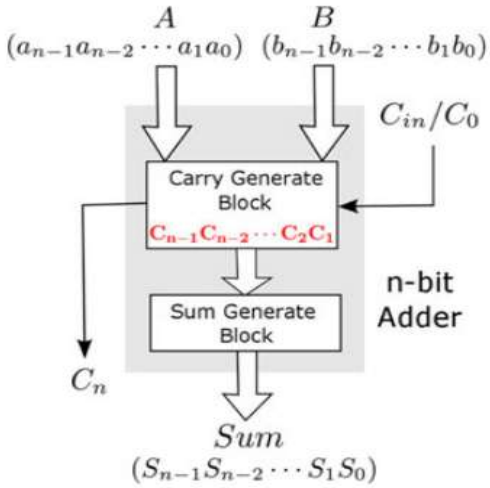

Fig. 6. Block diagram of n-bit binary adder

Fig. 6 demonstrates the chart of a n-bit parallel adder. The contributions to the adder are given by A = a n-1 a n-2 ... a1a0, B= bn-1 bn-2 ... b1b0 and Cin while Sum =Sn-1 sn-2 ... S1S0 and the convey Cn are the yields. Numerous methodologies have been proposed for figuring Sum and Cn productively. These include adders of the CLA and the prefix. While CLA provides a way to quickly expand two operand, fan out confines have led prefix adders to be improved to reduce the convey count to a 'Prefix' calculation.

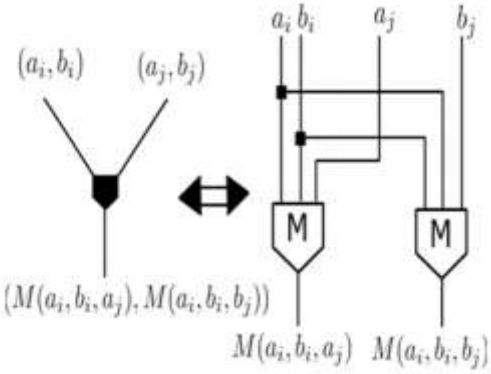

Fig. 7. Proposed prefix operator symbol and majority gate diagram.

Fig. 7 demonstrates the proposed prefix administrator image and the greater part entryway graph. Fig. 7shows the proposed prefix chart for computing C16. The lion's share door graph of C16 is appeared in Fig. 8(the proposed prefix affiliated administrator is set apart with dabbed lines in Fig. 8)

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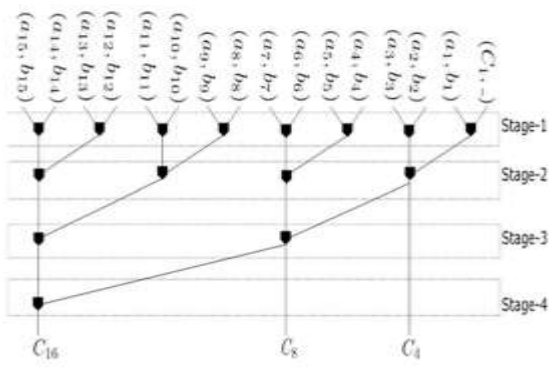

Fig. 8. Proposed prefix graph of carry C16.

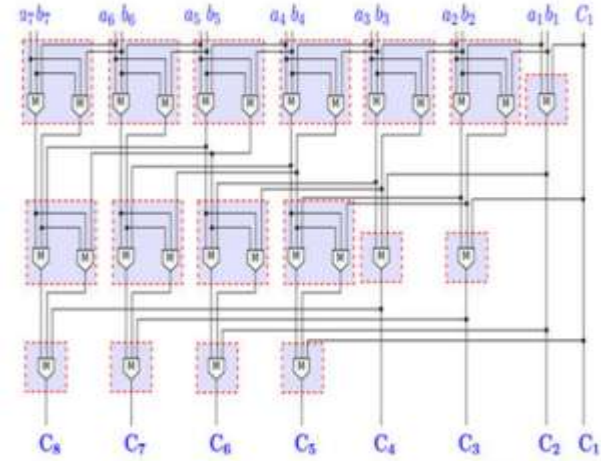

Fig 9-a: Majority gate diagram of proposed Kogge-Stone adder

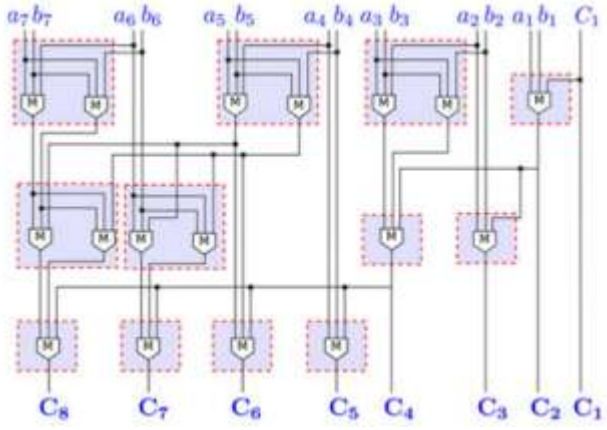

Fig 9-b: Majority gate diagram of proposed Ladner Fischer adder

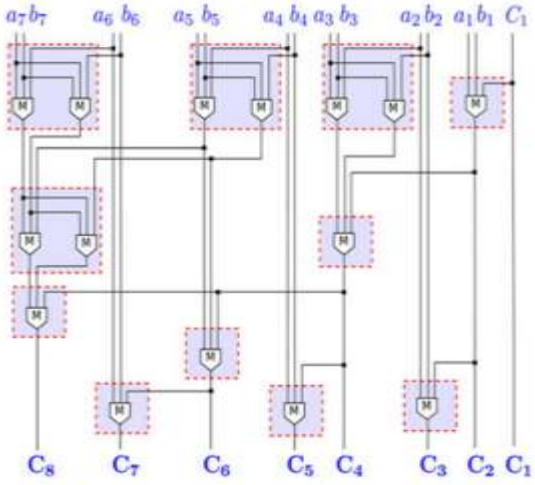

Fig 9-c: Majority gate diagram of proposed Brent-Kung adder

The suggested administrator prefix is directly suitable for a broad spectrum of adder prefixes.T his paper considers three kinds of prefix adders to be specific adders of KSA, LFA, and BKA. The proposed MAJ gates charts for different prefix adders are appeared in Fig. 9. Fig. 9a demonstrates the proposed MAJ gate chart of 8-bit KSA; it requires 3 phases and 4 Maj gates delay for computation all things considered, so log2n stages for estimation of all conveys in a n-bit adder. Fig. 9b demonstrates the proposed dominant Maj gate chart of 8-bit Ladner-Fischer adder; it requires three phases and four MAJ gates delay for estimation all things considered. A n-bit LFA requires log2n stages for estimation all things considered. Fig. 9c demonstrates the proposed dominant Maj gate outline of a 8-bit BKA. It requires five phases and causes in a six larger MAJ gates delay for the estimation all things considered. A n-bit BKA requires 2log2n one phases for the count of the conveys. The proposed prefix charts of KSA, LFA, and BKA are like the regular prefix-diagrams [2], [3], [4], the huge distinction is that the proposed prefix diagrams don't require the much count of the gi and pi arrays.

5. PROPOSED SUBTRACTORS:

In the previous a few circuits dependent on QCA are structured yet are danger to changes, vigor and absence of effectiveness regarding cell number and zone. In this paper effective full adder and full subtractor requesting lesser cell region, lesser vitality

scattering alongside less number of lion's share entryways utilizing single layer coplanar wire intersection have been proposed. Moreover a n-bit full adder and subtractor additionally has been structured.

1-bit Full Subtractor

A full subtractor is utilized to plays out the subtraction of two info An and B with acquire input C. The two yield of subtractor circuit are contrast 'D' and acquire 'B'. So the outflow of 1 bit full subtractor can be composed by

$$B_o = A'B + BC + CA'$$

$$D = ABC + A'B'C + A'BC' + AB'C'$$

To execute full subtractor in QCA it required to speak to the articulation as far as MGs, which can be given by

$$B_o = M_3(A', B, C)$$

$$D = M_5'(A', B, C, B_o', B_o')$$

The schematic depiction of full subtractor circuit is appeared by Fig.10. The utilization of 5-input lion's share door make the circuit more straightforward than utilizing just 3-input MG and inverter.

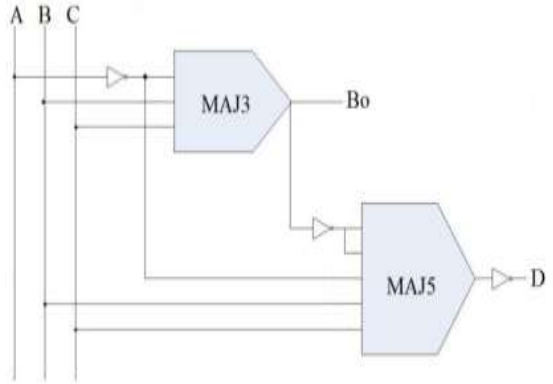

Fig. 10. Schematic of Full Subtractor design

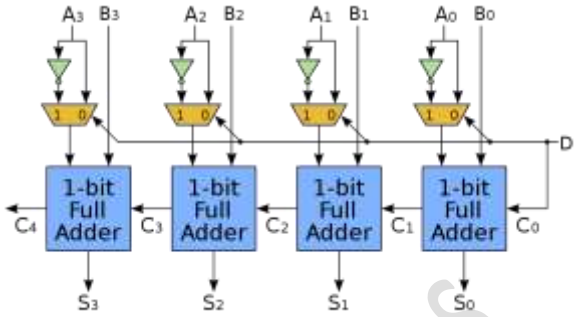

Fig. 11. N-bit adder and Subtractor

Having a n-bit adder for An and B, by then S = A + B. By then, acknowledge the numbers are in two's enhancement. By then to perform B − A, two's enhancement theory says to change each piece with a NOT door by then incorporate one. This yields S = B + A bar + 1, which is definitely not hard to do with a to some degree balanced adder.

The control input D that is furthermore connected with the basic pass on, by then the modified adder performs addition when D = 0, or difference when D = 1.

This works since the A commitment to the adder is incredibly A n when D=1 and the transmission in is 1.Adding B to An and 1 outcomes in B-A being preferably subtracted.

A way you can check number an as positive or negative without using a multiplexer on each piece is to use a XOR door to go before each piece.T he first commitment to the XOR door is the certified data bit. The second commitment to the XOR portal for each is the input D

Adders are a piece of the focal point of a normal unit for number of ALU operations. The control unit chooses which undertakings an ALU ought to perform (remembering the activity code being performed) and sets the action of ALU. One such control line from the control unit would be the D commitment to the adder subtractor above.

The adder subtractor above could without quite a bit of a stretch be contacted join more limits. For instance, on every Bi, a 2 to 1 multiplexer that would switch among zero and Bi could be spoken to, this could be used(related to D=1)to yield the An enhancement of the two since – A=A+1.

An another development is to change the 2 to 1 multiplexer on A to a 4 to 1 with the third data being zero, in this way multiplying it on Bi with the going with output possibilities.

A=0, B=0,D=0	Output=0
A=0, B=0,D=1	Output=1
B=0,D=0	Output=A
A=0,D=0	Output=B
B=0,D=1	Output=A+1
A=0,D=1	Output=B+1
D=0	Output=B+A
D=1	Output=A-B Output=B-A
A=***A*** **BAR**, B=0,D=0	Output= ***A*** **BAR**
A=***A*** **BAR**, B=0,D=1	Output= ***-A***
B=***B*** **BAR**, A=0,D=0	Output= ***B*** **BAR**
B=***B*** **BAR**, A=0,D=1	Output= ***-B***

6. SIMULATION RESULTS:

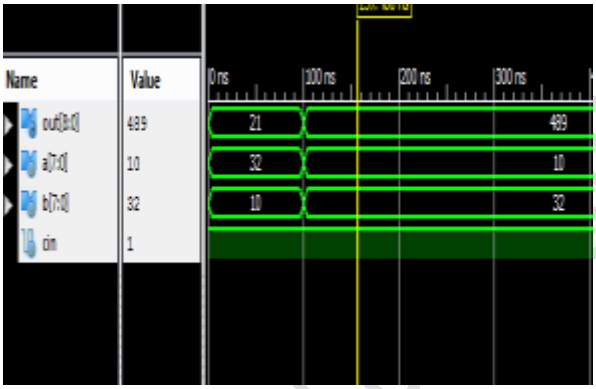

Fig. 12. N-bit Subtractor simulation waveform

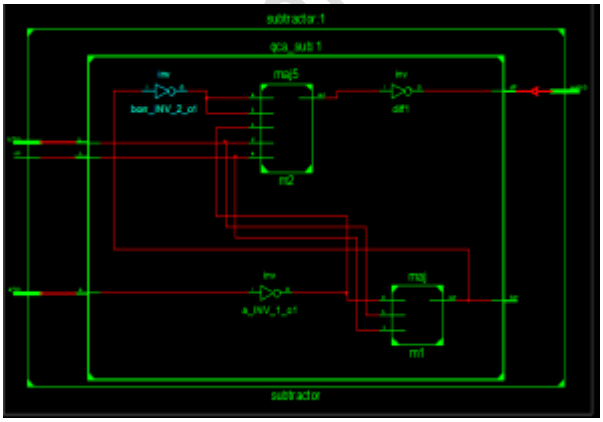

Fig. 13. Subtractor RTL Schematic

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	12	303600	0%
Number of fully used LUT-FF pairs	0	12	0%
Number of bonded IOBs	25	700	3%

Fig. 14. N-bit Subtractor design summary

```
Data Path: a<1> to out<8>
                                   Gate     Net
  Cell:in->out      fanout         Delay    Delay  Logical Name (Net Name)
  ----------------------------------------  ------------
   IBUF:I->O             2         0.000    0.608  a_1_IBUF (a_1_IBUF)
   LUT5:I0->O            3         0.043    0.417  s2/m1/out1 (borr1)
   LUT5:I3->O            3         0.043    0.417  s4/m1/out1 (borr3)
   LUT5:I3->O            3         0.043    0.417  s6/m1/out1 (borr5)
   LUT5:I3->O            1         0.043    0.339  s8/m1/out1 (out_8_OBUF)
   OBUF:I->O                       0.000            out_8_OBUF (out<8>)
  ----------------------------------------
  Total                            2.371ns (0.172ns logic, 2.199ns route)
                                           (7.3% logic, 92.7% route)
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Fig. 15. N-bit Subtractor Path delays

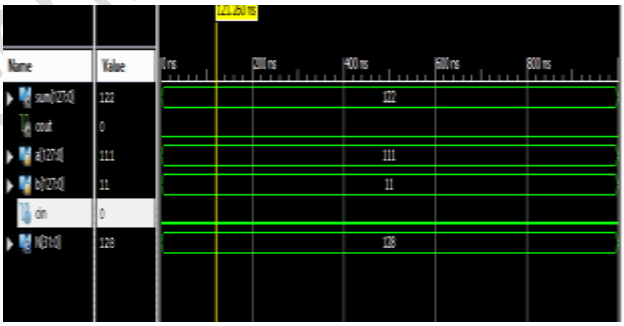

Fig. 16. N-bit adder simulation waveform

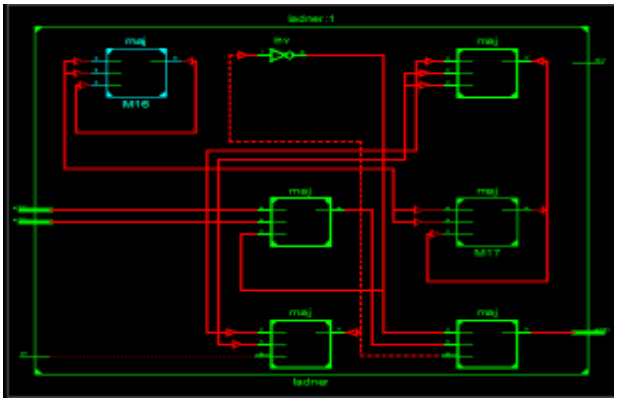

Fig. 17. adder RTL Schematic

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Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	13	303600	0%
Number of fully used LUT-FF pairs	0	13	0%
Number of bonded IOBs	26	700	3%

Fig. 18. Kogge-Stone adder design summary

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	3	0.000	0.507	b_0_IBUF (b_0_IBUF)
LUT3:I0->O	2	0.043	0.410	M31/m11 (M31/m1)
LUT5:I3->O	3	0.043	0.417	M35/m31 (M35/m3)
LUT3:I1->O	2	0.043	0.410	M6/m1 (c<4>)
LUT5:I3->O	3	0.043	0.615	M18/m21 (M18/m2)
LUT5:I0->O	1	0.043	0.339	M43/m1 (s_7_OBUF)
OBUF:I->O		0.000		s_7_OBUF (s<7>)
Total		2.914ns	(0.215ns logic, 2.699ns route) (7.4% logic, 92.6% route)	

Fig. 19. Kogge-Stone Path delays

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	13	303600	0%
Number of fully used LUT-FF pairs	0	13	0%
Number of bonded IOBs	26	700	3%

Fig. 20. Ladner Fischer adder Design summary

Cell:in->out	fanout	Delay	Delay	Logical Name (Net Name)
IBUF:I->O	3	0.000	0.507	b_0_IBUF (b_0_IBUF)
LUT3:I0->O	2	0.043	0.410	M31/m11 (M31/m1)
LUT5:I3->O	3	0.043	0.417	M35/m31 (M35/m3)
LUT3:I1->O	2	0.043	0.410	M6/m1 (c<4>)
LUT5:I3->O	3	0.043	0.507	M18/m21 (M18/m2)
LUT3:I0->O	1	0.043	0.339	M41/m1 (s_6_OBUF)
OBUF:I->O		0.000		s_6_OBUF (s<6>)
Total		2.806ns	(0.215ns logic, 2.591ns route) (7.7% logic, 92.3% route)	

Fig. 21. Ladner Fischer adder Path delays

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	17	303600	0%
Number of fully used LUT-FF pairs	0	17	0%
Number of bonded IOBs	26	700	3%

Fig. 22. Brent-Kung adder Design summary

Cell:in->out	fanout	Gate Delay	Net Delay	Logical Name (Net Name)
IBUF:I->O	3	0.000	0.615	a_1_IBUF (a_1_IBUF)
LUT5:I0->O	3	0.043	0.417	M33/m21 (M33/m2)
LUT5:I3->O	2	0.043	0.500	M8/m1 (c<4>)
LUT5:I2->O	4	0.043	0.630	M43/m_SW0 (M28/m4)
LUT6:I0->O	1	0.043	0.339	M39/m (s_5_OBUF)
OBUF:I->O		0.000		s_5_OBUF (s<5>)
Total		2.674ns	(0.172ns logic, 2.502ns route) (6.4% logic, 93.6% route)	

Fig. 23. Brent-Kung adder Path delays

CONCLUSION

In this paper, we have acknowledged diverse fast adders like Brent Kung, Kogge stone, Ladner Fischer of 8 bitIt is updated with the rationale of the QCA majority door only. If area is less and delay is not limiting ling adder is reasonable,,it is only appropriate when area is imperative. Brent kung adder has a great area delay product(ADP) and power delay product of all areas. We saw that the kogge stone has more area of less delay Majority entryway is more Area, Power, and Delay proficient.

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