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A Novel Hybrid Fuzzy Logic Controller based RFLC for fault limiting in Transmission Networks and it's Dynamic Analysis

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***Abstract*— The Fuzzy logic based resonant fault current limiter (RFCL) introduction in transmission network is analyzed. The fuzzy logic controller has fast response and error controlled closer to zero. The ability of fuzzy can enhances the system stability. It was concluded that RFCLs are effective devices for reducing the currents due to faults in bulk power systems. The fuzzy logic controller based RFCL used transmission network have enhanced transient stability and dynamic stability compared with conventional PI controller based RFCL network. The proposed system with fuzzy is tested and analyzed based on the MATLAB/Simulated software environment.**

***Keywords*— Fuzzy Logic Controllers, Transmission networks, fault analysis, network reduction, RFLC, stability.**

1. INTRODUCTION

Demand on electricity has been increasing tremendously and many countries invest significant amount of money for reliable power supply. More generation plants and transmission lines were constructed and the power systems became more complex. Major transmission lines tend to be long-distance and generation sites are large-scaled. Load concentration requires more transmission lines to be interconnected. However, those characteristics of power systems have been causing problems related to fault currents and system stabilities. Several approaches to cope with the fault current problems are being used in distribution and transmission areas.

Fault current and stability analysis has been studied separately, since network configuration influences in an opposite way to those problems. When transmission systems are fully meshed, they tend to yield fault current problems, rather than stability problems. On the other hand, when powers are delivered through high impedance transmission lines, stability issues may arise instead of fault current problems. However, as the power systems become more complex with the meshed transmission networks which are interconnected with long-distance, high-power transfer transmission lines, those two problems become co-existent. Consequently, countermeasures to deal with the fault current impact more on the power system stability than before.

The importance of using sustainable sources of energy will have a critical impact on future power systems, and is already leading to an increased presence of distributed generation (DG), microgrids, DC systems, and power electronic devices. These developments add further diversity to electrical sources and loads, and thereby complicate the system protection and control. For future power systems to cater for these fundamental changes, in many cases fault current levels will increase. For example, resiliency against blackouts is of importance in both grid and isolated networks. This, amongst other factors, may necessitate increased electrical network inter- connection, which normally increases fault current levels. The connection of DG can also significantly increase fault levels and disrupt protection coordination. Furthermore, the fault current levels in power-dense marine vessel and aircraft power systems are inherently high Safe network operation is very challenging in systems with a high fault level. Power system faults can cause significant damage to life and to equipment at the point of fault and to any equipment carrying fault current. Circuit breakers must be rated to clear faults for a particular system fault current level; higher fault currents lead to higher circuit breaker costs. A key solution to these issues is the adoption of fault current limitation in electrical systems. Fault current limiter (FCL) devices typically do not affect power system operation during normal conditions, yet rapidly act to mitigate the destructive and other undesirable effects caused by power system faults.

2. DESIGN AND WORKING OF RFLC

Fig.1 outlines the structure of a RFCL in one of the three stages. The arrangement thunderous circuit comprises of a current-limiting reactor and a full capacitor which are tuned to the required frequency of the power network to limit the impact of the RFCL under typical activity. It isn't for all intents and purposes conceivable to impeccably tune a resounding circuit and, along these lines, little stage move is unavoidable.

The figure shows that a thyristor-controlled bypass circuit, a metal– oxide varistor, and a bypass switch are in parallel to the capacitor. When a short out blame is distinguished, the thyristor valves are activated and the current commutates from the capacitor to the bypass circuit. In this way, the impedance of the RFCL changes quickly from very nearly zero (under typical activity) to the impedance of reactor, which keeps the advancement of huge blame current. The blame is recognized by contrasting a proportion of the line current, where the RFCL is situated, with a predefined edge esteem. On the other hand, a mix of the present greatness and its rate of progress and the span of their event can be utilized to recognize a blame. The bypass circuit depends on a string of direct light-activated thyristors in arrangement with a release current-limiting reactor and a damping resistor, see Fig. 3.1; these thyristor valves have a high ability amid turn-on and the likelihood to work at maximum capacity with a less complex activating circuit, contrasted with customary thyristors. The structure of the bypass circuit expects to restrict the rate of progress of release current and its pinnacle an incentive in the wake of setting off the thyristor valves, and to diminish motions of the release current amid bypass task. The bypass circuit continues to conduct the current after fault detection.

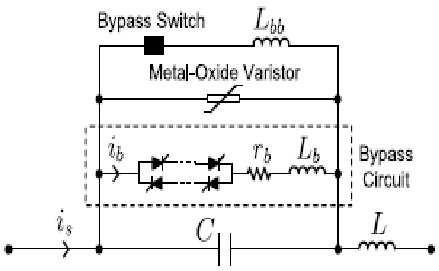

Fig-1. Design of a single phase RFLC.

When the fault is cleared by a successful tripping of the CB located near the fault location, the firing pulses of the thyristor valves are suppressed, and the capacitor is inserted into the circuit and, thus, the RFCL impedance reduces to zero. If the capacitor is required to remain bypassed for a longer period of time after the inception of the fault, then the bypass switch can be used to commutate the current from the bypass circuit. The inductor limits the rate of current commutation to the bypass switch. Also, the varistor should be properly rated to protect the capacitor

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against transient over voltages, whenever the capacitor is not bypassed. The IEEE nine-bus test power system, whose data are given, is illustrated in Fig. 3.2. Let us assume that breaker CB5 is properly rated for a three-phase-to-ground (3LG) solid fault at feeder F5 (labeled as FltA).

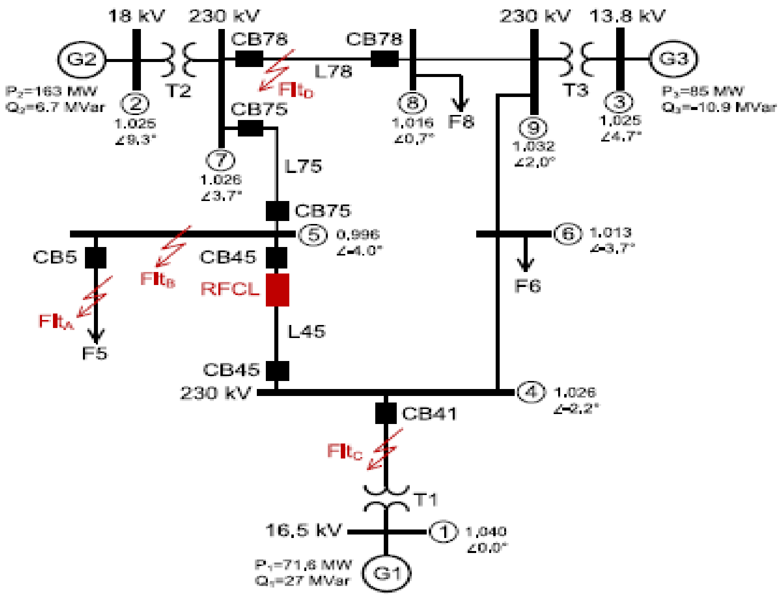

Fig. 2. Test power system with an RFCL inserted between bus 5 and 4.

Similarly, let us assume that breakers CB45 are rated for a 3LG solid fault at bus 5 (labeled as FltB). Now, if the interrupting capability of each aforementioned breaker is only marginally larger than the current that flows through the breaker due to a fault at feeder F5 (for CB5) or bus 5 (for CB45), then the addition of generation at bus 1, for example, in response to the installation of loads at bus 4, or in response to the growth of load at feeder F5, can prevent the breakers from interrupting the fault current. Therefore, the breakers must either be replaced or, alternatively, an RFCL can be connected in series with line L45, see Fig. 2, to limit the current through the line if faults and strike the system. This, in turn, results in a reduction in the current through breakers CB45 (for fault B), and, consequently, also breaker CB5 (for fault A), while the RFCL has a negligible impact under normal operation.

3. RFCL DESIGN

The process presented in this paper to design the elements of an RFCL and to assess its transient operation in a host power system is a combination of analytical analyses and iterative numerical simulations. Thus, an equivalent network of the overall power system, from where the RFCL is located, which accurately reproduces, during the time period of interest, the same instantaneous values of voltages and currents as those in the overall system can result in a more effective and less timely design process. The bypass circuits in the three phases of the RFCL in Fig.3.2 are triggered as soon as a fault is detected, which occurs within a quarter cycle after the fault strikes the system. Then, the current through line L45 is commutated from the resonant capacitors to the bypass circuits. Therefore, to capture the transient voltage and current stresses in the bypass circuits, in the equivalent network, it should reproduce a steady-state current through line L45, similar to that in the overall system, before the inception of the fault, and should also emulate the instantaneous line current for a quarter cycle after the strike of the fault.

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3.1. Current-Limiting Reactor

To reduce the current through line L45, for faults Flt_A and Flt_B, below its value in the case without RFCL, the value of the current-limiting reactor can be calculated, using the parameters of the equivalent network and based on the desired amount of reduction in the line current, by solving the following equation:

$$r_t^2 + (x_t + \omega_0 L)^2 = \left(\frac{|\overrightarrow{v_{re4}}|}{k|\overrightarrow{i_{sc}}|} \right)^2$$

3.2. Bypass Circuit Design

The thyristor valves in the bypass circuit are triggered when a fault is detected and, thus, the current starts to transfer from the resonant capacitor into the bypass circuit. The current through the bypass circuit includes a discharge current superimposed on the current due to the fault. Therefore, the elements of the bypass circuit should be designed to limit the rate of change of discharge current and its peak instantaneous value below their permitted maximum values, which, in turn, are determined based on the current withstanding ratings of the valves. The maximum rate of change of discharge current occurs when the bypass valves are triggered at the maximum possible instantaneous voltage across a resonant capacitor, which, in turn, is equal to the protection level voltage of the varistor. Moreover, reactor limits the initial rate of change of the discharge current when the valves are triggered.

3.3. Energy Absorption Capacity of Varistors

As previously mentioned, the resonant capacitors are not bypassed during the transient time periods subsequent to the strike of faults or and, thus, their parallel varistors are required to protect the capacitors against transient over voltages by absorbing the extra energy. Moreover, the varistors also protect the resonant capacitors during their insertion in the line, after they had been bypassed in response to the strike of fault. Thus, when fault is cleared by opening breaker CB5, it is desired to insert the capacitor in line L45, in order to compensate reactor and, therefore, to avoid reducing the maximum capacity of line L45 to transfer power. The amount of energy absorbed by a varistor during a transient time period can be calculated by integrating, over time, the product of the current through the varistor and the voltage across its terminals. This, in turn, can be achieved using the time-domain simulation of the system. In this paper, an ideal volt-ampere characteristic is assumed for the varistors and, therefore, the voltages across the capacitors are not allowed to exceed, while the extra current flows through the varistors.

4. FUZZY CONTROLLER SCHEME

The disadvantage of PI controller is its inability to react to abrupt changes in the error signal, ε, because it is only capable of determining the instantaneous value of the error signal without considering the change of the rise and fall of the error, which in mathematical terms is the derivative of the error denoted as Δε. To solve this problem Fuzzy logic control as it is shown in Fig.3 is proposed.

The determination of the output control signal, is done in an inference engine with a rule base having if-then rules in the form of

Table.I FLC rule base.

ε /Δε	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NM	NM	NS	ZE	PS
NS	NB	NM	NS	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PS	PM	PB
PM	NS	ZE	PS	PM	PM	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

"IF ε is .... AND Δε is ...., THEN output is ...."

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With the rule base, the value of the output is changed according to the value of the error signal ε, and the rate-of-error Δε. The structure and determination of the rule base is done using trial-and-error methods and is also done through experimentation. All the variables' fuzzy subsets for the inputs ε and Δε are defined as (NB, NM, NS, Z, PS, PM, PB). The fuzzy control rule is illustrated in the table I.

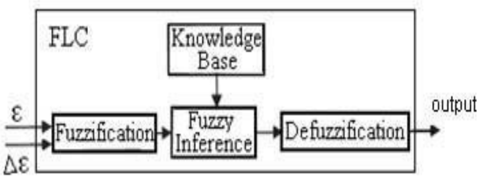
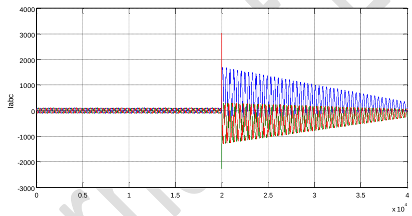


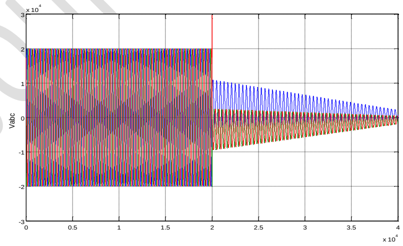
Fig.3. Basic representation of FLC

5. SIMULATION RESULT ANALYSIS

To compare the transient responses of the equivalent network with and without the RFCL in line L45, to the nine-bus test system, both networks are simulated in MATLAB/SIMULINK simulation results. In the nine-bus system, dynamic models of the generators, including their exciter and governor models, are utilized, whose parameters are given.



(a)



(b)

Fig. 4. Responses of the nine-bus system (left column) and its equivalent network (right column) to the strike of fault Flt_A with an RFCL in line L45.

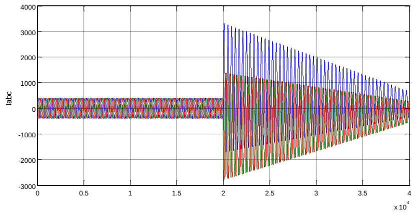
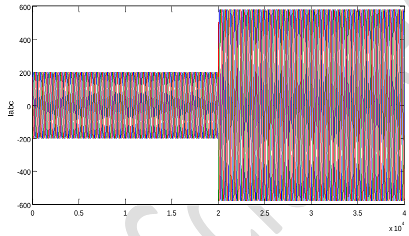
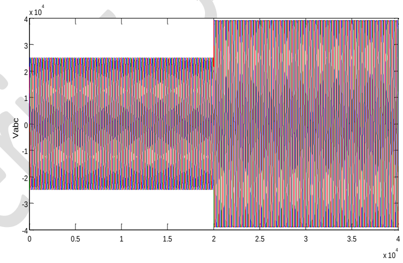


Fig. 5. Instantaneous currents through breaker CB5 in the nine-bus system (left column) and its equivalent network (right column) with the RFCL in line L45.

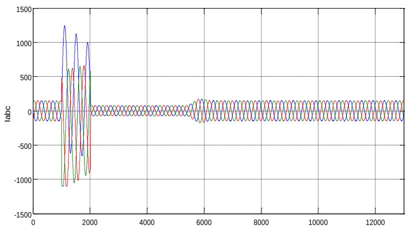


(a)

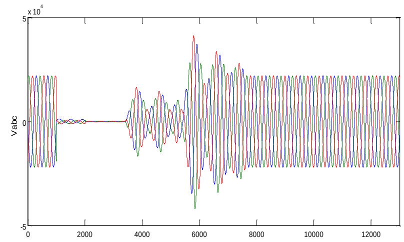


(b)

Fig. 6. Responses of the nine-bus system (left column) and its equivalent network (right column) to a 3LG fault at and bus 7, respectively Flt_D (a) Line currents. (b) Capacitor voltages.



(a)



(b)

Fig.7. Responses of the nine-bus system subsequent to the strike of fault Flt_A.(a) Line currents. (b) Capacitor voltages.

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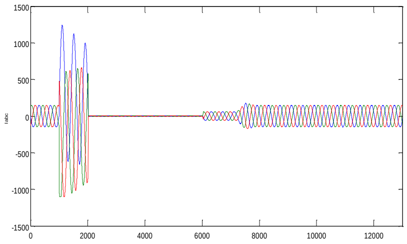
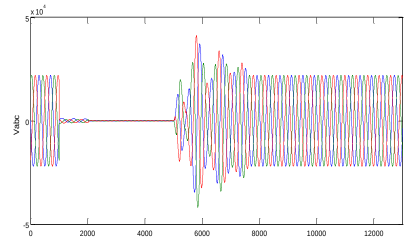


(a)



(b)

Fig.8. Responses of the nine-bus system subsequent to the strike of fault Flt_b.(a) Line currents. (b) Capacitor voltages.

It is observed that subsequent to the fault initially, the voltages across the capacitors increase due to the rise in the line current. Then, after the bypass valves are triggered, the line current commutates to the bypass circuit and the voltages across the capacitors drop. Fig. 2 plot the responses of the nine-bus test system in the two cases of without RFCL and with an RFCL in line L45, where at 0 s, fault strikes the system in each case.

In the case of the RFCL, the protection-level voltage of the varistors is selected equal to two times the capacitor voltage under normal operation, that is, 43 kV, and the current threshold is equal to four times the current through line L45 under normal operation, that is, 800 A. It is observed that the responses of the nine-bus system and its equivalent network, in the two cases, are in close agreement during the prefault and a quarter cycles after the inception of the fault.

Fig.8 also plot the instantaneous currents through breaker CB5 in the nine-bus system in the two cases of without RFCL and with the RFCL in line L45. It is observed that the peak value of the current is reduced from 5 kA to 3.5 kA, that is, 30% reduction. Fig.8 illustrates the responses of the nine-bus system when the resonant capacitors are inserted in line L45 after the clearance of fault, under the assumption that the system is at steady state before 0 s. Thus, Fig.8 depicts that the responses of the nine-bus system and its equivalent network are generally in agreement despite the discrepancies. Since the capacitor voltages remain below, no energy is absorbed by the varistors.

6. CONCLUSION

This paper describes about a comprehensive framework to design of Fuzzy logic based RFCLs in transmission network. The proposed system with fuzzy is tested and analyzed based on the simulated results. The transient response of the proposed system is analyzed. It was concluded that RFCLs are effective devices for reducing the currents due to faults in bulk power systems. The fuzzy logic controller based RFCL used transmission network have enhanced transient stability and dynamic stability compared with conventional PI controller based RFCL network.

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