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10-bit Segmented (7B(Binary)-3U(Unary)) Current Steering DAC for Improving SFDR

[1st]Ashok Kumar Adepu
Research Scholar, Dept. of ECE
JNTU Kakinada
Kakinada, Andhra Pradesh, India
adepuashokkumar@gmail.com

[2nd]Dr. N. Balaji
Professor of ECE
JNTU Kakinada
Kakinada, Andhra Pradesh, India
narayanamb@rediffmail.com

Abstract -

Current steering digital to analog converters (DACs) have wide range of applications in communication system and video systems. Even binary weighted architecture of DAC is suitable for medium resolution and speed, the performance of digital to analog converter can be improved by using segmentation architecture. The dynamic behaviour of the DAC is enhanced by segmented architecture. The method was proved successfully by a 10-bit 400 MHz segmented current steering DAC with a power consumption of 41 mW and operated at power supply of 3.3V. The proposed architecture achieved an SFDR of 63 dB. The 10bit segmented architecture has INL and DNL of less than 0.1 LSB.

Keywords – Segmented, Binary weighted, Current switch, Digital to analog converter (DAC), Binary to thermometer decoder, Spurious frequency dynamic range (SFDR).

I. INTRODUCTION

Digital to analog conversion technique is mostly preferred technique in order to reduce the noise of a signal which is to be transmitted. As all practical world signals are analog in nature, if the analog signal is transmitted into channel directly without converting it into digital, and if error is occurred in the channel then the removal of noise associated with the transmitted analog signal is very difficult as analog signal is having infinite number of voltage levels.

As a result, if transmission of analog signal is made after converting infinite voltage levels into finite voltage levels, the removal of noise becomes easy. The device which converts infinite voltage levels into finite voltage levels is analog to digital converter (ADC). Analog to digital converter which consists of number of stages to convert into digital form from Analog signal. At the receiver side this digital signal is converted back into analog signal using DAC.

All practical world analog signals such as voice, temperature are generally changed into digital form, which can be accessed very easily in present digitized systems. In almost all modern machines, the digitized data should be converted back into the analog data in order to make some real world applications. The device which does this work is digital to Analog converter. Complex fewer components such as switches resistor elements and current sources can perform this conversion and the outputs of those can be used to drive devices such as mechanical servos, loudspeakers, temperature, radio frequency, video displays etc. Figure 1 shows the block diagram of a digital to analog converter.

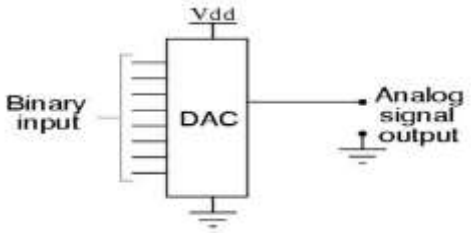

Figure 1. Block Diagram of DAC

II. DAC ARCHITECTURES

Digital to analog converter which is an essential part in communication systems can be implemented in three different architectures namely unary, binary weighted [1] and segmented structures. In unary structure, a B-bit unary array consists of 2^B-1 identical unit elements, each have LSB-size. To represent a binary digital code, the unary array requires a digital decoder that maps the binary input data to an equivalent number of DAC elements. Because the unit elements are not distinguishable, this mapping function is not unique. This means that a specific input code can be represented by more than one set of DAC-elements. Only the full-scale values, i.e., all zeros or ones, have a unique representation, all other codes do have at least 2^B-1 different combinations of unit elements that generate nominally the same output value.

Dynamic element matching (DEM) techniques [5] try to average out the unit element mismatch over time and make extensive use of this property of unary arrays. The drawback of unary arrays is that the complexity of the digital decoder is exponentially related to the resolution. In practical implementations the resolution of a unary array is therefore limited to typically 4–8 bits.

On the other hand, unary arrays offer the best possible performance. Because of their strictly incremental nature, monotonicity is always guaranteed.

The differential nonlinearity (DNL) of unary arrays is unequalled, because for every code transition it depends only on the accuracy of one single DAC-element of LSB-size. The same is true for a limited class of dynamic effects. When switching from one code to the next, certain transitional errors are linearly related to the code step. If the DAC-elements and the associated switching errors are additionally well matched, then, supposedly, only linear errors can occur in the output signal. That even perfectly matched unary current-steering arrays are subject to certain switching imperfections that cause nonlinear distortion.

In binary weighted architecture decoder is not used. The number of current sources used here are equal to the number of input binary bits. Here the weight of each current source is different and it depends on the position of the bit. For an n-bit input n number of current sources is used with n different weights.

Segmented architecture combines both unary and binary structures in order to improve the dynamic performance of digital to analog converter. As unary architecture includes binary to thermometer decoder over all complexity of the segmented DAC architecture increases.

III. BINARY TO THERMOMETER CODE DECODER

A general decoder is an electronic circuit which is used to select only single output line among various output lines depending on the input binary code. But, binary to thermometer code is a type of code which is used in the design of unary architecture, which is a part of segmented DAC architecture. For an n number of binary inputs the thermometer decoder produces 2^n-1 output. In binary to thermometer decoder the next output is selected along with the present outputs. When binary input 010 is given at the input of binary to thermometer code first two outputs made high such that the combined current source and switches which are connected to these lines get activated.

Different segmented DAC architectures can be designed such as 8-2, 7-3, and 6-4. In 8-2 segmented DAC least two bits are implemented using unary and remaining 8 bits are implemented using binary weighted [9]. In 7-3 segmented DAC least 3 bits are implemented using unary structure and remaining 7 bits are implemented using binary architecture. Similarly in 6-4 segmented architecture 4 bits are implemented with unary structure and bits are implemented with binary weighted structure. Unary architecture utilizes a binary to thermometer code decoder in order to get output. While implementing 8B-2U segmented architecture, 2-3 thermometer code decoders is used. Similarly during the design structures of 7B-3U and 8B-2U, architectures involve the use of 3-7 and 4-15 thermometer code decoders respectively.

As in VLSI design utilizing the existed one is better than implementing a new design, first a 2-3 thermometer code decoder is implemented and then it is used in the design of 3-7 thermometer code decoder, similarly 3-7 structure is utilized during the implementation of 4-15 thermometer decoder. Figure 2 shows the schematic of 3-7 binary to thermometer decoder used in unary structure of a proposed segmented DAC architecture.

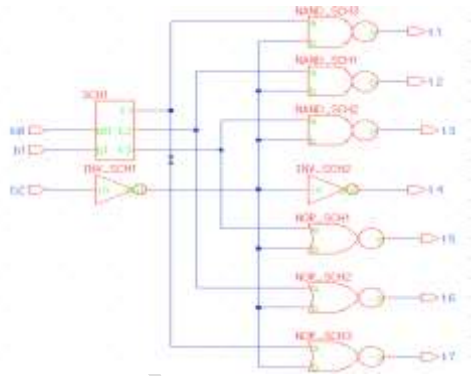

Figure 2. Schematic of 3-7 Thermometer Decoder

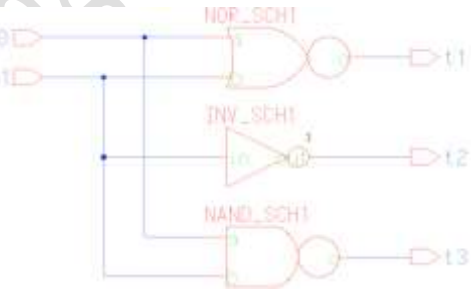

Figure 3. Schematic of 2-3 Decoder

As 3-7 thermometer code decoder structure is implemented using 2-3 decoder, the schematic of 2-3 thermometer code decoders is shown in figure 3.

IV. OVERALL ARCHITECTURE

In present days DACs need to be operated for high frequency applications [11]. Segmentation provides good performance of frequency domain applications than binary weighted structures. As we are intended to design 7B-3U segmented architecture we have to use unary architecture for least 3 bits and binary architecture for remaining 7 bits. As unary architecture needs a binary to thermometer decoder we need to obtain a 3 bit thermometer code from available basic gates. As the size of the thermometer decoder is 2^n-1, we will encounter with 7 outputs as the value of n is 3 in this case. These 7 outputs are connected to the seven combined current source and switches with same amount of weight.

Full scale range of binary input signal is provided from 10 bit asynchronous clock the least 3 bits are connected to the 3 inputs of binary to thermometer decoder and remaining 7 outputs from counter are directly given to binary weighted network which consisting of

combined current source and switches whose weight differs according to the position of the CSCW. The segmented architecture involves the combination of both remaining. Figure 4 shows the schematic of 7-3 segmented 10-bit DAC architecture without any compensation technique, in which 7 bits are implemented using binary and 3 bits are implemented using unary architectures.

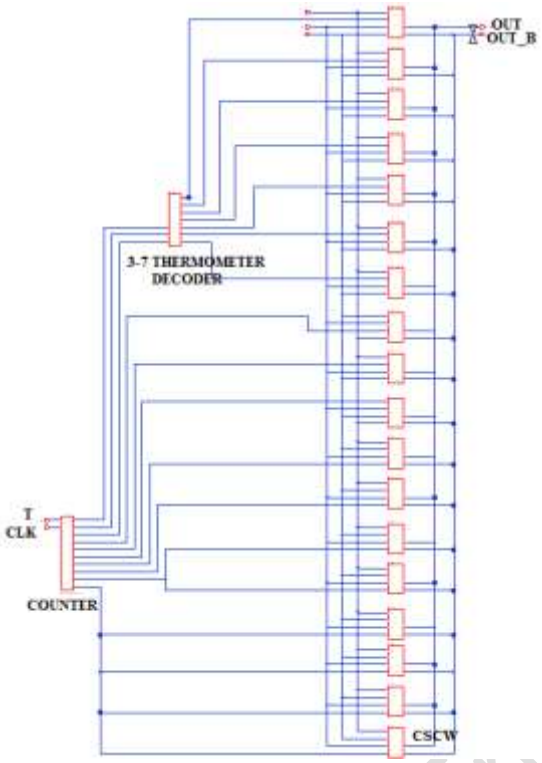

Figure 4. Schematic Diagram of Proposed Segmented DAC

The schematic of combined current source and switch is shown in figure 5. The CSCW cell joins the current source and current switch in order to minimize the parasitic capacitance. In order to produce higher weights of these CSCW cells these are connected in cascading nature. Output impedance of a current switch is the major parameter which decides integral non linearity error (INL) and spurious free dynamic range (SFDR) given in below equations (1) and (2).

$$INL\ (LSB) = \frac{R_L 2^{2N}}{4Z_0} \quad (1)$$

$$SFDR = 20\ \log\frac{2^N}{INL} \quad (2)$$

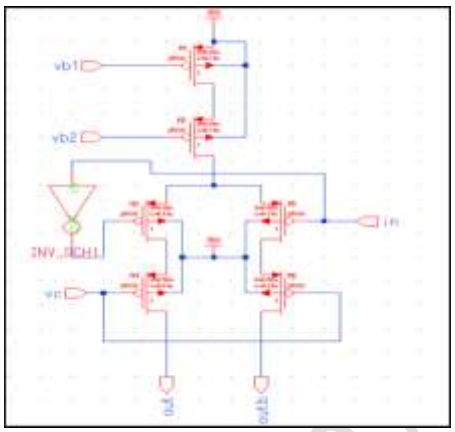

Figure 5. Schematic of CSCW Cell

V. SIMULATION RESULTS

As the proposed DAC is running at 400 MHz sampling rate, the time period of 1 clock signal is 2.5 ns. So that entire analog output can be obtained by 2600 ns. The clock corresponding to the 10-bit digital input from 0000000000 to 1111111111 is shown in below figure 6.

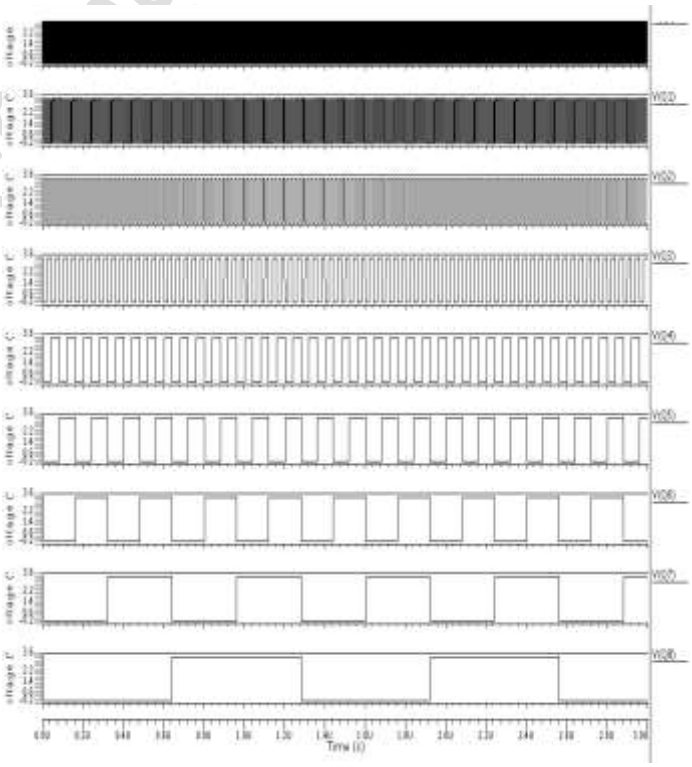

Figure 6. Results of 10-Bit Counter

Pre layout simulation results for 7-3 segmented DAC are shown in figure 7.

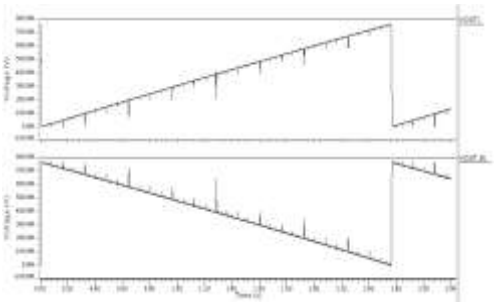

Figure 7. Analog Output of a Proposed DAC for 400 MHz

Table1 shows various parameter comparison of proposed DAC with other papers.

From table 1 it is seen that all different segmented DAC architectures are having better result performance than binary weighted DAC architecture. The segmented DAC architecture ran at a sampling rate of 400MS/s. The power dissipations of segmented DAC architectures are all more than binary weighted architecture because the binary weighted architectures are running at a power supply of 1.8V and all segmented architectures are operating at a power supply of 3.3V. Even though the complexity of segmented architecture is increased over binary the dynamic behaviour is greatly enhanced.

TABLE 1. COMPARISON OF VARIOUS SEGMENTED DAC'S WITH BINARY WEIGHTED ARCHITECTURE

	8-2 segmented DAC	7-3 segmented DAC	6-4 segmented DAC	Binary weighted DAC
Technology(µm)	0.13	0.13	0.13	0.18
Resolution	10	10	10	10
Sample rate (MS/s)	400	400	400	250
Best SFDR (DB)	61	63	62	60
Supply voltage (V)	3.3	3.3	3.3	1.8
Power consumption (mW)	30.7	31	31.3	27.3

Now discussing the parameter performance among various segmented DAC architectures, the segmented architecture 7 binary-3 unary is giving good result. Even though all the segmented architectures are operating at same operating frequency, 7B-3U segmented structure is providing best SFDR [8,10] of 63db. The segmented structure 7B-3U is offering lower complexity than 6B-4U segmented because 7B-3U is using 3-bit thermometer decoder.

VI. CONCLUSION

In this paper, architecture of 10-bit segmented (7B-3U) current steering DAC is proposed, as a result dynamic behaviour of DAC is improved. This architecture enhances the performance over binary weighted architecture by improving the linearity. The proposed design was implemented using 130 nm technology. The design was operated at sampling frequency of 400 MHz for a power supply of 3.3V. The SFDR of this structure is 63 dB with a power dissipation of 41mW. The 10bit segmented architecture has INL and DNL of less than 0.1 LSB.

VII. REFERENCES

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