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DESIGN OF VEDIC MATHEMATICS BASED ALU USING APPLICATION SPECIFIC REVERSIBILITY

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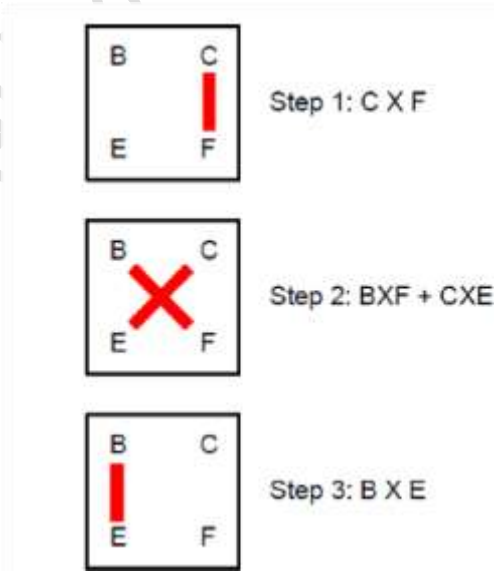
ABSTRACT:The proposed project utilizes the computational speed advantages of Vedic algorithm and energy optimization benefits of Reversible circuit. The Vedic algorithm optimizes the conventional mathematic computation logic used in the current processors thereby, effectively increasing the speed of computation. The Urdhva Triyambakam method derived from the ancient Indian mathematics will be used in the proposed project. Reversible circuits, on the other hand, reduces the power dissipation incurred due information/bits loss as in the case of an irreversible circuit making way for better power utilization along with reduced heat dissipation. The proposed project introduces the concept of application specific reversibility wherein the logical states belonging only to a particular function of the module is being considered, which significantly impacts in reducing the area limitations of a reversible unit while keeping its power efficiency benefits. The circuit design presented utilizes the above technique mentioned while designing the adder, multiplier along with other modules of an ALU.

1. INTRODUCTION

The Primary objective of a digital circuit design is to optimize for speed, area, power and energy. While it's a challenge for circuit designers, to achieve this optimization without compensating for one or the other parameters mentioned above. Certain design techniques, algorithms and smarter planning of the available resources have proven to be successful to achieve the level of optimization required for much higher efficiency. Arithmetic Logic Unit (ALU) being the driving component of a processor, optimizing its module for speed and power becomes quite inevitable. Many previously published technical papers have emphasized the use of reversibility in circuits design for reduction in power dissipation, while successfully demonstrating the same. However, this reduction in power was also followed by significant reduction in speed as well as increase in chip area. Hence smarter algorithm and logic design was required to speed up the execution of a logic module. With this reference, 'Vedic Algorithm' technique was utilized to pave way for faster execution of an arithmetic module of an ALU. While there are as many as 16 techniques(sutras) in the Vedic algorithm, the proposed design will implement multiplier using the popular Urdhva method (Urdhva Triyambakam along with certain improvisation while explained in the subsequent parts of the paper. The conventional way of implementing the multiplier would have involved series of AND gates and adders to get the required output while incurring significant delay. The Vedic algorithm provides a faster way to get through the output with less number of logical elements involved, thereby reducing the delay while effectively increasing the speed of processing the output. A simple illustration of Vedic technique is explained in the figure.



2. REVERSIBILITY:

The strengths of Reversibility in digital circuits is well documented and explained by R. Launder in his article.A circuit which can undo or reverse its output to get back its original input will not suffer information loss, since all the information are present within the circuit and only need to be reversed, to be recovered. Hence a reversible circuit will save major chunk of power dissipation suffered due to information loss that happens every clock cycle.

The basic requirement of a reversible circuit is to have a one-to-one correspondence between inputs and outputs, which requires the input and output pin count to be same. Also each input state must correspond to a particular unique state of the output i.e. output states cannot be shared by more than one input states available. If the above

criteria are satisfied the inverse circuit can be easily designed to make the circuit reversible.

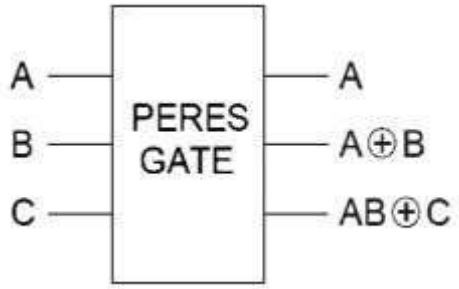
2.1 Reversible Gates

The reversible gates used in this paper are as follows.

A. Peres Gate

Peres gate is a 3x3 reversible gate. The quantum cost of this gate is 4. It is mainly used for half adder application. It has lesser area and quantum cost compared to other reversible gates like Fredkin and Feynman gate. It has three inputs A, B and C. The outputs are given as P=A, Q=A xor B and R= (A.B) xor

C. To use it as an half adder C is given logical zero. The outputs of the gate become P=A, Q=A xor B and R=A.B.



I. FIG 2: PERES GATE

A. HNG Gate

HNG gate is a 4x4 reversible gate. It is mainly used for full adder application. The quantum cost of this gate is

6. It has four inputs A, B, C and D. The outputs are given as P=A, Q=B, R=A xor B xor C and S= (A xor B).C xor (AB xor D). To use it as a full adder D is assigned to logical zero and C is assigned the input carry bit. The outputs of the gate become P=A, Q=B, R= A B C and S= (A xor B).C xor AB.

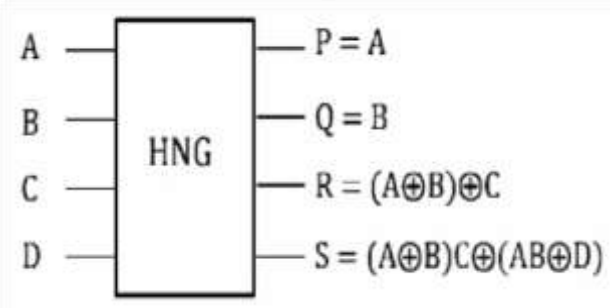


Fig 3: HNG Gate

B. BJN Gate

It is a 3x3 reversible gate. The quantum cost of this gate is 5. For the three inputs A, B and C the outputs are P=A, Q=A and R= (A+B) xor C. In this paper it is used in the logical unit. This gate is used to realize OR and NOR gates. When C=O, R= (A+B) and for C=l, R= (A+B).

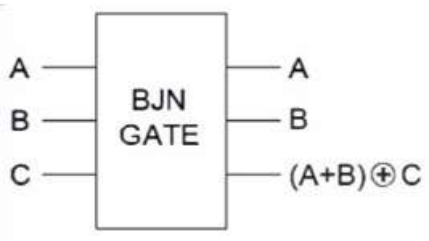


FIG 4: BJN GATE

C. TSG Gate

It is a 4x4 reversible gate. This gate can realize most of the Boolean logical operations like AND, NAND, XOR, XNOR and NOT. The outputs of this gate are P=A, Q=A'C' xor B', R= (A'C' xor B') xor D and S= (A'C' xor B') D xor (AB xor C). Inputs C and D are used as control signals to select the logical operation

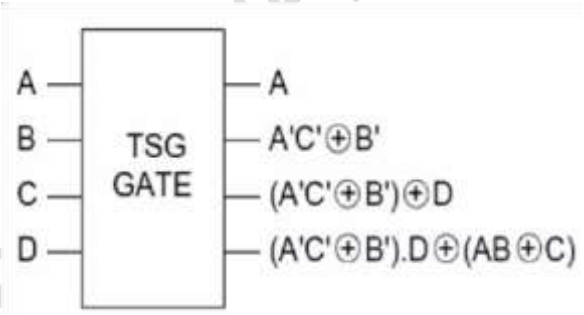


FIG 5: TSG GATE

2.2. Arithmetic Unit- Full Adder/Subtractor

This adder is a 4-bit ripple carry adder. It is made using four HNG gates. HNG gates have the minimum delay, area and quantum cost for full adder application. The two inputs and carry bit is given to the first, second and third input respectively of the HNG gate. The fourth input pin of this HNG gate is grounded so it acts as a full adder. The output bits of the HNG will be P=A, Q=B, R= (A xor B) xor C, S= (A xor B).C xor AB. R is the sum of the addition and S is the carry. A control signal S is used to switch between adder and subtractor mode. When S=0, the circuit acts as a 4-bit full adder. When S=1, input b is complemented and an input high carry bit is given to the LSB full adder. In subtractor, R is the difference and S is the borrow bit. If the result of

the 4-bit subtraction is negative then the borrow will be zero and output is stored as 2's complement

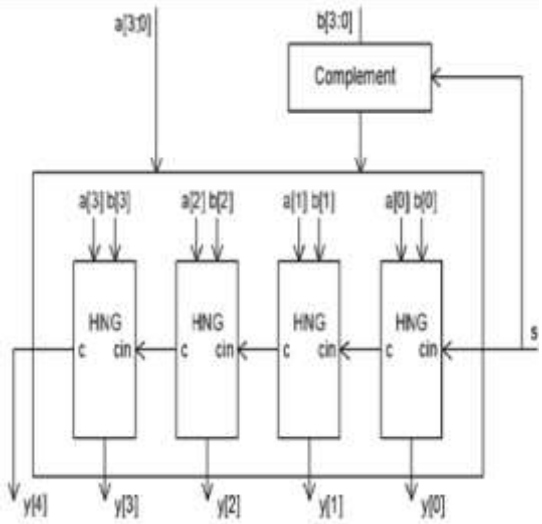


FIG 6: REVERSIBLE FULL ADDER/SUBTRACTOR

D. Proposed KSA Gate:

It is a 4x7 semi-reversible logic gate designed especially for 2-bit multiplication application. Out of the seven outputs, the first four outputs give the product of the two 2-bit inputs assigned to the four input pins. Three more output pins are added to make one-to-one mapping between inputs and outputs. Since this gate has 7 output bits it is expected to have one-to one mapping between all the 128 cases. The proposed semi-reversible gate has one-to-one mapping between the inputs and outputs for the possible 16 cases of output product. Using a general purpose reversible gate for a specific application has more number of redundant gates and garbage outputs

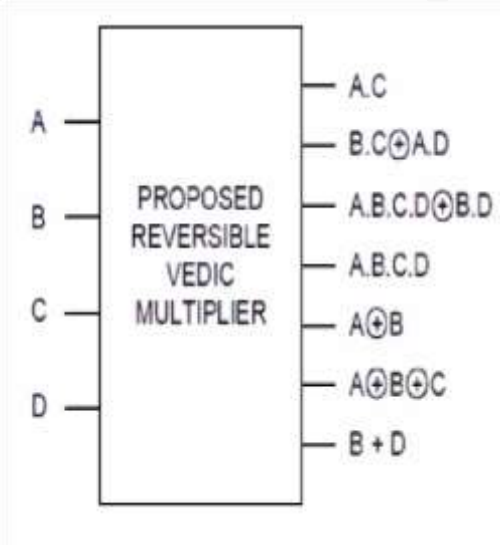


FIG 7: TSG GATE PROPOSED KSA GATE

2.3. *Logical Unit*

The proposed 4-bit logic unit performs the logic operations on two 4-bit numbers. The 8 basic logic operations performed by proposed logic unit are AND, NOR, XNOR, XOR, NOT (invert), NAND, A'B, OR,

NOR etc. A BJN gate is used to implement OR and NOR operations.

A control input C controls the operation of a BJN gate. When C=O, BJN gate performs OR operation of two inputs A and B. When C=l, it gives NOR operation of A and B. TSG gate is used to implement the rest of the logical operations. Input C and D acts as control signals to TSG gate. When c=o and D=O, it results in AND operation of A and B. When c=o and D=l, it gives XOR and XNOR operations of A and B. When C=1and d=0, the resulting output is inversion of B and NAND operation of A and B. When C=1and d=1, it results in A'B. Thus, overall logic unit uses only two types of reversible gates to implement 8 logic operations

2.4. *ALU Design*

The proposed ALU design has a four bit control signal.

- It performs six arithmetic operations and seven logical operations.
- The proposed ALU uses both reversible and semi reversible gates in it.

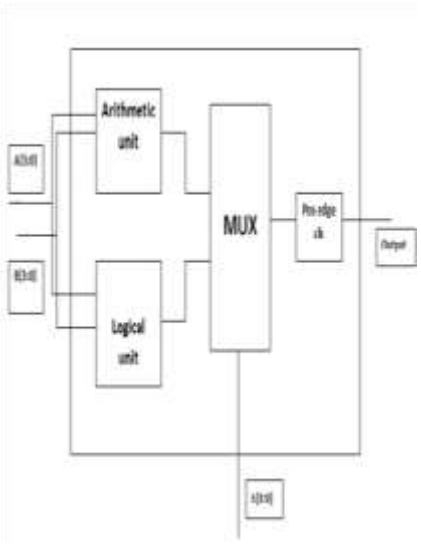


FIG 8: PROPOSED ARCHITECTURE OF ALU

The operations performed based on the control bits are as follows. Total of sixteen operations are performed by the proposed ALU

Table 1. Operations performed based on the control signal

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Control Signal	Operation
0000	Addition
0001	Subtraction
0010	Multiplication
0011	Increment
0100	Decrement
0101	A.B
0110	A⊙B
0111	$\overline{A \odot B}$
1000	$\overline{B}$
1001	$\overline{A.B}$
1010	$\overline{A}.B$
1011	A+B
1100	$\overline{A+B}$

3. SIMULATION RESULTS

Below figures represents the simulation and synthesis results indicating some of the operations performed using reversible gates in ALU.

Fig 9: addition of two binary numbers

Fig 10 :Increment of two binary numbers

Fig 11: XOR of two binary numbers

4. SYNTHESIS RESULTS

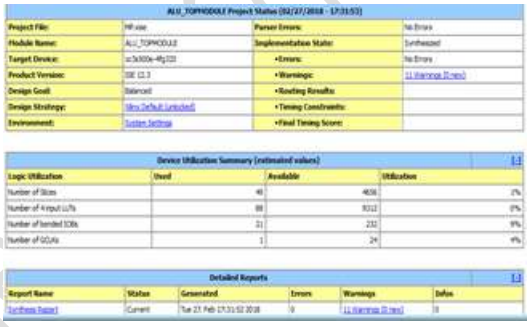

Fig 12: Area of Reversible ALU

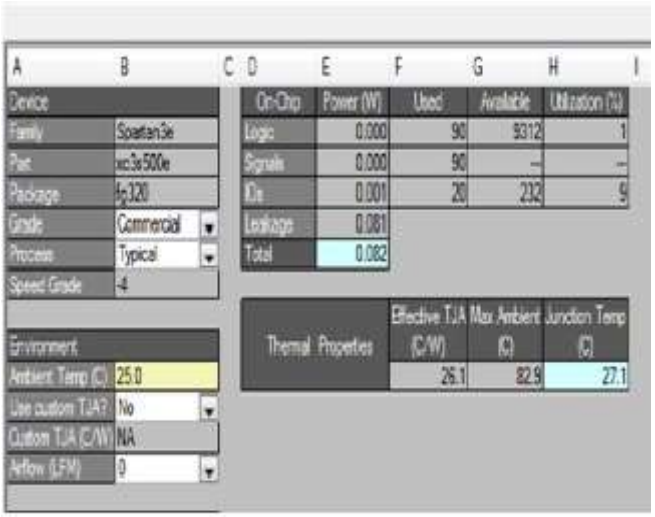

FIG 13: POWER OF REVERSIBLE ALU

The above figure represents the power consumed by the ALU block using application specific reversibility

5.COMPARISION

Table showing the comparison of various parameters between a normal 4 bit ALU with a 4 bit Reversible ALU block

Parameter	Normal 4-bit ALU	Reversible 4-bit ALU
LUTs used(area)	102	88
Power dissipation(W)	0.088	0.082
Delay(ns)	15.264	16.642

6.CONCLUSION

The proposed ALU design has a four-bit control signal. It performs six arithmetic operations and ten logical operations. The proposed ALU uses both reversible and semi reversible gates in it. Arithmetic operations are addition, subtraction, multiplication, increment and decrement. Logical operations are and gate, or gate, not gate, nand gate, nor gate, xor gate, xnor gate, a'b,. The operations are performed based on four control bits using mux. Total of sixteen operations are performed by the proposed ALU. The Reversible ALU occupies less area and consumes less power compared to normal ALU. The proposed ALU is coded in Verilog followed by synthesization using XilinxISE12.3v.

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