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PHYSICAL DESIGN IMPLEMENTATION OF OPENMSP430 USING DIFFERENT APPROACHES

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Abstract – Due to rapid growth in the field of electronics and communication engineering, VLSI plays essential role which been acquired by the mechanization of distinct steps pertaining the design and forgery of the VLSI chips. In this paper we appraised openMSP430 module in which lower technologies such as 45nm, 180nm, 350nm and 500nm are investigated from RTL to GDSII. The core area of the design is been considered up to 0.7 with high accomplishment, with the concern of clock frequency 404.85 MHZ with a significant reduction of 3440736 μm^2 die area. Primarily the design is been optimized for 500nm net-list, later it has been carried over lower technologies (350nm, 180nm, 45nm) with the enhancement of PPA (performance, power and area) are improved as scheme towards lower strategies by open source tools such as proton, open STA and Q-flow.

Key Words: synthesis; floor-planning; placement; physical design, routing

1. INTRODUCTION

Despite of being, inaugurated by Intel for more than 3-decades across 1980s. The openMSP430 is one of the most prominent general purpose use microcontrollers which are in use today. Numerous peddlers have expanded microcontrollers, appeals of openMSP430 has huge in technical areas, robotics and telecommunications.

The feat the microcontroller convened by Texas relatively in today's technology. The device is a 16-bit processed under nanometer technology. In order enhance the attainment of microcontroller; we have enacted the circuit optimization on the device by open source tools as proton and Q-flow.

We here present the adaption from net-list to final GDS-II. We ascertained the model by synthesizing RTL codes by CMOS technology by redesigning the layout of the chip. The design performance can be enhanced by minimizing die area of chip by evaluating the power consumption using different technologies in the process.

2 .METHODOLOGY

In order to formulate a complete chip from its preliminary stage is a problematic task. The RTL codes from synthesis which includes STA and accomplishes under front end. After the offspring net-list from synthesis then it fallows by floor-planning to final

routing falls under back end process. Even though the process is common some of these vary from technology to technology as the enhancement of chip takes place. -

2.1 Synthesis

To curtail the design turn-around moment we procure openMSP430 which equivalents to 16-bit extracted from YOSYS source code. The process of converting RTL codes to net-list is synthesis. The codes are compiled by the accomplishment of design checks. The design with 500nm technology library is been synthesized with a clock frequency of 404.82 MHZ and die area to be feeblest. Once the design passes all the specifications and design checks then the gate level net-list is yielded which is expected in order to develop the layout of the design.

2.2 Floor planning

Floor-planning is a crucial that is interpreted after formulating a net-list in the synthesis. In this, the core area and routing area of the standard cells with the applicable values are set by the core utilization ratio. The standard cells are fairly placed once the floor plan is formulated without any optimization. The tool guides the phase of placement to place the cells in orderly fashion.

The valuable part of the VLSI is power planning after floor plan. In power planning the power nets, power

rings and power straps are formulated to the top metals of the design such that power will be ratifying through supply provided to the cells along power rails which are used to build the standard cells known as power network which is used to assess the current and resistance or IR drop.

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2.3 Placement and Routing

Placement is the successive stage after floor plan which purses after PNS. The performance, power, area (PPA) and timing optimizations as well it also checks CTS which are maintained by EDA tool. At this stage the cells are positioned in respective places which there after assessed with timing and congestions for violations. If any violations are found during this phase, they are stored based on clocks in ehich optimization and CTS are accomplished until they are controlled. The standard cells are to be placed in legal locations with no overlaps. By CTS the cells are placed on timing optimizations in order to built clock nets for all clock pins and macros. Skew should be as minimal as possible with reduction in insertion delays.

The tool acquires routing once the placement is completed. The placed cells are routed in order to pertain all the nets such that no open and shorts of nets should present while routing. The tool tries to route nets in order to connect all the cells. The DRC rules are honored at this phase in order to rectify the violations such as spacing, length and width between the cells that are routed. We should revert back to floor planning, placement and routing to resolve the offenses that ensued in DRC, some of violations are perceived by ECO route.

2.4 Physical verification

Physical verification is the final stage in which CTS and final area analysis are aimed before the GDSII file. Antenna check is another important parameter which is used to prevent the damage of chip during manufacturing. LVS is perpetrated to distinguish the physical layout with the schematic and optimized gate level net-list. It is mandatory to get final GDS in order to fabricate a chip.

3. RESULTS AND DISCUSSION

The below Fig-1 illustrates the floor plan of openMSP430. In the proposed floor plan the 0.7 area utilization is been utilized with die area of 3591144μm^2. From the diagram below the blue color represents the standard cells; black color represents the macros such as memories, flip-flops etc., white color represents the cells that the area left for routing during the routing stage.

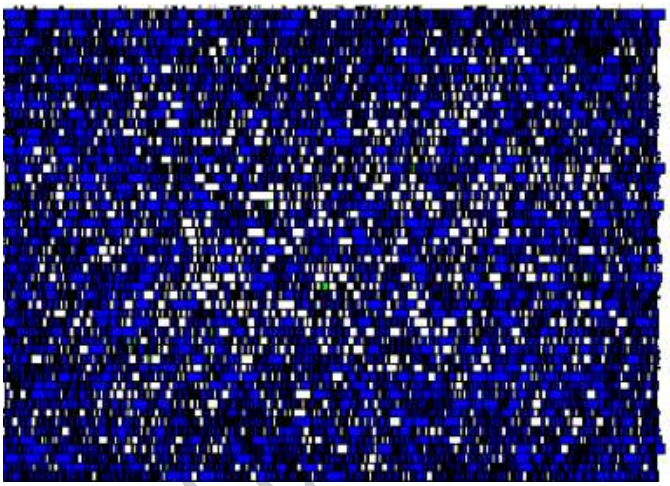

Fig -1: proposed floor plan of openMSP430

The layout of the design is been illustrated in the fig-2, 3. The view of the design layout is been done only when all the cells are placed in their respective places without any violations. The step CTS is been performed while routing in which filler cells are been used in the design while empty spaces are present at the time of routing in order to avoid the violations, at this phase buffers are also added in order to reduce the wire delay at the time of routing.

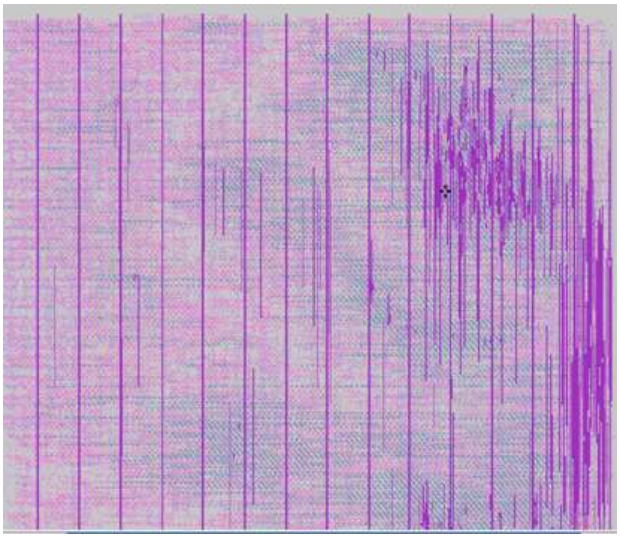

Fig -2: Final Layout of openMSP430

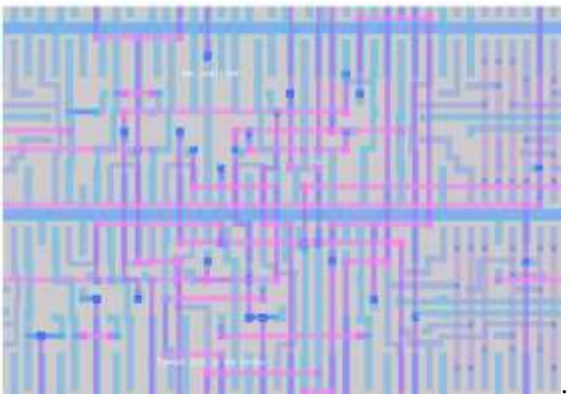

Fig -3: Center of the Layout of openMSP430

The fig-4 diagram represents the power report of the openMSP430 in the terms of milli watts with the significant reduction of channel length in which the significant switching speed of the logic components and less power required in order to turn on transistors. The power here considered is with macros and standard cells. The chip can be minimized by placing the standard cells carefully at the time of routing and optimization.

The below table-1 illustrates the assessment of different lower technologies with power, performance and area.

Group	Internal Power	Switching Power	Leakage Power	Total Power	
Sequential	9.79e-02	2.89e-03	3.75e-07	1.01e-01	37.5%
Combinational	1.26e-01	4.21e-02	6.39e-07	1.68e-01	62.5%
Macro	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.0%
Total	2.24e-01	4.50e-02	1.01e-06	2.69e-01	100.0%
	83.3%	16.7%	0.0%		

Fig -4: final power report of openMSP430

Table-1: comparison of power, performance and area of lower technologies of openMSP430.

Technology (nm)	Power (Watts)	Performance (Hz)	Area (μm^2)
45	$2.07*10^{-3}$	2.32 G	27774
180	$2.13*10^{-2}$	714.2M	399016
350	$1.10*10^{-1}$	471.6M	1596064
500	$3.19*10^{-1}$	404.85M	3591144

G-Giga: M-Mega

4. CONCLUSIONS

In this document, we have eventually inferred that the configuration of openMSp430 can be considerably strengthened by synthesizing the RTL codes from YOSYS using libraries of nanometer technology with variant technology size. We were able to diminish the die area up to 277774μm^2 and enhanced clock frequency up to 2.32 GHz which is found to be 10% power analysis with 70% utilization in the execution and optimization of openMSP430 derivatives.

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