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MULTILEVEL INVERTER

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ABSTRACT

The demand of electrical energy is increasing day-by-day, but the world is going through shortage of conventional energy sources. Hence the entire world is now interested in alternative source of energy among which solar PV energy is best alternative to generate electricity. It has long life compared to wind energy due to absence of rotating parts. The solar energy cannot be used directly since we get only DC, but our appliances works on AC. Thus, it requires a special converter called inverter to convert DC to AC. Earlier conventional two-level inverters have their drawbacks such as low efficiency and harmonics multilevel inverters are used which are more efficient and have myriads of advantages. In this book various multilevel inverter topologies and various modulation schemes are discussed.

Keywords: Inverter, Multi-level inverter, Total harmonic distortion, diode clamped inverter, cascaded H bridge multi-level inverter.

INTRODUCTION

INVERTER

The Inverter is an electrical device which converts direct current (DC) to alternate current (AC). For emergency backup power inverter is used in home. Some aircraft systems use inverter to convert a portion of the aircraft DC power to AC. The electrical devices like lights, radar, radio, motor and other devices use AC power. Recently industrial applications have begun to require high power. Industries possess certain appliances that require medium or low power for their operation. High power source usage for all industrial loads may prove beneficial to some motors that require high power, while it may lead damage to other loads. Utility applications of some medium voltage motor drives require medium voltage. Multi level inverter has become an alternative in high power and medium voltage situations. The Multi level inverter is used for industrial applications as alternative in situations of high power and medium voltage. There are three types of multilevel inverters. Diode clamped multilevel inverter is traditional topology is shown in Figure: 1. The main concept of this inverter is to use diodes and provides the multiple voltage levels through the different phases to the capacitor banks which are in series. A limited amount of voltage is transferred by diodes, reducing the stress on another electrical device. The input DC voltage is twice the maximum output voltage, which becomes the main drawback of the diode clamped multilevel inverter. By increasing the switches, diodes, capacitors the problem can be solved. The capacitor balancing issues limited them to the three voltage levels. Flying capacitors multilevel inverter is also existing method but it has better performance compared with Diode clamped MLI is also shown in figure: 2. the main concept of this inverter is usage of capacitors. Capacitor clamped switching cells are arranged seriously. The limited amount of voltage is transferred by capacitors to electrical devices. The switching states of the inverter are like in the diode clamped inverter. Diode clamping is not required in this type of multilevel inverters. The input DC voltage is twice the output voltage, became the drawback of the flying capacitors multi level inverter. The flying capacitors possess switching redundancy within the phase to balance out the capacitors. The active and reactive power flow can be controlled. Switching losses will takes place due to frequency.

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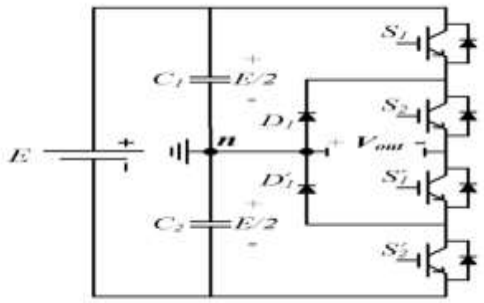

Figure: 1 Basic circuit diagram of Diode clamped Multi Level Inverter

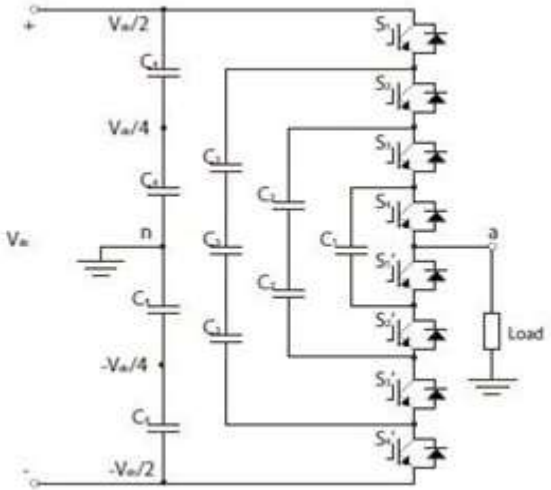

Figure: 2 Basic circuit of flying capacitor Multi Level Inverter.

The cascaded H-bridge multi level inverter is to use capacitors and switches and requires a smaller number of components in each level. This topology consists of series of power conversion cells and power can be easily scaled. The combination of capacitors and switches pair is called an H-bridge and gives the separate input DC voltage for each H-bridge. It consists of H-bridge cells and each cell can provide the three different voltages like zero, positive DC and negative DC voltages. The merits of this type of multi level inverter are its requirement of components in lesser quantity compared with diode clamped and flying capacitor inverters sections. The new alternate switching strategic methods are used for soft switching. The objective of the project is to design CASCADED H-BRIDGE INVERTER using Simulink with switches triggered by SPWM scheme by employing solar photo voltaic system implemented using FPGA resulting in reduce switching losses and total harmonic distortion by increasing output voltage levels. simulated using MATLAB SIMULINK. The operation of the inverter was studied in the MATLAB environment and the spectral studies were also carried out and recorded in this report. Inspired by the large number of ports, reduced coding complexity, speed and modularity the field programmable gate array will be used for the development of the hardware for this application. Multilevel Inverters are growing technology applicable to power electronics, Electric drive systems and Power systems etc. Even there are many topologies available in real world, here new multilevel topologies are discussed, and comparative results are analysed. Solar Photo Voltaic system is employed to compete the disadvantages of conventional energy sources and resulted in energy conservation system that reduces power consumption. Thus, by computing switching angles for various modulation indexes proved that the range of modulation index between 0.53 to 0.78 resulting in reduced total harmonic distortion value of 32%.

Multilevel Inverter:

Inverter is power electronic circuit that converts a direct current into an alternative current power of desired magnitude and frequency. The inverters find their application in modern ac motor and uninterruptible power supplies. The conventional inverters yield only two voltage levels. To improve voltage level multilevel inverters are used which starts with three level inverters which are economical for medium and high-power applications. In comparison to conventional inverters it has lower switching losses, lower harmonics and better electromagnetic compatibility.

Classification of Inverter:

The various multilevel inverter topologies are shown in the table.

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Table 1 Classifications of Various Inverter Topologies

Parameters classifying Inverters	Types of Inverters
Sources	Voltage source inverters Current source inverters
Switching methods	Pulse width modulation Square wave inverters
Switching devices	Transistorized inverter Thyristor zed inverter
Inversion principle	Resonant inverter Non-Resonant inverter

Multilevel Inverter Topology

Multilevel inverter technology has emerged recently as a very important alternative in the area of high-power medium-voltage energy control.This increased attention is probably due to the fact that the output waveforms are much improved over those of the two-level inverter technologies, and that the voltage rating of the inverter is increased due to the series connection of the devices.Multilevel inverters have grown better counterparts to conventional two-level inverters. Commonly employed multilevel inverter topologies are Diode clamped, Capacitor clamped and Cascaded Multilevel inverters. In all these topologies, output voltage is synthesised from several levels of input voltages obtained from several capacitors connected across the dc bus. In Capacitor clamped inverter, both real and reactive power can be controlled, but it suffers from high switching losses due to real power transfer thus reducing the efficiency of power conversions. Also, it requires a large number of storage capacitors at higher levels. The Cascaded inverter uses a large number of separate dc source for each of the bridges. However, in the diodeclamped topology, all devices are switched at fundamental frequency resulting in low switching losses and high efficiency. Other main feauters of this topology are controlled reactive power flow between source and load, much better dynamic voltage sharing among switching devices and simple topological structure. Therefore, diode clamped inverter topology is considered here for study. The control logic is simple, especially for back-to-back inter-tie connection of two systems.

Advantages of Multilevel Inverter

1. Devices of lower rating can be used thereby enabling the schemes to be used for high voltage applications.
2. Reduced total harmonic distortion (THD).
3. The dv/dt and EMI from the system is low.
4. Lower switching frequencies can be used and hence reduction in switching losses.

Disadvantages of Multilevel Inverter

1. The number of isolated DC-links are more compared to a two-level inverter.
2. Neutral point voltage variations.
3. Power bus structure and hence the control schemes become complex as the number of levels increases.
4. Decrease in Reliability.

Harmonic distortion

One of the biggest problems in power quality aspects is the harmonic content in the electrical system. Generally, harmonics may be divided into two types: 1) voltage harmonics, and 2) current harmonics. Current harmonics is usually generated by harmonics contained in voltage supply and depends on the type of load such as resistive load, capacitive load, and inductive load. Both harmonics can be generated by either the source or the load side. Harmonics generated by load are caused by nonlinear operation of devices, including power converters, arc-furnaces, gas discharge lighting devices, etc. Load harmonics can cause the overheating of the magnetic cores of transformer and motors. On the other hand, source harmonics are mainly generated by power supply with non-sinusoidal voltage waveform. Voltage and current source harmonics imply power losses, Electromagnetic Interference (EMI) and pulsating torque in AC motor drives. Any periodic waveform can be shown to be the superposition of a fundamental and a set of harmonic components. By applying Fourier transformation, these components can be extracted. The frequency of each harmonic component is an integral multiple of its fundamental. There are several methods to indicate of the quantity of harmonics contents. The most widely used measure in North America is the total harmonics distortion (THD), which is defined in terms of the amplitudes of the harmonics, *Hn*, at frequency nw_0, 2 where w_0 is frequency of the fundamental component whose amplitude of *H1* and *n* is integer. The THD is mathematically given by

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$$\sqrt{\sum_{n=2}^{\infty} H^{2}{}_{(n)}} \; / \; H_1 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(1)$$

Application of Multi Level inverters:

1. High Power Applications.
2. Where ever need sinusoidal supply, this type of inverter circuit can be implemented.
3. To improve the harmonic characteristics, a five-level inverter could be modulated by a multilevel carrier technique such as four-level carrier modulation.
4. For our parallel connection, on the other hand, a specific technique has been devised and designed, so that the apparent carrier can be increased to eight levels. In this section, some techniques for devising and designing the carriers will be presented.

Functional Diagram Of Multilevel Inverter

Figure 1.1 represents the schematic diagram of one phase leg of inverers with different number of levels, for which the action of the power semiconductor is represented by an ideal switch with several positions. A two-level inverter generates an output voltage with two levels with respect to the negative terminal of the capacitor, while the three-level inverter generates the three levels and so on.The term multilevel starts with the three-level inverter introduced by Nabaeetal. By increasing the number of levels in the inverter, the output voltages have more steps genertaing a staircase waveform, which has a reduced harmonic distortion. However, a higher number of level increases the control complexity and introduces voltage imbalance problems.

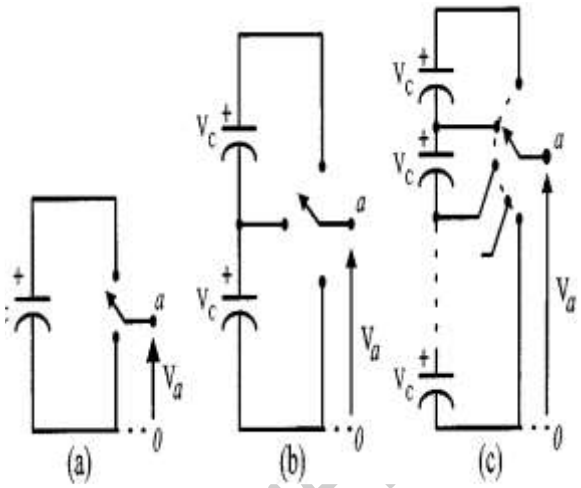

Figure 3 One phase leg of an inverter with (a) two-level, (b) three-level and (c) n-level.

Types of Multilevel inverters:

Diode-clamped multilevel inverter

The most commonly used multilevel topology is the diode clamped inverter, in which the diode is used as the clamping device to clamp the dc bus voltage to achieve steps in the output voltage. Figure 2.1 shows the circuit for a diode clamped inverter for a three-level and a four-level inverter. The key difference between the two-level inverter and the three-level inverter are the diodes D_{1a} and D_{2a}. These two devices clamp the switch voltage to half the level of the dc-bus voltage. In general, the voltage across each capacitor for an N level diode clamped inverter at steady state is vdc/(n-1) Although each active switching device is only required to block, the clamping devices have different ratings. The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series of capacitors. According to the original invention, the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels [4] where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped (NPC) inverter was introduced [4]. However, with an even number of voltage v_{dc} / (n-1) levels, the neutral point is not accessible, and the term multiple point clamped (MPC) is sometimes applied [5]. Due to capacitor voltage balancing issues,

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the diode-clamped inverter implementation has been limited to the three levels. Because of industrial developments over the past several years, the three-level inverter is now used extensively in industry applications. Although most applications are medium-voltage, a three-level inverter for 480V is on the market.

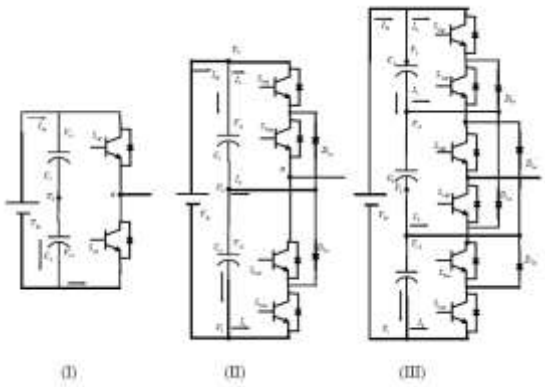

Figure 4: Topology of the diode-clamped inverter (I) two-level inverter, (II) three-level inverter, (III) four-level inverter.

In general, for a N level diode clamped inverter, for each leg 2 (N-1) switching devices, (N-1) * (N-2) clamping diodes and (N-1) dc link capacitors are required. When N is sufficiently high, the number of diodes and the number of switching devices will increase and make the system impracticable to implement. If the inverter runs under pulse width modulation (PWM), the diode reverse recovery of these clamping diodes becomes the major design challenge.

Cascaded multilevel H-bridge inverter

The cascaded-H- bridge inverter where a seven level H bridge cell is connected in series with a three-level cell. The complete topology involves three phases. This is a combinational topology in a couple of senses. First, the five-level cell is a combination of the diode-clamped and H-bridge topologies. Next, the five level cells are inserted into the series H-bridge inverter in place of a three-level cell. In general, any number of cells having any number of levels is possible. The dc voltage ratio can be selected to maximize the number of voltage levels. However, the maximum case suffers from the disadvantage that negative dc currents in the lower voltage cell will distort the dc voltage if a transformer/rectifier source is used to supply *vadc*2. One solution to this problem is to use a ratio of *vadc*1 = 4*vadc*2 instead which reduces the number of voltage levels to eleven. The per-phase RSS can be used to avoid negative dc source currents. Also, per-phase RSS within the five-level cell can be used to ensure that each of the capacitors is charged to one-half of the supply voltage *vadc*1. In general, any number of cells can be placed in series and only one isolated dc source is needed per phase. If the number of voltage levels is lowered to nine. lt shows that both cells are switching at nearly the same frequency.

PULSE WIDTH MODULATION

Usually, the on- and off-states of the power switches in one inverter leg are always opposite. Therefore, the inverter circuit can be simplified into three 2-position switches. Either the positive or the negative dc bus voltage is applied to one of the motor phases for a short time. Pulse width modulation (PWM) is a method whereby the switched voltage pulses are produced for different output frequencies and voltages. A typical modulator produces an average voltage value, equal to the reference voltage within each PWM period. Considering a very short PWM period, the reference voltage is reflected by the fundamental of the switched pulse pattern.

Characteristic of the Pulse Width Modulation (PWM)

The essential parameters of the multilevel inverter are:
The index of modulation is:

$$m=f_p/f_r$$

Where:

f_r is the frequency of the reference.

f_p is the frequency of the carrying wave.

The control factor in voltage is $f=A_r/A_p$

A_r: Amplitude of the reference.

A_p: Amplitude of the carrying wave

Symmetrical sampling PWM

In regular sampling technique, the reference waveform is sampled at regularly spaced intervals. Normally, the sampling takes places at the triangular waveform peaks. With one sample per carrier cycle the output is a double edge modulated waveform, which is symmetrical with respect to the center point between the two consecutive samples. The modulation process is termed symmetrical modulation because the intersection of adjacent sides of the triangular carrier waveform with the stepped sine wave, about the non-sampled carrier peak, is equidistant about the carrier

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peak. figure 1.3 illustrating the general features of symmetrical sampling PWM.

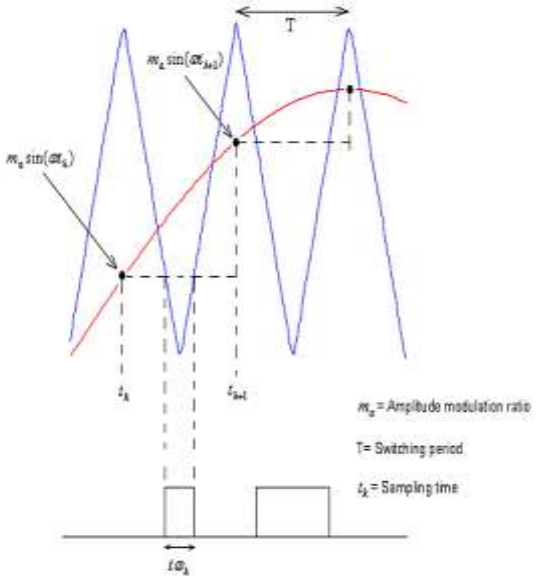

Figure 5 Symmetrical regular PWM

Asymmetrical Sampling PWM

The asymmetrical modulation is produced when the triangular carrier waveform is compared with a stepped sine wave produced by sampling and holding at twice the carrier frequency. Each side of the triangular carrier waveform about a sampling point, intersect the stepped waveform at different step level. The resultant pulse width is asymmetrical about the sampling point as illustrate in figure 1.4. By using this technique, the dynamic response can be improved and produces less harmonic distortion of the load current.

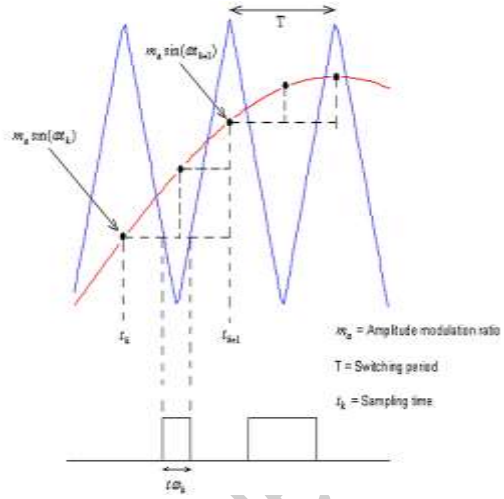

Figure 6 Asymmetrical regular PWM

Sinusoidal Pulse Width Modulation

A very popular method of controlling the voltage and frequency is by sinusoidal pulse width modulation. In this method, a high-frequency triangle carrier wave is compared with a three-phase sinusoidal waveform, as shown in figure 4.3. The power devices in each phase are switched on at the intersection of sine and triangle waves. The amplitude and frequency of the output voltage are varied, respectively, by varying the amplitude and frequency of the reference sine waves. The ratio of the frequency of the sine wave to the frequency of the carrier wave is called the modulation index. The carrier and reference wave are mixed in a comparator. When sinusoidal wave has magnitude higher than the triangular wave, the comparator output is high, otherwise it is low. The comparator output is processed in a trigger pulse generator in such a manner that the output voltage wave of the rectifier has a pulse width agreement with the comparator output pulse width.

Reference Signals

They are sinusoidal signals shifted between them of 120° and are characterized by the amplitude A_r and its frequency f.

$$V_{ref_a} = A_r \sin(2\Pi ft).....(2)$$

$$V_{ref_b} = A_r \sin(2\Pi ft - 2\Pi/3).....(3)$$

$$V_{ref_c} = A_r \sin(2\Pi ft - 4\Pi/3).....(4)$$

The Carrying Wave

The carrying triangular wave is characterized by the amplitude A_p and the frequency f_p, $f_p=1/t_p$. The intersections between the reference voltage standards

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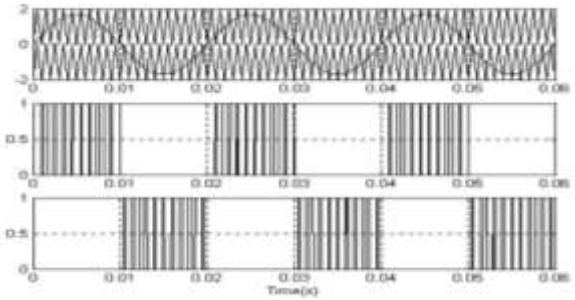
and the carrying wave give the time of opening and closing of the switches.



APPLICATION

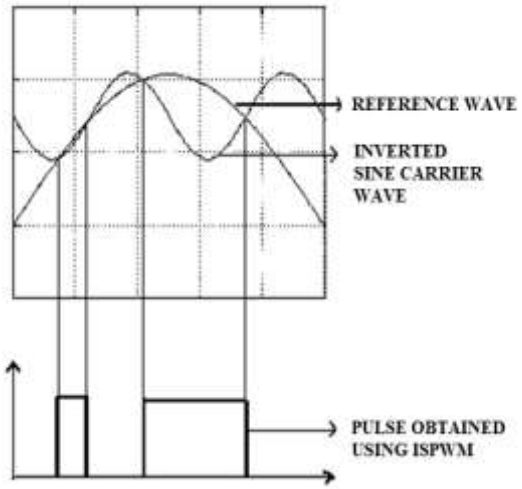
In many industrial applications, Sinusoidal Pulse Width Modulation (SPWM), also called Sine coded Pulse Width Modulation, is used to control the inverter output voltage. SPWM maintains good performance of the drive in the entire range of operation between zero and 78 percent of the value that would be reached by square-wave operation. If the modulation index exceeds this value, linear relationship between modulation index and output voltage is not maintained and the over-modulation methods are required.

INVERTED SINE PULSE WIDTH MODULATION

The proposed control strategy replaces the conventional fixed frequency carrier waveform by variable frequency inverted sine wave. The inverted sine PWM has a better spectral quality and a higher fundamental voltage compared to the triangular based PWM was shown in figure 1.6. But the main drawback is the marginal boost in the magnitude of lower order harmonics and unbalanced switch utilization. This is overcome by employing variable frequency inverted sine carrier signals was shown in figure 1.7 In order to balance the number of active switching among the levels is to vary the carrier frequency based on the slope of the modulating wave in each band. The frequency ratio for each band should be set properly for balancing the switching action for all levels.

Generation of Pulse using ISPWM

An inverted sine wave of high switching frequency is taken as a carrier wave and is compared with that of the reference sine wave. The pulses are generated whenever the amplitude of the reference sine wave is greater than that of the inverted sine carrier wave.



Carrier and Reference wave for ISPWM Technique

ISPWM control strategy replaces the triangular based carrier waveform by inverted sine wave. The ISPWM method uses sine as reference signal while the carrier signal is an inverted sine that helps to maximize fundamental voltage and reduce THD. From figure 1.7 it is clear that the pulses are generated whenever the amplitude of reference sine wave is greater than that of the inverted sine carrier wave. Carrier frequencies are selected such that the number of switching in each band is equal.

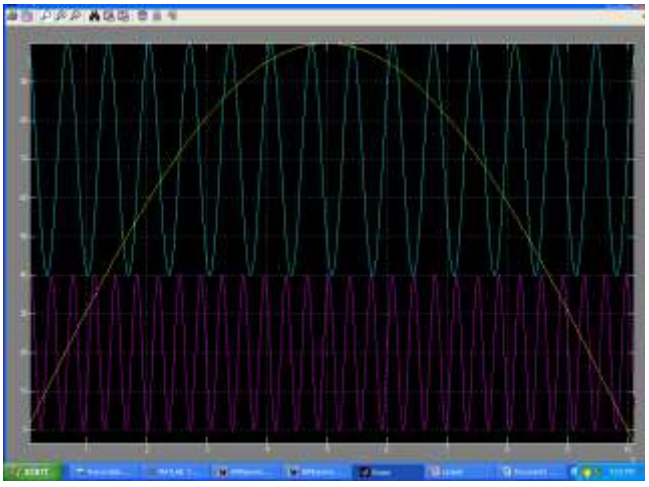


Figure 7 Carriers and Reference for ISPWM

Advantages of ISPWM

1. It has a better spectral quality and a higher fundamental component compared to conventional PWM (SPWM) without any pulse drooping.

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2. The ISPWM strategy enhances the fundamental output voltage particularly at lower modulation index ranges.
3. There is a reduction in total harmonic (THD).
4. The appreciable improvement in the THD in lower range of modulation index attracts drive application where low speed operation is required.

SOLAR PANEL:

A solar panel is a set of solar photovoltaic (PV) modules electrically connected and mounted on a supporting structure. A PV module is a packaged, connected assembly of solar cells. Solar panels can be used as a component of a larger photovoltaic system to generate and supply electricity in commercial and residential applications. Each module is rated by its DC output power under standard test conditions (STC), and typically ranges from 100 to 320 watts. The efficiency of a module determines the area of a module given the same rated output - an 8% efficient 230-watt module will have twice the area of a 16% efficient 230-watt module. There are a few solar panels available that are exceeding 19% efficiency. A single solar module can produce only a limited amount of power; most installations contain multiple modules. A photovoltaic system typically includes a panel or an array of solar modules, an inverter, and sometimes a battery and/or solar tracker and interconnection wiring.

Construction:

Solar modules use light energy (photons) from the sun to generate electricity through the photovoltaic effect. The majority of modules use wafer-based crystalline silicon cells or thin-film cells based on cadmium telluride or silicon. The structural (load carrying) member of a module can either be the top layer or the back layer. Cells must also be protected from mechanical damage and moisture. Most solar modules are rigid, but semi-flexible ones are available, based on thin-film cells. These early solar modules were first used in space in 1958. Electrical connections are made in series to achieve a desired output voltage and/or in parallel to provide a desired current capability. The conducting wires that take the current off the modules may contain silver, copper or other non-magnetic conductive transition metals. The cells must be connected electrically to one another and to the rest of the system. Externally, popular terrestrial usage photovoltaic modules use MC3 (older) orMC4 connectors to facilitate easy weatherproof connections to the rest of the system. Bypass diodes may be incorporated or used externally, in case of partial module shading, to maximize the output of module sections still illuminated. Some recent solar module designs include concentrators in which light is focused by lenses or mirrors onto an array of smaller cells. This enables the use of cells with a high cost per unit area (such as gallium arsenide) in a cost-effective way. Thus, the various inverter topologies and various modulation schemes for triggering inverter switches are discussed in this chapter. In the next chapter reviewed reference papers related to the base paper concepts are discussed.

LITERATURE REVIEW

Cascade Multilevel Inverter with Phase Shift SPWM and its Application in STATCOM

This paper deals with the application of cascade multilevel inverter in static synchronous compensation. It succeeds the conventional transformed based multiphase inverters and employing phase-shift sinusoidal pulse width modulation to control the switching devices of each voltage source inverter. The devices operate higher carrier frequency which causes distortion even though it resulted in various advantageous factors such as less power loss due to transformer less design, dynamic response is fast. It could be directly connected o power distribution system without employing transformer. These specific factor features enable a simplified designing and implementation of filter. The study of this paper enables us to analyse the superiority of proposed STATCOM system

Comparison of Neutral point clamped inverter and Symmetrical inverter

Here the three different topologies used in drive system such as neutral point clamped, flying capacitor and symmetrical cascaded multilevel inverter are discussed. It possesses a same DC link for all legs but in symmetric and asymmetric DC link is separately given the space vector modulation technique used in voltage source inverter to decrease harmonic content of output voltage and to decrease the number of

computations. Neutral point clamping is simple to use. It uses small number of semiconductor devices employing only one dc voltage source to supply more legs. Whereas symmetrical inverter has high conduction and power loss and asymmetric inverters possess high switching losses

Comprehensive Relationship between Carrie Based PWM and Space vector PWM in a Five Phase VSI

This paper aimed at providing a comprehensive relationship between carriers-based pulse width modulation and space vector pulse width modulation techniques. The main reason for multiphase machines to be employed for applications such as locomotive traction and high-power applications is for its better fault tolerance and reduction in power loss and lower rating of semiconductors. In carrier-based pulse width modulation the signal is generated by keeping carrier frequency much high compared to modulating signal. In space vector pulse width modulation, the active space vectors used to increase 5.15% of dc bus compared to carrier-based pulse width modulation.

Implementation and Control of Distributed PWM Cascaded Multilevel Inverter with Minimal Total Harmonic Distortion and Common Mode Voltage

This paper speaks about the implementation of cascaded inverter achieved through the series connection of single-phase H bridge modules. It deals with design of an integrated power bridge with its own digital signal processor and signal conditioning circuitry, networked control algorithm and signal protocol needed for modular implementation of a cascaded inverter with PWM computation. The presented modular implementation concepts are verified to be accurate and effective by the close match between simulation and experimental results using cascaded inverter. The accuracy can only be achieved through the proper design of power bridges and networked control algorithm.

Multilevel Converters or Large Electric Drives

This paper deals about the multilevel inverter that can generate near sinusoidal voltages with only fundamental frequency switching. It has almost no electromagnetic interference (or) common mode voltage. It is suitable for large voltage ampere rated (or) high voltage motor drives. It has high efficiency because the devices can be switched at minimum frequency. Power factor close to unity for multilevel inverter used as rectifier to convert the alternating current to direct current. Here no change unbalance problem results with converters in either charge mode (or) drive mode. The paper's simulation results show out the superiority of these two converters over two level pulse width modulation-based drives.

New Configuration for the Three-phase five level Asymmetrical Multilevel Inverter

This paper deals with the employment of three phase six switch voltage source inverter with single phase H bridge to design out asymmetrical multilevel inverter. It is an advantageous structure to obtain a high resolution. We reviewed the way to reduce the number of insulated supplies and to improve the energetic efficiency. We have shown that this problem can be overcome for three phase application and that these previously rejected configurations are usable. In addition, some new configuration with even higher resolution have been proposed. The new available configuration extends the design flexibility and the possibilities to optimize out the combined device matching.

Study of Simplified SVPWM Algorithm Based on Three Level Inverter

The importance of three level inverter is compared to conventional two-level inverter in this paper. It also speaks about the three-level inverter space vector pulse width modulation which simplifies the calculation and also facilities the realization of simulation Its simulation results show out its excellent performance which will benefit for the research and improvement of grid-connected photovoltaic inverter's control strategy. In this paper SVPWM can be effective to solve problems such as high harmonic content and complex separation of traditional Direct current, Alternating current technology. It resulted in higher utilization of DC voltage and lower harmonic content and also facilities the streamlined control algorithm

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Three-Dimensional Space Vector Modulation Reduce Common Mode Voltage for Multilevel Inverter

Two level pulse width modulation inverters are compared with multilevel inverter which has the capability to reduce the common mode voltage responsible for bearing current. The complete elimination of common mode voltage increases the step magnitude in the line voltage. The proposed three-dimensional technique of space vector modulation achieves the trade-off between the magnitude of common mode voltage, line voltage step magnitude and elimination of lower order harmonics in the inverter output voltage. These concepts can be applied to medium as well as low voltage drives increase the life of bearing and improve reliability of motor and three dimensional SVPWM is implemented using Digital signal processor.

EXIXTING SYSTEM

Requirement of high-power capacitors for voltage sharing increases the cost of the existing system. The numbers of diodes employed get increases to achieve high voltage levels at output to reduce harmonic distortion thus resulted in high cost solution problems. Reduced power consumption by employing solar PV module in the place of conventional energy sources. Atmel microcontroller where each pin is assigned for specific application. Thus, coding compatibility is difficult. Whereas the problem is mitigated by employing FPGA which has high reconfigurability feature.

PROPOSED WORK

Designing cascade-H-bridge inverter using Simulink. Achieving reduced total harmonic distortion by increasing the output voltage levels. Reducing the switching losses by employing carrier based Sinusoidal Pulse Width Modulation scheme. Employing solar photo voltaic module to energize switching circuits of inverter.

ADVANTAGES OF PROPOSED WORK

1. Switching loss is reduced by cascaded-H-bridge configuration.
2. Power consumption is achieved by employing solar photo voltaic module.
3. Harmonic distortion is reduced by increasing output voltage levels.
4. Reduced usage of high-power capacitors for voltage sharing as separate dc sources are used.
5. 2N+1 level can be achieved with n diodes. Thus, reduces number of diodes employed.

APPLICATION

1. Adjustable speed ac drives,
2. UPS static VAR compensators
3. Active filters
4. Flexible AC transmission system
5. In all vehicle for lightning
6. Now also used for driving electric vehicle

DESCRIPTION

In practice to improve the harmonics characteristic of the parallel-connected seven level inverter design. It is found that the dc current flow through the dc power supplies can be controlled by means of phase shifting of the injected third order harmonics. In the case of svc, the output capacitor voltage can be controlled by means of this technique. The switching signal for the inverter generated using the field programmable gate array. In this project the AC is converted in to dc for input to level the inverter. The filter block is used to suppress the ac components and stiff dc voltage. The gate driver circuit performs three operation the first one is to boost the mc output pulse, second one is the impedance matching for the mc and gate & emitter terminal circuit and the third one is to provide is isolation between the pulse generation unit to power circuit .three phase seven level inverter circuit configuration with seven level inverter block consist 16 power mosfets to convert multi level ac output **.**

Lm7805 voltage regulator

DESCRIPTION

The MC78XX/LM78XX/MC78XXA series of three terminal positive regulators are available in theTO-

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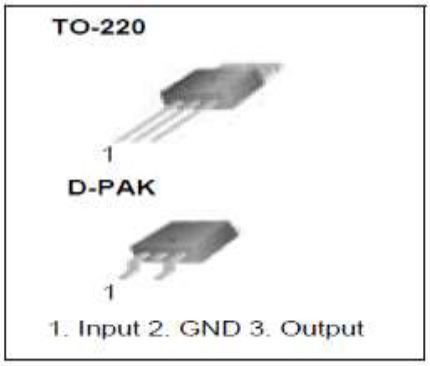
220/D-PAK package and with several fixed output voltages, making them useful in a wide range of applications. Each type employs internal current limiting, thermal shut down and safe operating area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents

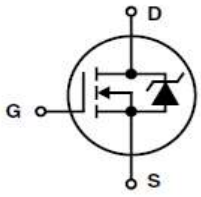
Features



- Output Current up to 1A
- Output Voltages of 5, 6, 8, 9, 10, 12, 15, 18, 24V
- Thermal Overload Protection
- Short Circuit Protection
- Output Transistor Safe Operating Area Protection

MOSFET

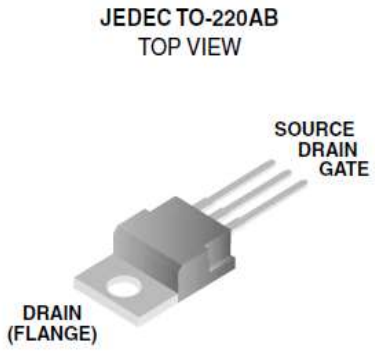
Symbol



Features

- 8A, 500V
- Nanosecond Switching Speeds
- High Input Impedance

PACKAGING:



MOSFET SECTION

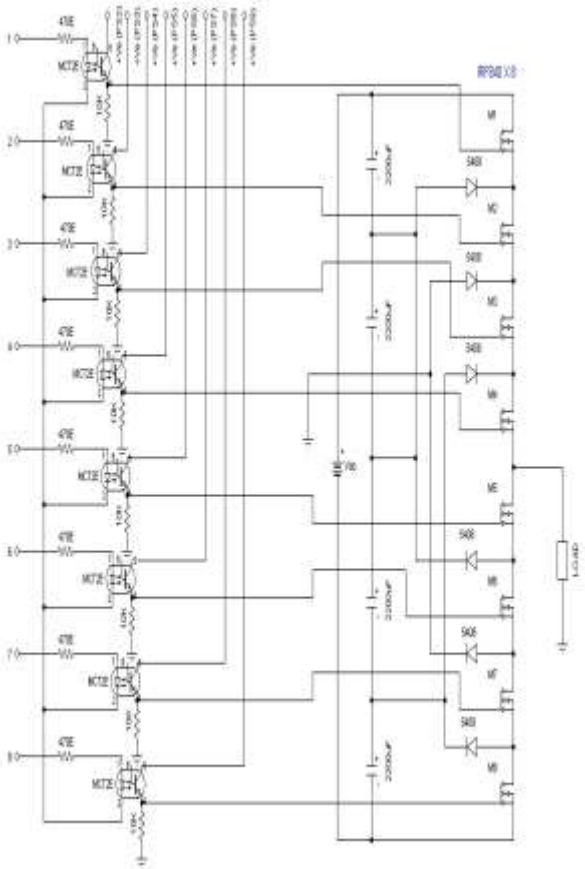


Figure 8 MOSFET Section

POWER SUPPLY UNIT

A Power supply is a device that supplies electrical or other types of energy to an output load or group of loads.

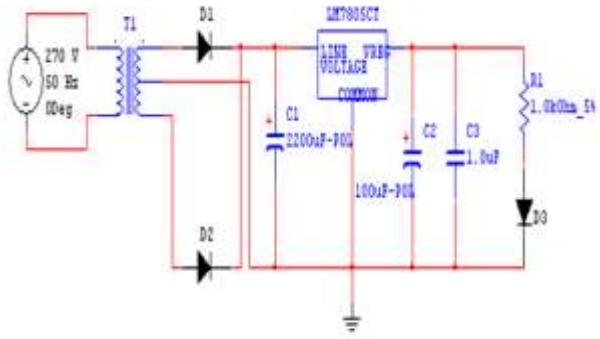


Figure 9: Power Supply to the Driver Circuit

BRIDGE RECTIFIER: A Rectifier is an electrical device that converts alternating current to direct current or at least to current with only positive value, a process known as rectification.

TRANSFORMER: A transformer is a static piece of which electric power in one circuit is transformed into electric power of same frequency in another circuit.

REGULATORS: The voltage regulator is a device, which maintains the output voltage constant irrespective of the change in supply variations, load variations & temperature changes.

FILTERS: A Filter section is used to convert pulsating dc to a purer, more desirable form of dc voltage.

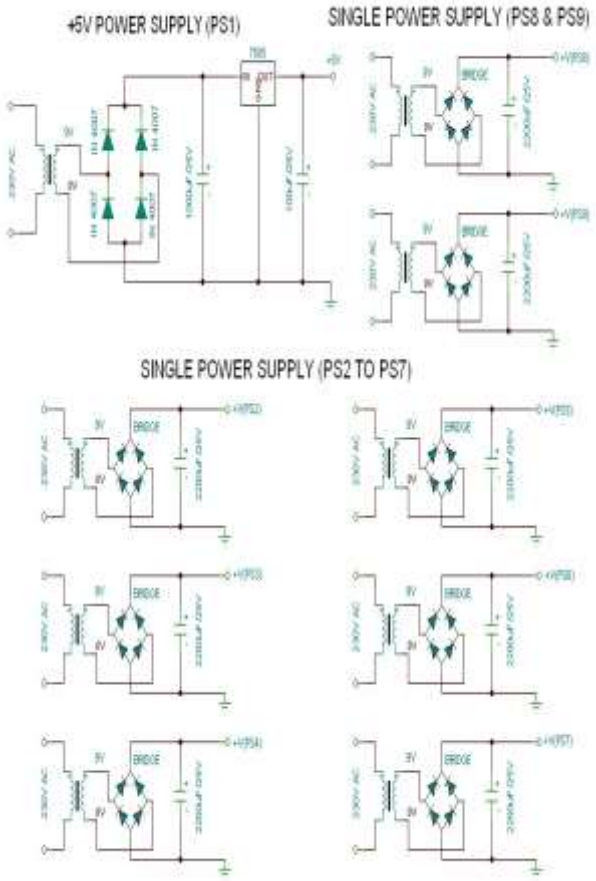


Figure 10 Power Supply Section

DRIVER UNIT

The driver unit usually isolates the control circuit and the power circuit and ensures the safe operation of the equipment.

OPTOCOUPLERS: Optocouplers are used to isolate the control voltage from the controlled circuit.

DESCRIPTION

The MCT2XXX series opto isolators consist of a gallium arsenide Infrared emitting diode driving a silicon phototransistor in a 6-pin Dual in-line package.

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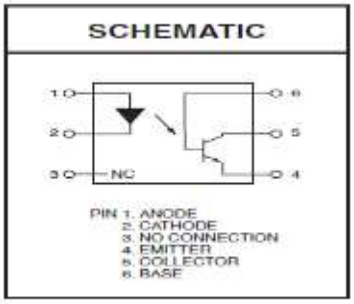

APPLICATIONS

- Power supply regulators
- Digital logic inputs
- Microprocessor inputs

Thus, in this chapter the cascaded-h-bridge configuration, hardware description of MOSFET switching sections and their constructions in Simulink module were discussed in a detailed manner. The simulated results were discussed in the next chapter.

SOFTWARE IMPLEMENTATION

Simulation is an effective tool by which we can experience the practical results through the software. There is a number of simulation software available, and the most efficient tool is the MATLAB. Here we have a number of parts of MATLAB. We employ the Simulink part of the MATLAB.

Simulation parameters

The parameters chosen for simulation using the ISPWM technique is shown below

Table 2 Performance parameters for simulation using ISPWM

S.NO.	PARAMETERS	VALUES
1	Main DC source voltage (V_{dc})	100v
2	Carrier frequency	2821Hz, 1478 Hz
3	Rated output frequency	50 Hz
4	Load, R	10k
5	Lowpassfiltercutoff frequency	50 Hz
6	Damping factor	0.707

Simulink model of SPWM

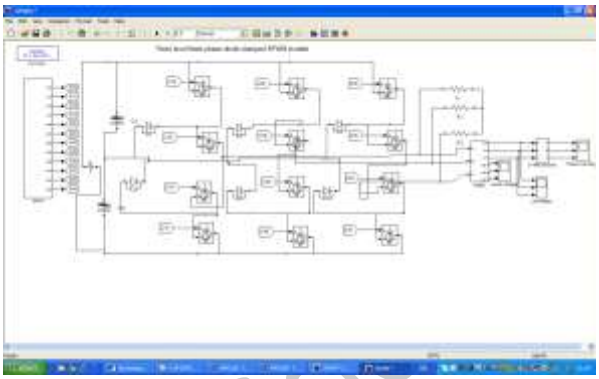

Figure 3.1 Simulation diagram of SPWM

Simulink model of SPWM was shown in the figure 9 SPWM circuit using CHB topology was simulated. The subsystem used to provide the gating pulse to this switch. The solar module used for switch controlling operation. Total Harmonic Distortion is computed using power graphics user interface tool. The line voltage and Phase voltage for CHB circuit is also obtained through simulation.

Gate pulse generation for SPWM

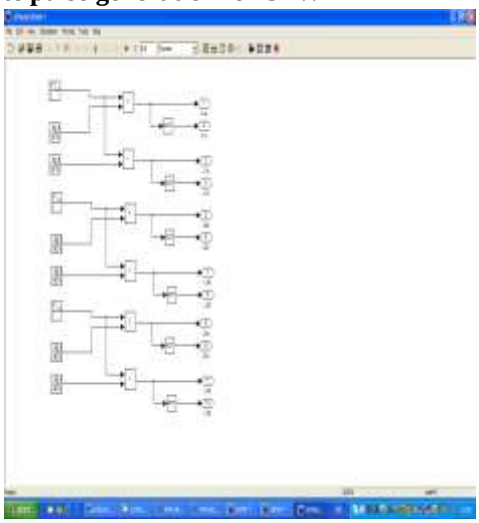

Figure 10 Simulation diagram of gating pulse generation of SPWM

- The triangular carrier wave and reference sine wave was mixed in a comparator. The

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comparator produces output when amplitude of sine wave was greater than amplitude of triangular wave.

- The output is logic 1 if the amplitude of sine wave is greater than the carrier wave. Thus, the output is the stepped waveform which is equivalent to reference sine waveform.
- The comparator output is processed in a trigger pulse generator in such a manner that the output voltage wave of the rectifier has a pulse width agreement with the comparator output pulse width.

LINE VOLTAGE OUTPUT FOR SPWM

SEVEN LEVEL OUTPUT

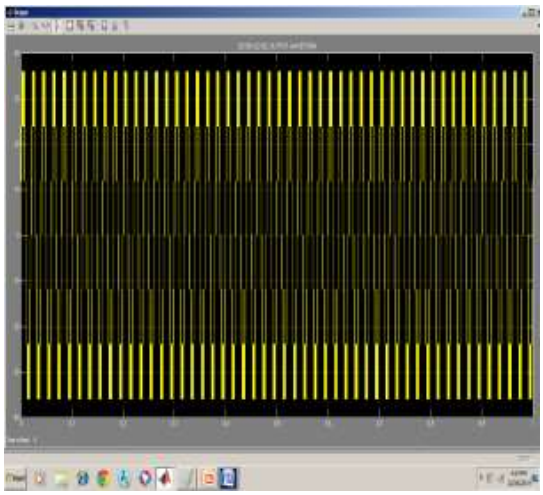

Figure 11 line voltage output

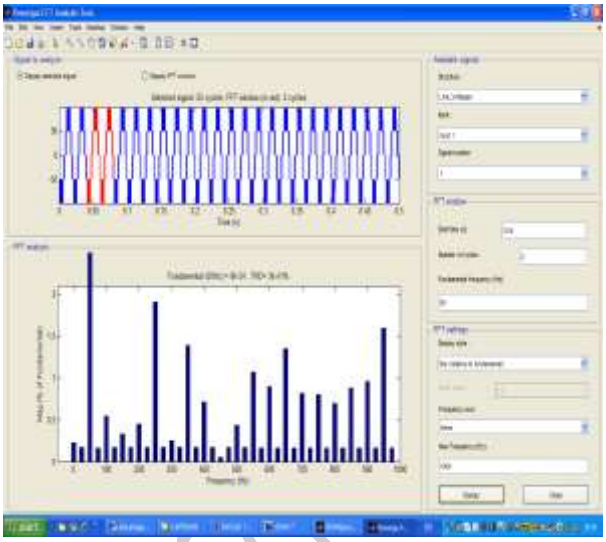

Figure 12 FFT analysis of Line voltage output

From the FFT spectrum analysis THD=34.54, fundamental voltage=84.54v. From SPWM technique, the stepped Line voltage output are $+v_{dc}$=100v, $+v_{dc}/2$=50v, 0, $-v_{dc}/2$=-50v, $-v_{dc}$=-100v.

Simulink model of ISPWM

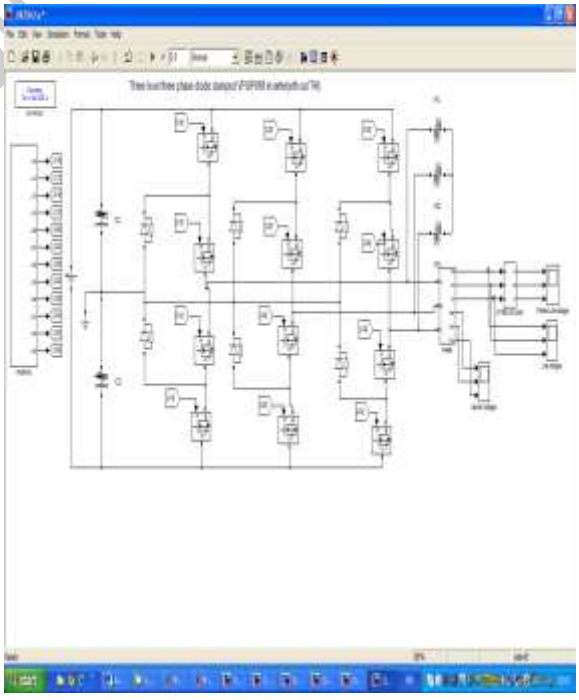

Figure 13 Simulation diagram of ISPWM

Simulink model of ISPWM was shown in the figure 3.4. ISPWM circuit using NPC topology was simulated. The subsystem used to provide the gating pulse to this switch. Powerful was used for FFT analysis for output. Total Harmonic Distortion is computed using power graphics user interface tool. The line voltage and Phase voltage for CHB circuit is also obtained through simulation.

Gate pulse generation for ISPWM

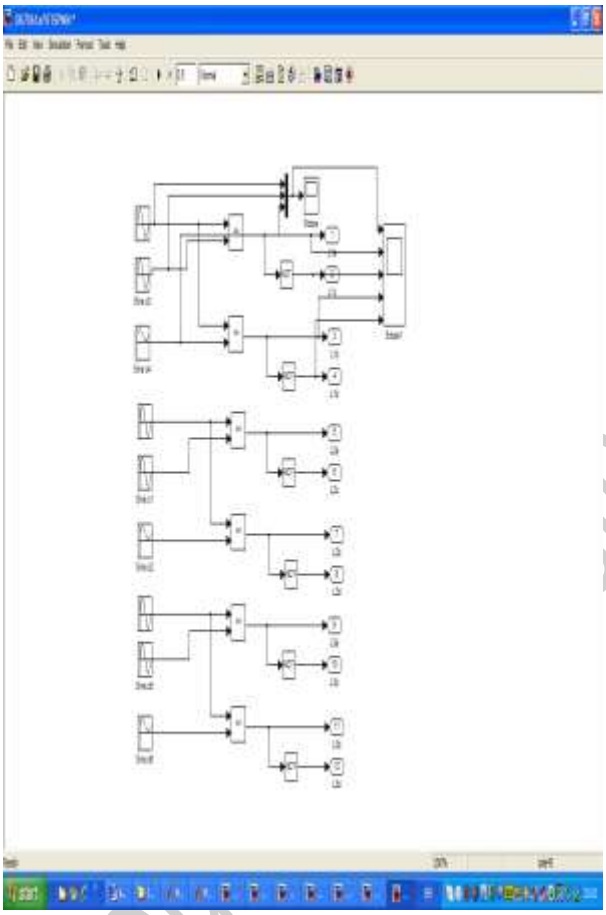

Figure 14 Simulation diagram of gating pulse generation of ISPWM

The inverted sine carrier wave and reference sine wave was mixed in a comparator. The comparator produces output when amplitude of sine wave was greater than amplitude of inverted sine wave. Amplitude of sine wave was 100 and amplitude of inverted sine carrier wave are 20, 40. The comparator output is processed in a trigger pulse generator in such a manner that the output voltage wave of the rectifier has a pulse width agreement with the comparator output pulse width.

LINE VOLTAGE OUTPUT

LINE VOLTAGE OUTPUT FOR ISPWM

SEVEN LEVEL OUTPUT

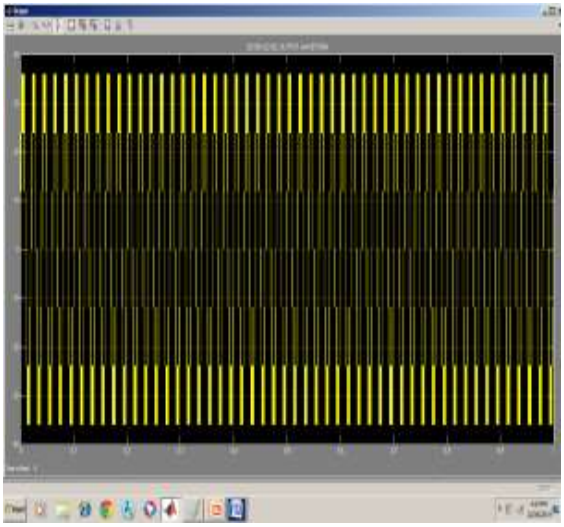

Figure15 Line voltage output

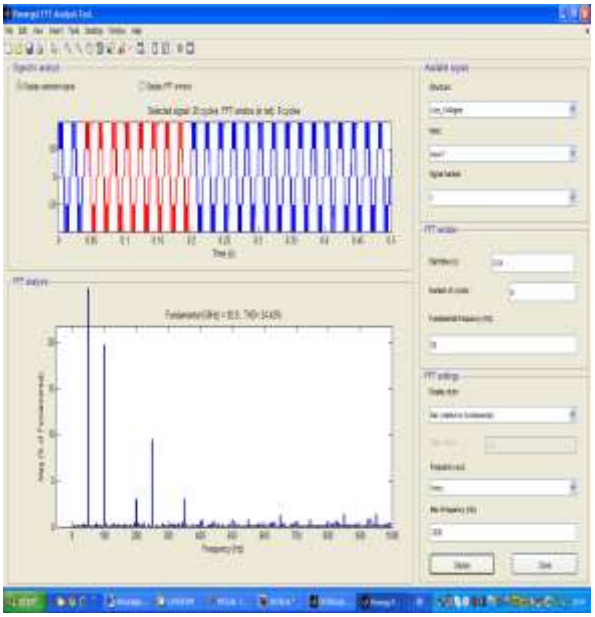

Figure 16 FFT analysis of Line voltage output

From the FFT spectrum analysis THD=24.42, fundamental voltage=92.8v. From ISPWM technique, stepped Line voltage output are $+v_{dc}$=100v, $+v_{dc}/2$=50v, 0, $-v_{dc}/2$=-50v, $-v_{dc}$=-100v.

Simulink model of THI-ISPWM

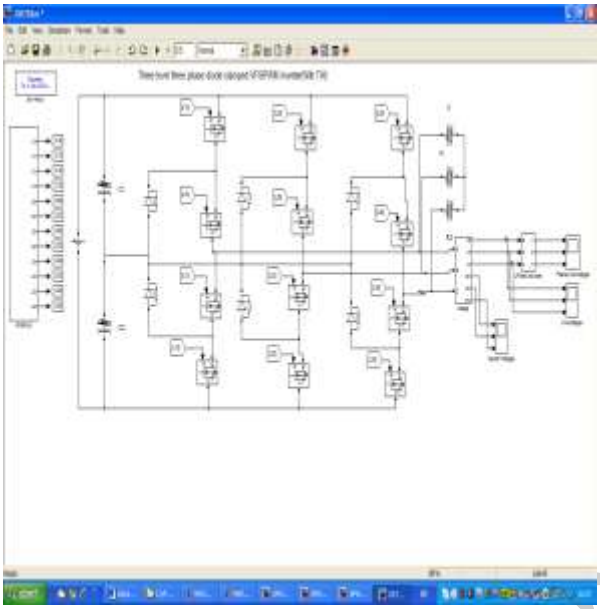

Figure 17 Simulation diagram of THI-ISPWM

Simulink model of ISPWM was shown in the figure 3.7. ISPWM circuit using NPC topology was simulated. The subsystem used to provide the gating pulse to this switch. Powergui was used for FFT analysis for output. Total Harmonic Distortion is computed using power graphics user interface tool.

Gate pulse generation for THI-ISPWM

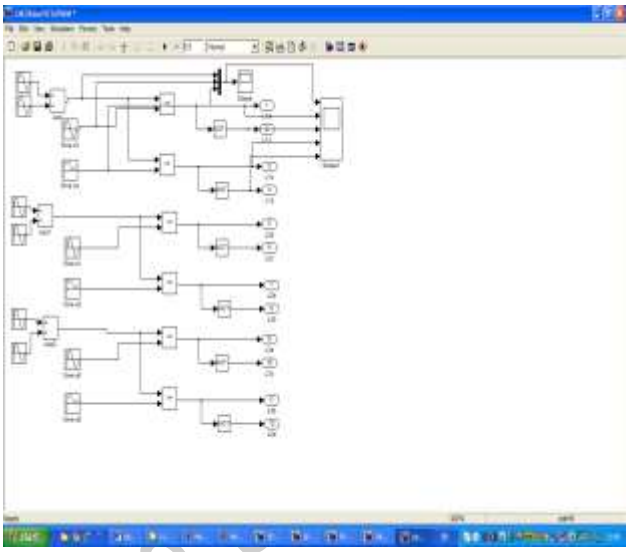

Figure 17 Simulation diagram of gating pulse generation of THI-ISPWM

The reference sine and third harmonic reference sine wave was given to adder. The inverted sine carrier wave and third harmonic injected sine wave was mixed in a comparator. The comparator produces output when amplitude of third harmonic sine wave was greater than amplitude of inverted sine wave. Amplitude of sine wave was 100, third harmonic sine was 100/6 and amplitude of inverted sine carrier wave are 20, 40.

LINE VOLTAGE OUTPUT FOR THI-ISPWM

SEVEN LEVEL OUTPUT

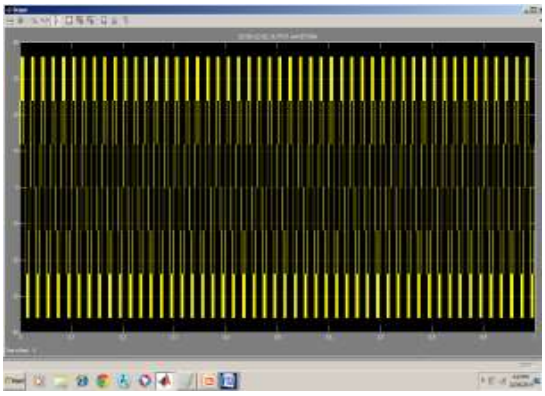

Figure 18 Simulation diagram of seven level output waveform

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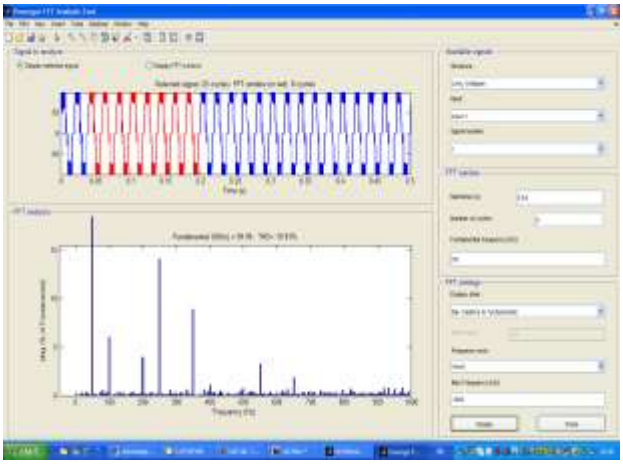

Figure 19 FFT analysis of Line voltage output

From the FFT spectrum analysis THD=19.93, fundamental voltage=99.96v. From THI-ISPWM technique, the stepped Line voltage output are $+v_{dc}$=100v, $+v_{dc}/2$=50v, 0, $-v_{dc}/2$=-50v, $-v_{dc}$=-100v.

3.2 . Simulink model of Seven Level Inverter

SIMULATION RESULTS

The Cascaded-H-Bridge Multilevel Inverter

SCHEMATIC DIAGRAM

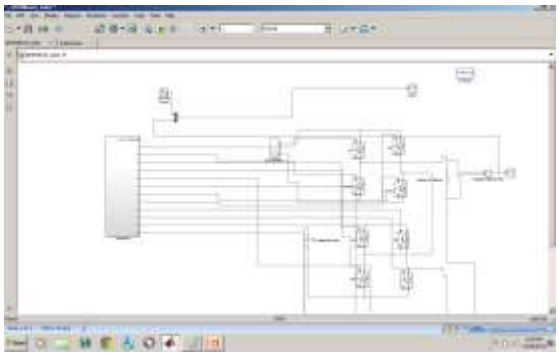

Figure 20 Simulation diagram of CHB inverter

HARMONIC DISTORTION

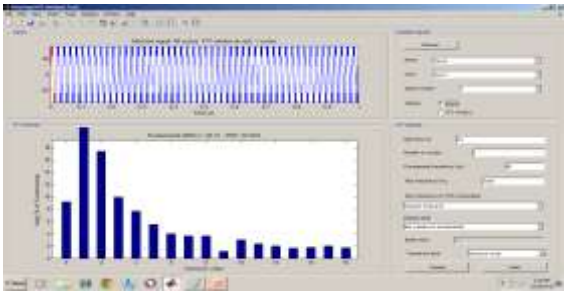

Figure 21 FFT analysis of Line voltage output

SUB SYSTEM MODULE

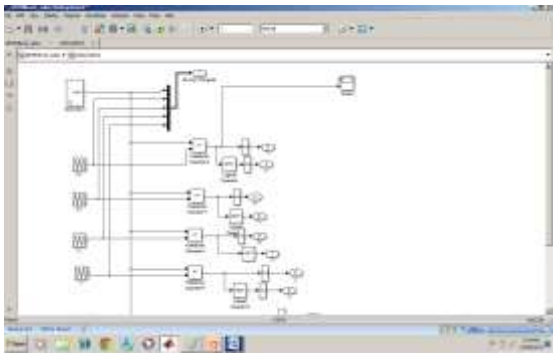

Figure 22 Simulation diagram of gating pulse generation

SOLAR ARRAY SUB MODULE

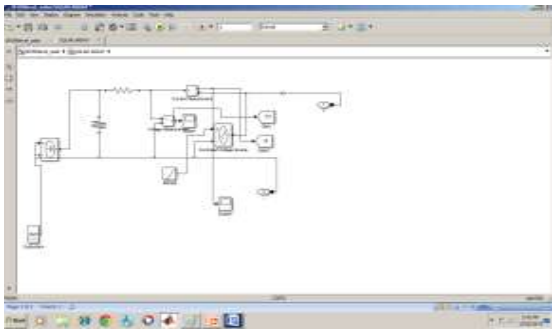

Figure 23 Simulation diagram of solar photo voltaic module

SIMULATION RESULTS
PULSE WIDTH MODULATIONS

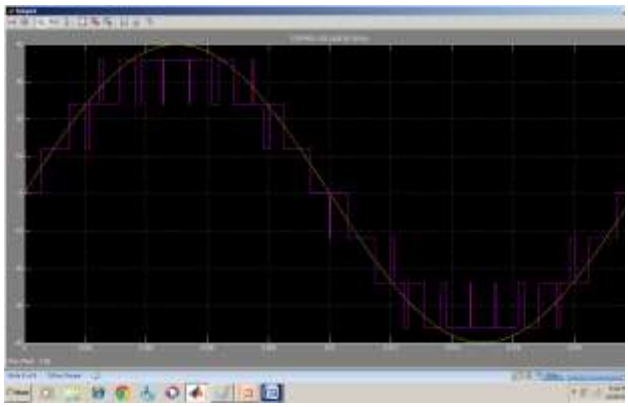

Figure 24 Simulation diagram of pulse width modulation

SIMULATION RESULTS
STEPPED VOLTAGE WAVEFORM

Figure 25 Simulation diagram of stepped voltage waveform

TRIGERRING PULSE

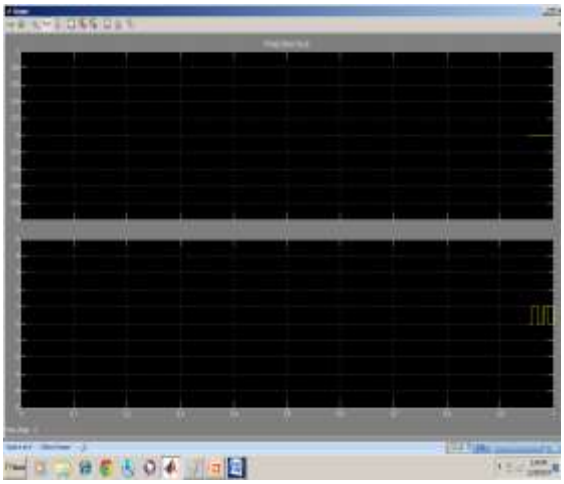

Figure 26 Simulation diagram of triggering pulse

SEVEN LEVEL OUTPUT

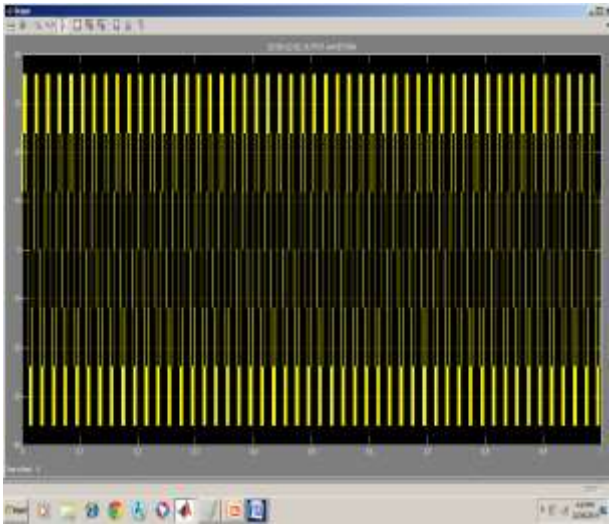

Figure 27 Simulation diagram of seven level output

SEVEN LEVEL CASCADED H-BRIDGES MULTI LEVEL INVERTER FED PHOTO VOLTAIC SYSTEM.

Photo Voltaic System

The solar light energy is converted to electric energy by photovoltaic approach. It takes place with the enrolment of PV, or solar cell. Though solar cell individually has limited output power, for high power applications the structure must be increased by parallel and series integration of solar cells. The cell connected in series may refer as string and the combination of cell in parallel may called group. This integration of solar cell collectively called as Solar PV Module. The elementary component of solar PV module is Solar PV cell. Series and parallel integration of several solar PV cell which are electrically connected to generate the required current and voltage represented as solar PV array. The Fig. 3 shows the equivalent circuit of solar PV module the arrangement is done such that if we require the same voltage as of one cell but if we require high current then the parallel connection to be made.

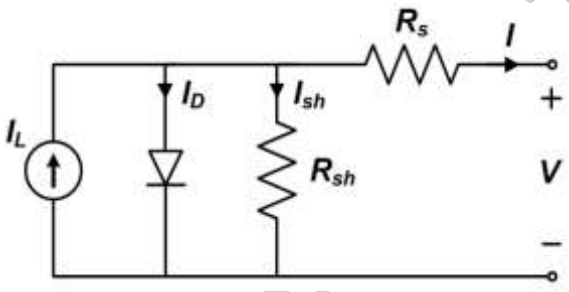

Figure: 28 Equivalent circuit diagram PV system

cascaded H-bridge topology

In proposed system there are three H-bridges are used and all are connected in cascaded manner.
The No. Of H-bridges is determined from Equation (1)

N= (2n+1) (1)
Where,
N= No. of levels in voltage
n= No. of H- bridges.

Each H bridges are single phase inverter circuit having 4 switching devices which may be SCR, MOSFET or IGBT. According to Bridge rule same leg switching devices shouldn't turned ON same time. There are three different DC sources are used to produce 3 level in positive half cycle.

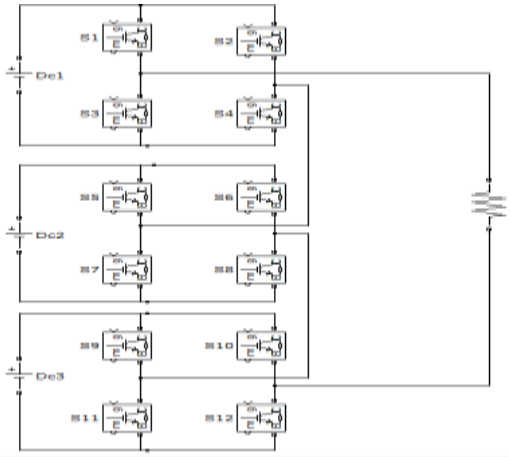

Figure: 29 Proposed 7 level cascaded H-bridge multilevel inverter

The CHB-MLI is simple arrangement of numbers of two-level bridges, whose terminals are connected in series to yield synthesized output waveforms. CHB-MLI requires several independent DC sources. The combinations of the four switches of each cell can able to generate three output voltage level, +Vdc/2, 0 and -Vdcl2 if the input voltage is V de' The overall output is the sum of the individual bridge outputs. Such a proposed system circuit is shown in figure: 4

Table: 8 Switching device on/OFF status for 7 level Voltage

S.no	Voltage	ON Status
1	V1	S1, S4, S7.S8, S11, S12
2	V2	S1, S4, S5.S8, S11, S12
3	V3	S1, S4, S5, S8, S9, S12
4	0	S3, S4, S7, S8, S11, S12
5	-V1	S2, S3, S5, S6, S9, S10
6	-V2	S2, S3, S6, S7, S9, S10
7	-V3	S2, S3, S5, S7.S10, S11

The above table describes the pulse pattern for 7 level voltages.

CONTROLLING METHOD

The advent of the multilevel inverter topology has brought forth various pulse width modulation (PWM) schemes as a means to control the switching of the active devices in each of the multiple voltage levels in the output of an inverter sections. The output voltage is controlled by incorporating pulse width modulation control (PWM control) within the inverters. In this method, a d.c. input voltage which is fixed is supplied to the inverter and a output voltage which is an controlled a.c. is evolved by making adjustments at the on and–off periods. PWM inverters which are voltage type are incorporated in to such fields as power supplies and motor drivers.

The advantages of PWM control are:

- Without any additional components the output voltage control can be evolved.
- The output voltage control eliminates lower order harmonics. The higher order harmonics can be eliminated by filters.

In the Sinusoidal pulse width modulation scheme, the inverter switch is turned on and turned off for stipulated times during every half-cycle, the pulse width is varied to change the output voltage. Harmonics which are lower can be eliminated or reduced by selecting the type of modulation for the pulse widths and the number of pulses per half-cycle. Higher order harmonics increases, they can be eliminated easily by filters. It aims at generating a low-order harmonics eliminated output voltage of inverter. It is acquired when the sampling frequency is high where the fundamental output frequency of the inverter is low.

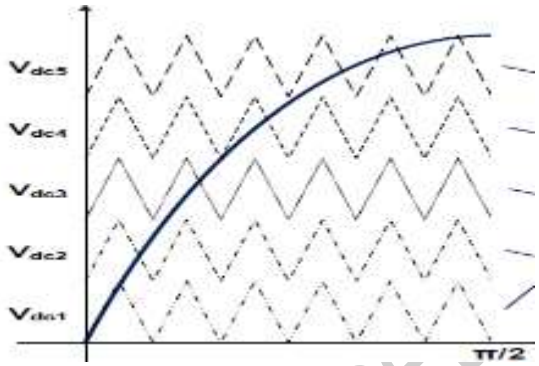

Figure: 30 SPWM techniques.

SIMULATION DESIGN AND RESULT ANALYSIS

MATLAB is a software package for computation in engineering, science, and applied mathematics. It offers a powerful programming language, excellent graphics, and a wide range of expert knowledge. MATLAB is published by and a trademark of The Math Works, Inc the focus in MATLAB is on computation, not mathematics: Symbolic expressions and manipulations are not possible (except through the optional Symbolic Toolbox, a clever interface to maple). All results are not only numerical but inexact, thanks to the rounding errors inherent in computer arithmetic. The limitation to numerical computation can be seen as a drawback, but it's a source of strength too: MATLAB is much preferred to Maple, Mathematical, and the like when it comes to numerics. On the other hand, compared to other numerically oriented languages like C++ and FORTRAN, MATLAB is much easier to use and comes with a huge standard library.1 the un favourable condition is slow speed of execution. This gap is not always as dramatic as popular lore has it, and it can often be narrowed or closed with good MATLAB programming Moreover, one can link other codes into MATLAB, or vice versa, and MATLAB now optionally supports parallel computing. Still, MATLAB is usually not the tool of choice for computing performance. The numerical computation on workstations for non-experts is MATLAB niche. This is one way that tell us to look at the number of MATLAB-related books on mathworks.com. MATLAB remain as an environment which is valuable even for super computer users to

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explore and fine-tune algorithms before more laborious coding in various languages. Computing languages and environments acquire a distinctive character or culture. In MATLAB, that culture contains several elements: an experimental bias, interactive environment and compression of the write-compile-link-execute analyze cycle; an emphasis on syntax that is compact and friendly to the mode which is interactive, also tightly constrained and verbose; a kitchen-sink mentality for providing functionality; and a high degree of openness and transparency (though not to the extent of being open source software). Figure: 6 show the Simulation diagram of PV module. Solar module is created by connecting number of solar cells in series and parallel in order to boost the current and voltage respectively.

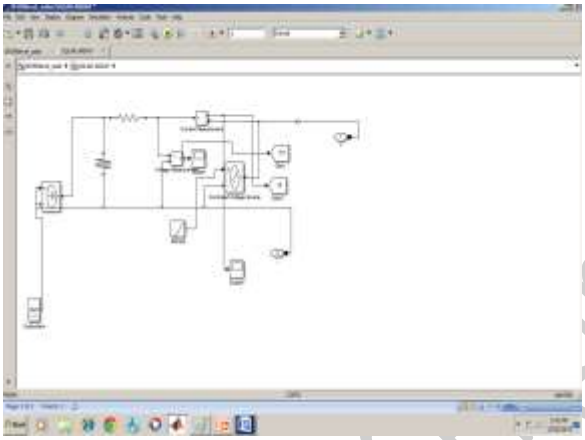

Figure: 31 Simulation diagram of PV module

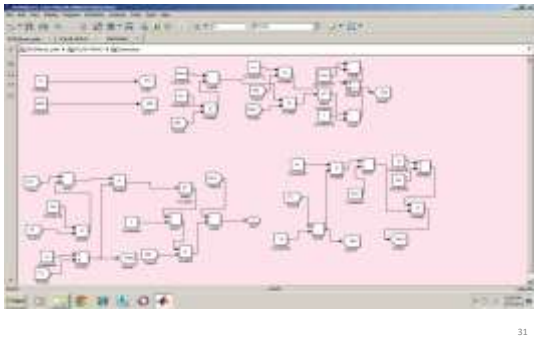

Figure: 32 Simulation diagram of PV sub module

Figure: 8 shows the complete simulation diagram of Cascaded H-bridge 7 level multilevel inverter circuit. Actually, these three H-bridges are developed in Sub system block in order to reduce the complexity of understand. IGBT are used as switching devices, but in hardware MOSFET IRF840 is used because of fewer prices as compared to IGBT.Figure: 10 shows 7 level output voltage waveform which looks like a near sinusoidal voltage. The harmonics content in the proposed system is 19% which is very less compared with 3 level inverters where T.H.D will be 46%. It will result in even more sensors and switches being integrated into vehicle and will further increase the complexity of wiring, cost factor and weight analysis of the complex wiring structure. The harness via wiring is the heaviest, complex, bulky and expensive electrical component in a vehicle and it can contribute up to 50 kg. Given the weight, complexity and cost of the complex wiring harness, it is desirable that other alternatives has to be investigated, such as WSNs. Intra-Vehicle WSNs have the potential to solve this problem but can deliver the same level of performance and reliability offered by wired

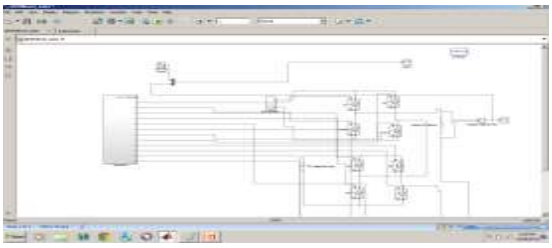

Figure: 33 Simulation diagrams of Proposed C.H-B. 7 level inverter

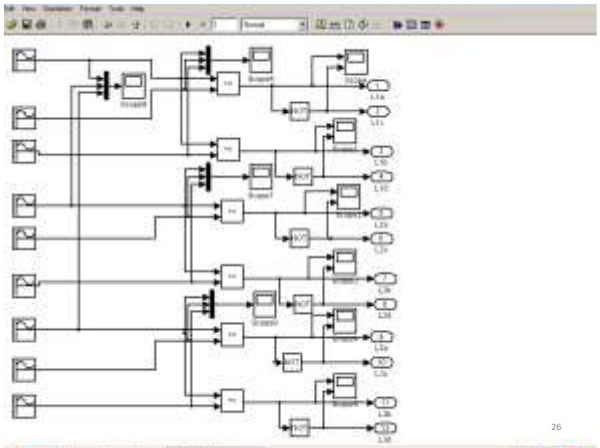

Figure: 34 Schematic of Pulse Width Modulation Scheme

The Figure: 34 depicts the schematic representing pulse width modulation scheme employed to generate triggering signals to control the operations of IGBT switches thus enable us to control the output voltage without the need of any extra hardware requirements. The Figure 11: depicts the stepped voltage waveform of seven level multilevel inverter resembles near sinusoidal waveform.

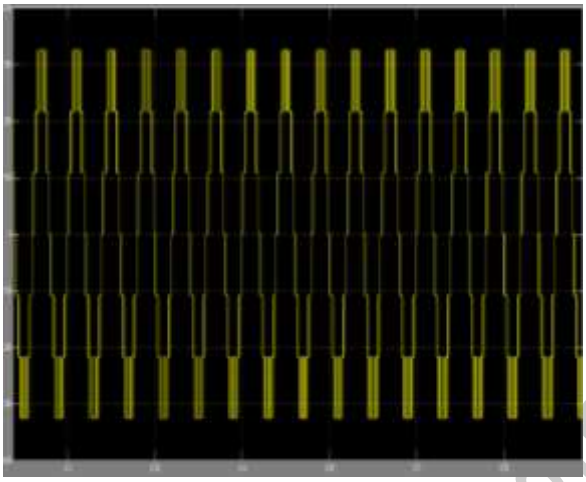

Figure: 35 final output voltage of 7 levels MLI

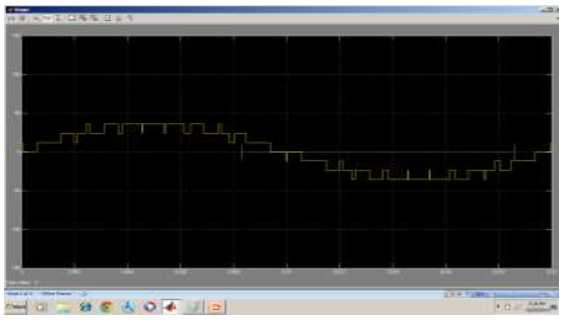

Figure: 36 Stepped voltage waveforms of 7 levels MLI

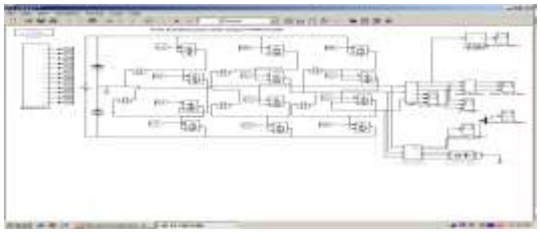

Figure: 37 Schematic diagrams of the Diode Clamped Multilevel Inverter

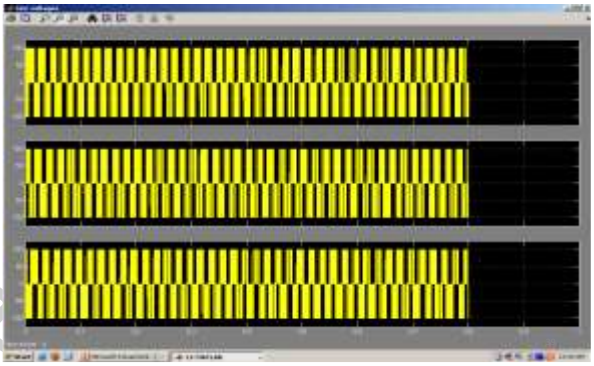

Figure: 38 Line Voltage Output of NPC Inverter

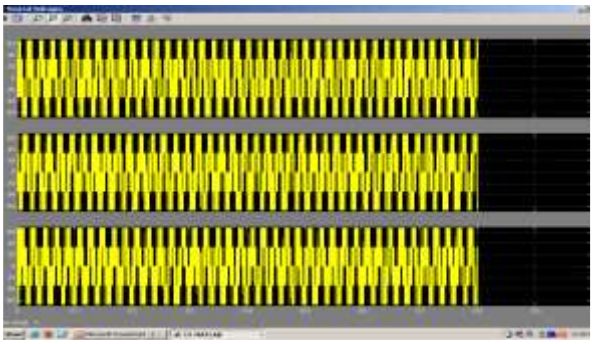

Figure: 39 Phase Voltage Output of NPC Inverter

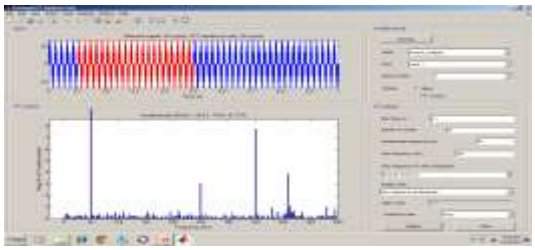

Figure: 40 Harmonic Distortion of NPC inverter

The figure: 15 depict the Harmonic Distortion of Neutral Point Diode Clamped Inverter.

CONCLUSION

The Cascaded-H- Bridge seven level inverters has been simulated in the MATLAB SIMULINK environment. The switching signals were applied at the appropriate switches using multiple sine wave carrier modulation. The switching patterns were studied for different modulation indices. The output voltages and the load currents of the three-phase inverter with inductive and resistive loads were studied. Thus, the reduction in switching losses leads to reduced total harmonic distortion by choosing the modulation index value ranging between 0.5 to 0.9 and the computations prove that the harmonic distortion is reduced up to 32%. The junction of the two capacitors at the source side exhibited a DC level with ripple. The ripple across the capacitors was attributed to the unbalance in the DC voltages across the capacitors and their charge and discharge cycles. There is much scope in the study of balancing the voltage across the capacitors. Thus, the study of the Cascaded-H-Bridge inverter has been carried out and the observations are satisfactory. The project work was educative and opening up new avenues for research. Thus, the new multilevel topology of Cascaded H-Bridge is designed, and results are verified in both simulation and FPGA controller. Various MLI topologies are given detailed manner and T.H.D comparison shows proposed MLI topology gives better results. Moreover, use of FPGA controller in hardware development makes works simpler. The simulated results are listed.

LIST OF REFERENCES

1. A. Tahri, A. Draou and M. Ermis, “A Comparative Study of PWM Control Techniques for Multilevel Cascaded Inverters,” Applied Power Electronics Laboratory, Department of Electrotechnics, University of Sciences and Technology of Oran, BP 1505 El Mnaouar (31000 Oran), ALGERIA.

2. A. Tahri, A. Draou and M. Ermis, “A Comparative Study of PWM Control Techniques for Multilevel Cascaded Inverters,” Applied Power Electronics Laboratory, Department of Electrotechnics, University of Sciences and Technology of Oran, BP 1505 El Mnaouar (31000 Oran), ALGERIA.

3. G. Sinha, T.A.Lipo, “A Four Level Rectifier Inverter System for Drive Applications”, IEEE IAS Annual Meeting 1996, pp 980-987

4. Carrara, Dasani, Gardella, Salutary, “Optimal PWM for the Control of Multilevel Voltage Source Inverter”, Fifth Annual European Conference on Power Electronics, volume 4 ,1993, pp255-259.

5. G. Sundar and S. Ramareddy “Digital simulation of multilevel inverter based statcom “ , Journal of Theoretical and Applied Information Technology ,2005.

6. J.K. Steinke. “Switching Frequency Optimal PWM Control of a Three-Level Inverter”. Proceedings of the 3rd European Conference on Power Applications EPE‟89. Aachen, Germany.1989. pp. 1267-1272.

7. J. Rodriguez, J. S. Lai and F. Z. Peng, “Multilevel Inverters: Survey of Topologies, Controls, and Applications,” IEEE Transactions on Industry Applications, vol. 49, no. 4, Aug. 2002, pp. 724-738.

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