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Analysis of Power, Performance and Area at sub-micron ASIC implementation

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***Abstract* – This paper aims at understanding the existing deep sub-micron and sub-micron implementation of a digital design, analyzing it in terms of power, area and performance (timing) and to come up with solutions and strategies to optimize the design in terms of power, area and timing. An effort was made to comprehend the constraints, causes and the requirements that may result in the existing implementation of the design. Also, various experiments were carried out to enhance the design in various aspects like power, area and timing. Benefits of experiments and tradeoffs required were comparatively analyzed. An effort was made to experiment for optimum solutions and strategies to balance the requirements.**

The key areas stressed upon in this paper are the 28-nm technologies which pose some unique challenges, such as Low-Power Design, Restricted Design Rules, and Design for Yield. Several design examples have been presented, highlighting key techniques employed in the Synopsys® IC Compiler.

***Keywords*– SoC Implementation, Bound Creation method, Data path optimization, Clock path optimization, WNS, TNS**

1. INTRODUCTION

In recent times, semiconductor industry has seen a rise of Very-Deep-Submicron (VDSM) technology. This has added to the pre-existing challenges of System-On Chip (SOC) implementations. The newer technologies have become more complex in design as a result of factors like finer geometries, more features on smaller design size, higher clock frequency and lower voltage consumption. Consequently, interconnect and signal integrity has emerged as major causes of chip failures. Due to sub-threshold leakage, the power dissipation has become uncontrollably large and thus a dominant component of the overall power in a chip.

In the current scenario, designers face various challenges in physical design of multi-million gate chips such as design size, interdependence of design variables, timing closure, clock and power routing, signal integrity, and design sign-off [1][2]. Of these challenges, Timing closure is still the most complex goal. Only accurate modeling and evaluation of propagation delays of Library cells, their placement and interconnect's electrical characteristics can ensure optimum timing closure [3]. A major component of these timing-closure difficulties are Signal integrity (SI) issues. Crosstalk delay and noise are critical at lower geometries and particularly unavoidable below deep sub-micron.

The trade-off between routability, timing and power consumption are the imperative design variable interdependencies. As these are interdependent, so optimization of any one may cause problems with the others. Enormous amount of routing resources are used by Clock and Power networks. Their construction and analysis must be started early and they must be customized for an individual chip's requirements. Clock trees are built after detailed placement is complete. Power networks are frequently predetermined based on statistical or empirical estimates and are built after floor plan is completed. In order to determine whether the requirements are achievable or not physical design plays an important role. Design size has exceeded the limitations of gate-level design tools. It is not possible to design and implement a multi-million gate chip as an indivisible whole. The chip must be planned at a high level, partitioned into smaller pieces, and then completed using lower level tools.

2. TIMING CLOSURE CHALLENGES

Timing closure must be complete before final signoff and tape-out in modern system-on-chip (SOC) implementation. The requirements may vary widely across companies and products for timing closure, along with enablements and paths taken to reach this final state of the IC design. Timing closure is achieved based on effects of various factors like –

whether a part is binned, whether it is in a cost- and/or low power driven market, and many other considerations such as range of functional modes, maturity of target process, lifetime, and maturity of EDA tooling. Timing closure combines (i) years of methodology development, script development, signoff recipe development; (ii) months of block-level and top-level final physical implementation; and (iii) a last set of several hundred manual noise and DRC fixes, along with a final multi-day pass of full-chip signoff analysis and physical verification.

The nature of timing closure has changed as technology is shrinking and our aim must be to implement more design for low power. During low power designing, HVT cells are used and these cells possess properties of high threshold voltage and low leakage power. Due to this, transition time increases and it becomes challenging to achieve the timing closure. Nowadays multi-million gate chips are used in order to increase the functionality in digital design. As the number of gates increase, routing becomes complex and many nets may detour. Detouring of nets adversely affect the timing closure of the design. In deep sub-micron implementation, crosstalk delay and noise are dominating which affects timing closure adversely. Crosstalk delay changes the timing of the design and crosstalk noise changes the functionality of the design.

All anticipated drivers for future growth in semiconductors share one critical requirement: low power. However, low-power design techniques – multiple supply voltages, multiple voltage domains, power and clock gating, DVFS, MTCMOS, multi-Lgate, etc. – increase the timing closure burden by adding complexity to analysis and/or optimization.

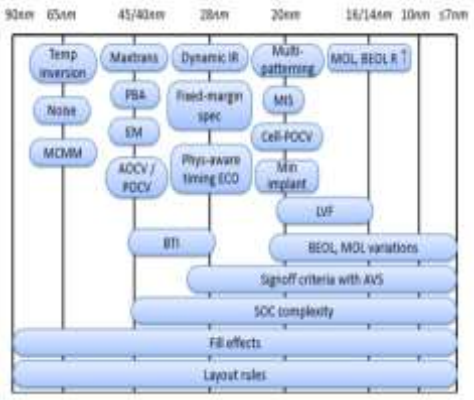

Fig.1. Timing Closure concerns across technologies

As shown in Fig. 1 a sampling of timing closure concerns, mapped against technology nodes. This section samples "what is new" in timing closure. To achieve timing closure, it is important to have balanced use of HVT, SVT and LVT cells and this may also help in optimizing the other parameters, such as area and power. A good floor plan avoid congestion and nets detouring to achieve timing closure. By double spacing between aggressor and victim net and shielding, crosstalk can be avoided.

3. PHYSICAL DESIGN IMPLEMENTATION PROCESS

Physical design process go through many iterations before it arrive at an optimum floorplan. The gate-level netlist (written using a Hardware Description Language) is converted into a physically realizable format (GDSII) which finally becomes the hardware.

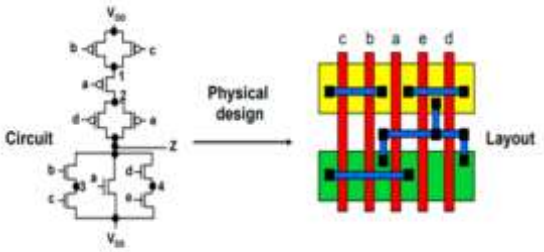

Fig.2. Conversion of a transistor level circuit to a physically realizable layout in physical design

The major steps involved in Physical Design are:

- Importing Inputs
- Floorplanning & Partitioning
- Power Planning
- Placement
- Clock Tree Synthesis (CTS)
- Routing

The final output of a frontend design or circuit (logic) design is a gate-level netlist has an extension .v or .vhdl that contains the logical functionality of chip. This netlist has information of plenty of instances (standard cells, macros, I/O pads etc.,) with interconnections (nets) between them based on the functionality of design which will be implemented.

3.1. FLOOR PLANNING

This is the first major step in to get the layout done, and is the most important step which determines the chip quality. At this step, one defines the size of the chip/block (estimation of die dimensions) pin placement and macro placement, allocates power routing resources and creates or decides space for standard cell placement. Apart from all these we also place few special cells such as decoupling capacitors, welltap cells and endcap cells. Decap cells are placed to provide power to power domains when a deficiency in power arrives. Well tap cells are placed to avoid latch up conditions.

Fig.3. Back-end Design Flow

3.2. POWER PLANNING

Power planning is generally done in conjugation with the floorplanning itself and the main intention of this stage is to provide power rings and straps to our current design. The topmost layer is usually chosen to build the power distribution network as the resistance of the top most layer is the least and hence will result in the least IR drop at the later stages. With the advancement in technology power rings are rarely used to deliver power to the chip. Fig. 4 shows a typical power planning for a chip. There are two types of power planning and management. They are core cell power management and I/O cell power management.

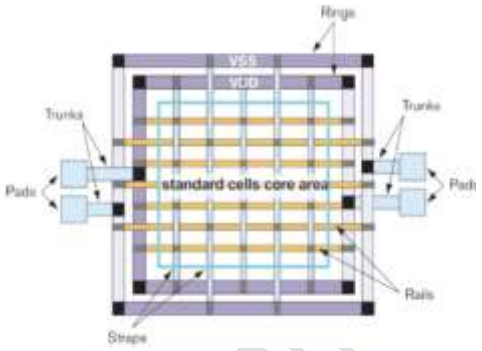

Fig.4. Power Planning

VDD and VSS power rings are formed around the core and macros in core cell power management. As per the power requirement straps and trunks are created for macros. Power rings are formed for I/O cells and trunks are constructed between core power ring and power pads in I/O cell power management. The power information can be obtained from the front end design. The synthesis tool reports static power information. Dynamic power can be calculated using Value Change Dump (VCD) or Switching Activity Interchange Format (SAIF) file.

3.3. PLACEMENT

Placement is the process of placing standard cells in the rows created at floorplanning stage. It is the stage which will define the chip performance and will also decide the routing ability of the tool that is how well the tool will perform the routing of the design. Apart from placing standard cells, global routing is also performed during placement. Also the tool performs high fanout net synthesis and legalize placement to avoid DRCs. Apart from what tool does, power optimization also needs to be performed in terms of dynamic power and static power. Then IR drop analysis is performed after placement.

3.4. CLOCK TREE SYNTHESIS

At this stage, clock is provided to sequential elements which is achieved by various clock tree algorithms. Apart from providing the clock tree to proposed design, clock tree optimization for balancing the skew and power optimization on clock network are performed. Clock networks are the

largest power consumers and hence need to be optimized. One of the famous clock tree algorithms is shown in Fig.5.

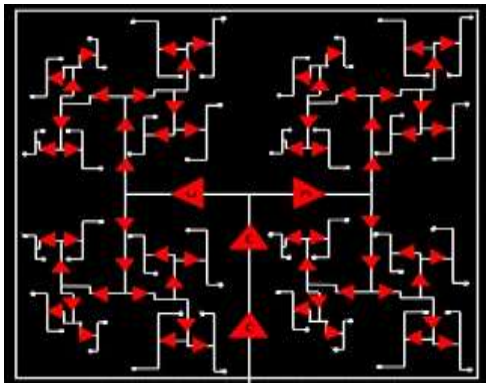

Fig.5. H-Tree Structure

3.5. ROUTING

After placement and CTS routing process determines the paths for nets on the chip layout to interconnect the pins on the circuit blocks or pads at the chip boundary. These precise paths of nets must satisfy the design rules provided by chip foundries to ensure that the designs can be correctly manufactured. The most important objective of routing is to complete all the required connections (i.e., to achieve 100% routability); otherwise, the chip would not function well and may even fail. Other objectives, such as reducing the routing wire length and ensuring each net to satisfy its required timing budget, have become essential for modern chip design. Fig. 6 shows orientation of different metal layers.

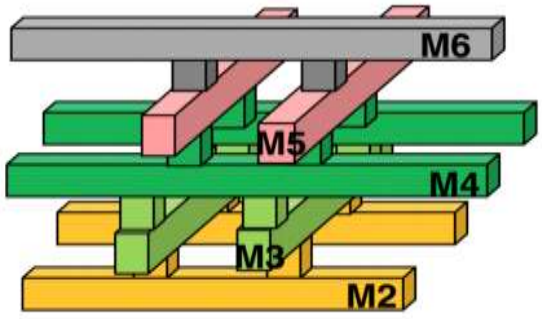

Fig.6. Orientation of different metal layers

4. EXPERIMENTS AND ANALYSIS

In order to perform timing analysis and establish the correlation between timing, area and power, continuous design iterations must be undertaken. The violations coming out of these iterations must be fixed such that other violations are also optimized for closing timing of the design. In this section, firstly, the experimental setup used for performance analysis has been presented. This is followed by the various experiments performed and the results observed – obtained at each stage, the best iterations and worst iterations using different techniques which have been evaluated and finally correlation between power, area and timing has been established.

4.1. EXPERIMENTAL SETUP

The SoC design is partitioned at the block level. The P&R flow has been performed on only one block. The design specifications of the simulation block used for experimental analysis are as following:

a) 28 nm technology implementation
b) 75 MHz clock frequency and 13.33 ns Clock Period
c) Voltage 0.81 V
d) Number of metal layers are 10 (M1-M9)
e) Gate count of the design is 234830
f) Number of macros is 6
g) 928 Input / Output ports
h) Area used for block implementation is 1.498 mm^2
i) EDA tool used for the block implementation is Synopsys® Integrated Chip Compiler (ICC) tool.

The execution flow begins with Initialization of the design block, followed by Floorplanning, Placement, CTS and Routing stage. After completion of each stage, the parameters of Time, Area and Power were compared. Violating points for timing (setup and hold), congestion, and DRC were identified. The better performing iteration was then used for further evaluation.

4.2. DESIGN SUMMERY

At the Floorplanning stage, multiple iterations have been created using different floorplan techniques such as Fly Line analysis, Data Flow Analysis (DFA), All Fan_in and All Fan_out techniques. The first Iteration was created using the Fly Line analysis as shown in figure 7(a). This allowed for observation of connections of macro with other macros, standard cells and I/O parts of the basic block design.

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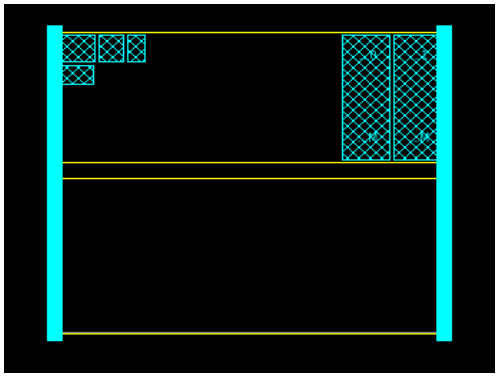

Fig.7 (a). Iteration-1 Block created using Fly Line analysis technique at Floorplan stage

This allowed for observation of connections of macro with other macros, standard cells and I/O parts of the basic block design. On this iteration of design block, the entire P&R flow was executed. To solve the timing violations thus observed, the floorplan was changed in Iteration-2 as shown in Fig. 7(b).

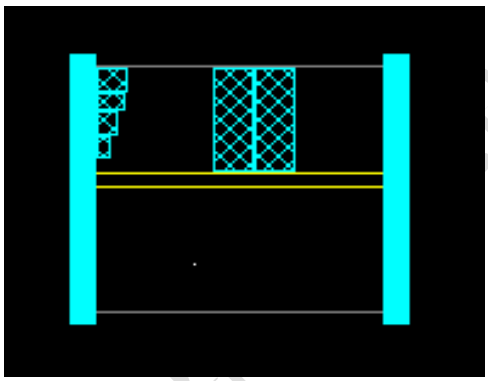

Fig.7 (b). Iteration-2 Block design changed at Floorplan stage

The third iteration, as shown in Fig. 7(c), was performed using DFA where the top module connection of block can be now seen. After evaluating Iteration-2 and Iteration-3 at Placement stage, the timing violations were observed and compared with area (congestion) and power. It was noted that Iteration-3 provided least timing violations among the three. Therefore, Iteration-3 was used for further evaluations and analysis. These intermediary results provide us our basic design specifications for the block as summarized in Table I.

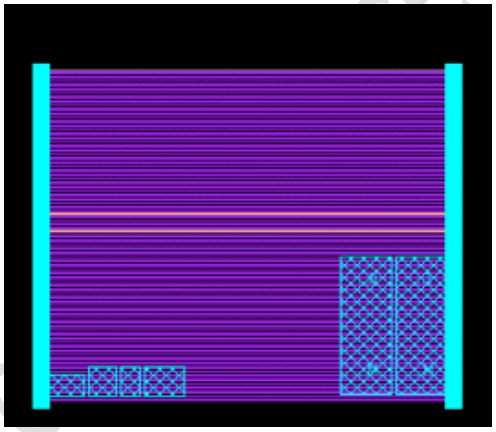

Fig.7(c). Iteration-3 Block created using DFA

As it can be seen in Table I tabulating the Timing Report after floorplan of the different experiments, experiments 1, 2, 3, and 4 have almost same results. It can be noted that the setup and hold Worst Negative Slack (WNS) and Total Negative Slack (TNS) are same. When the standard cells are introduced in the placement stage, difference in WNS and TNS can be observed.

Shown in Table II, there is a setup violation in the placement timing reports of the three iterations 1, 2, and 3. On comparing these iterations with the placement timing reports as a basis, it can be noted that Iteration-3 has the least violations while Iteration-2 has the worst violations.

TABLE I. Timing Report at Floorplan stage

Parameter	EX.1	EX.2	EX.3	EX.4
Setup WNS (ns)	-0.55	-0.55	-0.55	-0.55
Setup TNS (ns)	-2552.29	-2552.29	-2552.29	-2552.29
No. of violating Paths	8228	8228	8228	8228
Hold WNS (ns)	-0.17	-0.17	-0.17	-0.17
Hold TNS (ns)	-12.30	-12.30	-12.30	-12.30
No. of violating Paths	97	97	97	97

TABLE II. Placement QOR/Timing Report

Parameter	EX.1	EX.2	EX.3	EX.4	EX.5
Setup WNS (ns)	-0.42	-0.39	-0.36	-0.14	-0.34
Setup TNS (ns)	-2474.70	-2633.94	-2400.32	-552.45	-627.59
No. of violating Paths	9246	8646	8957	6950	3958
Hold WNS (ns)	-0.14	-0.13	-0.12	-0.12	-0.13
Hold TNS (ns)	-450.71	-874.42	-426.81	-451.92	-255.81
No. of violating Paths	24319	21725	19792	21569	18007
DRV	6	5	6	1	3

After placement stage, when checking the Placement QOR reports, the type of violations being faced by the block can be evaluated. If the block faces a congestion violation, a congestion-driven placement strategy is adopted. In case of timing violations, usually a timing-driven placement strategy is adopted. However, since the objective of this paper is to present a replacement strategy for timing-driven placement, two placement techniques were tested at the placement stage as alternatives.

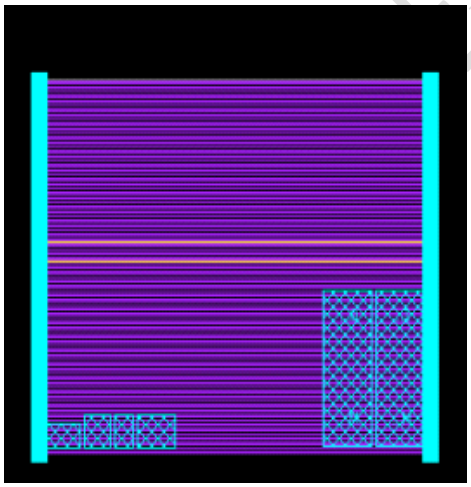

Fig.9 (a). Iteration-4 (Block created using Bound Creation technique at Placement stage)

Iteration-4, as shown in Fig. 9(a), was created using Bound creation technique. Since some cells belonging to the top violating paths were scattered and had the same hierarchy, a bound was created for that near to the end point, as shown in Fig. 9(b).

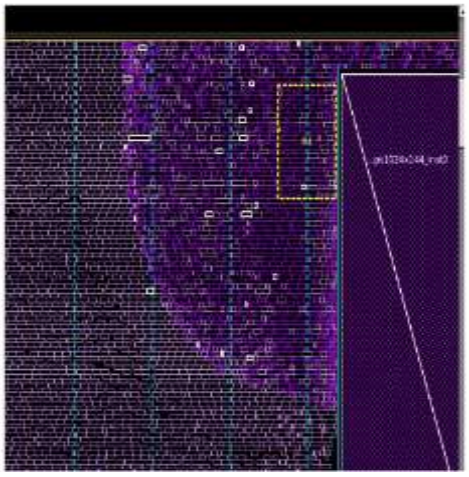

Fig.9 (b). Bound Creation

Another experiment (EX.5) was conducted by applying Magnet Placement technique to Iteration-3. As evident from Table II, the setup WNS for EX.5 was noted to decrease from -360 ps to -320 ps. However, it is not a significant reduction. It can also be seen that setup violation becomes worst compared to bounding technique (EX.4) where the setup WNS reduces drastically from -360 ps to -140 ps. Also to be noted is that with Bounding technique, the number of violating paths reduced and so did the setup TNS. The DRVs are also reduced to 1 from 6. The timing reports are as tabulated in Table III for CTS stage. Table IV details timing reports after Routing. For further analysis, only EX.1, 3 and 4 were considered for complete P&R flow. During the CTS stage, data path optimization technique was applied.

TABLE III. CTS QOR/Timing Report

Parameter	EX.1	EX.3	EX.4
Setup WNS (ns)	-0.39	-0.33	-0.19
Setup TNS (ns)	-398.76	-330.62	-103.95
No. of violating Paths	4562	3394	2481
Hold WNS (ns)	-0.06	-0.06	-0.01
Hold TNS (ns)	-458.02	-442.47	-1.53
No. of violating Paths	24863	23667	1363
DRV	11	3	19

TABLE IV. Routing QOR/Timing Report

Parameter	EX.1	EX.3	EX.4
Setup WNS (ns)	-0.42	-0.30	-0.17
Setup TNS (ns)	-496.65	-328.65	-67.84
No. of violating Paths	3115	3255	1067
Hold WNS (ns)	-0.08	-0.05	-0.03
Hold TNS (ns)	-381.26	-120.60	-0.41
No. of violating Paths	21895	7012	187
DRV	468	506	374

As shown in table VI, the three parameters Power, Area and Timing are compared for all three experiments at routing stage. Different techniques have been used for different experiments. As we can see in Ex-1 Power is very less as compared to Ex-3 and 4 but at the cost of Timing (highest setup violation -420 ps). In Ex-4 where I have used Data path optimization technique the Timing improves drastically from -420 ps to -170 ps and also Power and Area reduced by some amount. It means the block has very less setup violation and at the same time Power and Area are also decreased significantly.

As in VLSI there is always tradeoff between these three parameters. Therefore we have to see which parameter is more important for our design and according to that we have to choose best strategies and results for the design.

4.3. COMPARISION OF POWER, AREA AND TIMING

Comparison of Power, Area and timing is tabulated as Table V for the routing stage.

TABLE V. Comparison of Power, Area and Timing

Experiments	Power (mW)	Area (um^2)	Timing (ns)			
			SETUP		HOLD	
			WNS	TNS	WNS	TNS
Ex. 1	171.69	760785.71	-0.42	-496.65	-0.08	-381.26
Ex. 3	182.12	747785.72	-0.30	-328.65	-0.05	-120.60

Ex. 4	178.33	761660.34	-0.17	-67.84	-0.03	-0.41
Ex. 5	173.91	743526.41	0.01	0.00	-0.16	-263.152

It can be seen in Ex-1 Power is very less as compared to Ex-3 and 4 but at the cost of Timing (highest setup violation -420 ps). Data path optimization technique has been used in Ex.-4 and the Timing improves drastically from -420 ps to -170 ps and also Power and Area reduced by some amount. It means the block has very less setup violation and at the same time Power and Area are also decreased significantly. As in VLSI there is always tradeoff between these three parameters.
Therefore we have to see which parameter is more important for our design and according to that we have to choose best strategies and results for the design.

5. CONCLUSION

Assessing the different experiments conducted, it can be inferred that the physical implementation in VLSI is beyond doubt a balancing act of various parameters. Working with low-power design, design rules and designing for yield are bound by many constraints. As witnessed in the experiments, when leakage power is reduced it is often at the cost of timing. In certain cases while the power and timing are optimized, area may cause concerns.

Therefore, very careful planning and envisioning of the impact on every parameter is required before a strategy can be chosen and implemented. Using different strategies and optimization techniques, the same design could be implemented in varied ways. They could either result in the reduced power consumption, or swift operations, or would have the minimum footprint. The challenge thus lies in meeting the specifics for all the parameters while accommodating the constraints of the design and yet making it the most optimized design.

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