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Comparative Implementation and Analysis AFE Cardiac Amplifier for Bio-Signal Recording System (ECG)

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Abstract- **This paper is focused on comparative analysis and implementation of cardiac front end amplifier, In order to achieve highly refined signal quality, low noise and low power consumption, the proper architecture of AFE instrumentation amplifier plays vital role. The cardiac recording system overall performance is determined by front end amplifier, it senses the weak bio-potential cardiac signals which ranges in micro to milli-volts and results in amplification meanwhile maintaining signal quality with minimal contamination of signal with noise. The paper reflects the comparative design and analysis of two different architecture mentioned as Current reused based stacked inverter-4 and Current reused based folded cascode amplifier with mid rail current sink/source (MCS) both are implemented in 180nm technology. The performance analysis of both amplifiers is determined by various predominant parameters like gain, power, and supply voltage, IRN, CMRR and PSRR. On basis of simulation, comparative analysis of both topologies result that the current reuse based stacked inverter-4 proves to well suited AFE for cardiac recording system, gain is 49.57dB operated at 1V supply voltage, CMRR is 85.29dB, noise is 150uV/√Hz @300Hz and the power consumption obtained is 1.89x10^-11W.**

Keywords- **BMI (Bio-Medical interface), MCS (Mid Rail Current Source), Current Reuse, Stacked Inverter, IRN (Input Referred Noise), Weak Signal, Low Voltage, ECG and Bio-inspired.**

1. INTRODUCTION

A drastic change is observed in field of health care equipments. In modernized clinical practices, Electro-cardiography (ECG) is responsible for continuous monitoring of heart beats. By placing electrodes on chest of patient, a non-invasive medical procedure is implemented in regard to monitor the cardiac electrical signals known as ECGs. Electrical activity is generated due to polarization of one portion of heart and depolarization of another portion, results in electrical signal which is captured and recorded.[1]

This time domain cardiac potentials are responsible to indicate electro-mechanicals heart muscle's activity like as rhythmic action of heart chambers size and position, damage of heart muscles.

The information carried by ECG signal in regard to heart's information, is responsible for proper diagnosis of cardiac arrest, fainting, pulmonary embolism and collapse. [2]

Continuous monitoring of bio-potential signal, analyzing and recording is considered as important part of clinical practices. Under such practices patients are interfaced with cumbersome bio-potential recording devices for the purpose of diagnosis of ailments, which is responsible for discomfort and mobility of patient as a result signal acquisition time is, reduced which prevents proper diagnosis of heart ailments.[3]

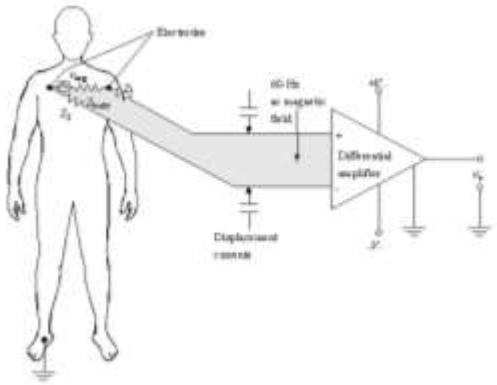

Fig 1: ECG Recording Block Diagram [1]

As a result, there has been drastic demand for miniaturized bio-potentials acquisition devices characterized with low noise, ultra low power consumption, high CMRR and high gain which has necessitated the wide research in architectures of such interfaces, which inspired to design miniature bio-potential recording system.

In order to achieve high signal quality, low noise and low power consumption, the design of analog front end instrumentation amplifier plays vital role. Since, the overall performance of recording system, overall noise as well amplification of low voltage cardiac signal and output of the sensor readout circuitry is defined by design of front end instrumentation amplifier.[5]

The amplitude of cardiac signal ranges from few micro-volts to few milli-volts as result the cardiac signal at the first stage is very weak, in order to analyze the signal parameters properly, a proper architectural design of instrumentation amplifier is needed which is capable enough to boost the amplitude of weak cardiac signal, being a weak signal it's obvious of the signal being corrupted by noise and as result proper diagnose of ailment will get failed as result rejection of noise required as well as common mode voltage.

As a result, in the field of bio-signal processing microelectronics plays a vital role in field of healthcare industry like as battery operated portable healthcare equipments, which causes need of low voltage power supplies in CMOS circuit applications meanwhile not compromising with the power consumption. [7]

There is demand of more and more advancement in the application circuitry required to record the ultra-low amplitude cardiac signal for measurement module. Interfacing circuitry at the first stage of recording system posses the stringent constraints for the measurement of weak signals as a result monitoring of bio-potentials has become an interesting topic, since it carries health information which plays a vital role in diagnosing the cardiac related ailments used by practitioners to combat the diseases. The overall performance of signal acquisition or signal recording system can be enhanced by simply improving first stage, which comprises of instrumentation amplifier or LNA which picks the weak bio-potential and forward it to the succeeding stages.[10]

2. DESIGN CONSIDERATION AND TECHNIQUES FOR CARDIAC FRONT END AMPLIFIER

A. Characteristics of Cardiac Amplifier

As cardiac signal lies within the range of micro to milli volts, amplifier must be capable enough to extract the weak bio-potential for which the, input impedance of amplifier should be high for cardiac signal in order to transfer the cardiac signal faithfully without any attenuation. The equivalent skin electrode interface may be high enough within the bandwidth. CMRR should be high enough to reject common mode interference, Mostly it is observed that the fully differential amplifier mismatching causes degradation in CMRR. High pass filtering requirements must be satisfied to lower down the differential electrode offset effect. Amplifier, operation of CMOS in weak and moderate inversion region proves to be suitable for low power designs, In order to achieve the longer term battery life power dissipation. PSRR must be high, the cardiac signals extracted are weak in turn posses low amplitude such variations in supply voltage must be eliminated for proper amplification. NEF should be optimized for the circuit to become more efficient as a result with low input referred noise, circuit consumes less amount of power.

B. Design Challenges of Cardiac Amplifier

Bio-signal is acquired, amplified by instrumentation amplifier and obtained signal is recorded with small

content of noise and interference as a result signal can be processed by the subsequent blocks. Amplitude level of cardiac signal ranges from 0.1mV to 5mV and have very low frequency. Due to such nature of signal it is dominated with flicker noise (1/f) of MOS transistors due to which detectable signal get failed to properly analyze.

Another problem is DC offset which is generated at skin electrode interface, although poor input DC offset is showcased by MOS. There exist common mode interference exist due to 60Hz get coupled with ECG signal even get significant in the wired system.

C. Introduction to Nature of Cardiac Signals

Electrodes are attached to the surface of chest skin, due to polarization and depolarization of cardiac muscles, electrical activity is produced and recorded. A typical ECG recording of the cardiac cycle (heartbeat) consists of a P wave, a QRS complex, and a T illustrated in figure 2.

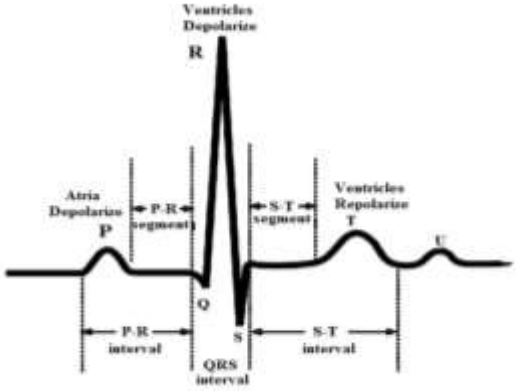

Fig 2. ECG Graph showing various segments [3]

The voltage range of typical ECG signal lies in range between the micro-volts to several mV when the signal is measured with wet electrodes, artifacts motion is up to 10mV. Heart rate and heartbeats regularity can be measured by ECG waveform, as well position and size of chambers, presence of any damage to heart and presence drugs or device effects used to regulate heart.

Wide range of disease is interpreted by the ECG waves such as seizures, pulmonary embolism, cardiac murmurs, myocardial infarction and perceived cardiac dysrhythmias.

D. Noise Consideration in Op-amp

The AFE bio-signal amplifiers suffer from three major sources which are Thermal and flicker noise obtained from the amplifier circuit by itself, Electromagnetic and electrostatic signals coupled through cable and human body as well Electrode Noise.

Noise coupled through the cable can be minimized by using shorter length of cable. The coupling of noise to human body can also be diminished by approaching high CMRR. Some noise is also generated by the electrode impedance which corrupts the signal to be detected. The type electrode used in detection the signal, its chemical make and surface of the human body is responsible to determine the impedance and as a result noise voltage is produced.

Thermal noise and flicker is considered to be originated from the circuit itself which is important limiting factor.

In bio-potential amplifiers is to raise the noise efficiency which quantifies the power efficiency in terms of noise.

With the lower value of NEF the amplifier is capable to achieve low power dissipation.

E. Concept of Current Reuse Technique

The idea behind using current reuse technique is without increasing the bias current I_D, to boost the overall trans-conductance of the amplifier. The design technique involves in biasing the MOS in such a way to drive MOS in weak inversion region to maximize the g_m/I_D. There exist a vice versa relationship in which, power can be reduced for same noise or for same power amplifier noise can be reduced. These two parameter scenarios are interchangeable.

In order to increase the trans-conductance g_m , the input pair of PMOS can be stacked on the on to the NMOS input pair in order to obtain inverter based input stage, as result of the setup the overall amplifier g_m get doubled but without any need of extra biasing current, since it shared by both of the pairs. With vertical stacking of N number of inverters, 2N time current can be reused by single input channel. Current reuse can be achieved by more times simply by vertically stacking the inverted based amplifiers, this way 4 times the bias current is reused and thus g_m is boosted by four times.

F. Concept of Mid Rail Current Sink/Source (MCS)

The noise of the acquisition system is defined by the front end amplifier, the current reuse among different channels is enabled by mid rail current sink/source in order to obtain the power efficient front end system with the application of single voltage supply.

It is known that the input stage of recording system with AFE (Analog Front End) amplifier generates the low output swing as result it aggressively reduces the supply voltage, so amplifier is stacked between the rails which enables current reuse.

The sources of NMOS and PMOS are connected to form MCS as shown in figure 3. Biasing branches provides the gate voltage to the MOS. Circuit comprises of MOS are basically driven in weak inversion region as well in order to confirm that MOS are operated in saturation region V_{DS} for the NMOS and PMOS should four times more than the thermal voltage.

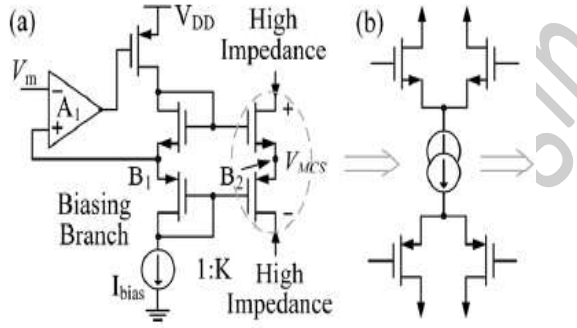

Fig 3. a). Circuit for mid-rail current sink/source (b).Connection for two differential pairs[5]

3. CIRCUIT IMPLEMENTATION OF PROPOSED CARDIAC FRONT END AMPLIFIER

A. Implementation of Current Reuse Technique Based Stacked Inverter-4 Amplifier

In this proposed design of amplifier, four stage stacked inverter design is based upon stacking of inverters tend to share the same bias current. The common gates braches originating from the stacked amplifiers tends to aggregate the current signal from all the eight pairs. Thus the overall trans-conductance of the circuit obtained is $8g_m$. The approach behind designing of this amplifier is to embed it in between the capacitive feedback loop.

The input pairs are separated such that they can be biased at different voltage levels. There are total eight input pairs, as result this is known as stacked amplifier version-4. The circuit shown in figure 4.1 employs eight common gate transistors which are PMOS_ (8/10), NMOS_ (8/12), PMOS_(9/11) and NMOS_(9/13) in order to aggregate the signal obtained from the input pairs.

Small signal behavior can be analyzed, such that the total trans-conductance g_{mt} of the amplifier can be given by equation 1.

$$g_{mt} = \frac{gm}{ID} (4I_D + 4I_D) \sim 8g_m \quad \ldots\ldots\ldots\ldots\ldots\ldots (1)$$

I_D is the input bias current of the transistor; it is assumed that all the transistors have identical g_m/I_D and the intrinsic gain is shown by $g_m r_o$ for all the MOS in circuit is greater than 1.

The open loop gain DM, A_{DM} is given by equation 2.

$$A_{DM} = g_{mt} r_{ot} \quad \ldots\ldots\ldots\ldots\ldots\ldots (2)$$

The differential mode gain (DM) is the square of the intrinsic gain, which can be compared to telescopic or folded cascode amplifier. The amplifier is the combination of folded cascode amplifier and telescopic amplifier. If lower end of amplifier is considered NMOS_10 and NMOS_11 and rest of the inputs are dc biased then amplifier overall structure behave like same as telescopic amplifier and if we consider the lower end PMOS circuit input pair PMOS_12 and PMOS_13, its input and output relationship is similar to the folded cascode amplifier topology. The same consideration will be considered for the upper pair of the MOS transistors.

The amplifier input referred 1/f noise can be given by the equation 3.

$$N_{PSD} = \frac{K_f}{C_{ox} \cdot 4 W L} \cdot \frac{1}{f} \quad \ldots\ldots\ldots\ldots\ldots\ldots (3)$$

K_f is considered as process dependent parameter, W and L are the width and length of the transistor, 1/f noise associated with the circuit can be minimized by increasing the size of the input transistor, as result in band noise will be dominated by thermal noise.

The CMRR of the circuit topology can be calculated, as CM input is applied and output DM is derived in the presence of mismatch can be given by the equation 4.

$$\textbf{CMRR} = \frac{A_{DM}}{A_{CM-DM}} \quad \text{..... (4)}$$

In above mentioned equation 4, $A_{CM\text{-}DM}$ expresses the CM to DM gain. The PSRR of the circuit can be illustrated by the equation 5.

$$\textbf{PSRR} = \frac{A_{DM}}{A_{VDD-DM}} \quad \text{..... (5)}$$

A_{VDD-DM} denotes the voltage gain from V_{DD} to V_{DM}. In order to minimize the requirement of supply voltage the dc bias voltage tends to be different. The lower end of the NMOS and PMOS pairs of circuit are quite simple to bias, in case if small deviation does exist causes minimal influence on operation of amplifier. PMOS (8/10) ,NMOS(8/12),PMOS(9/11) and NMOS(9/13) is responsible to form cascode transistors which is responsible to provide low impedance node at the drain of MOS pairs can be given as PMOS_2,NMOS_1;PMOS_3,NMOS_2;PMOS_4,NMOS_3;PMOS_5,NMOS_4;PMOS_6,NMOS_5;PMOS_7,NMOS_6 , PMOS_12,NMOS_10 and PMOS_13,NMOS_11. The current induced due to the mismatches between the bias and input transistors tends to flow in the CG transistors.

The circuit of current reuse based inverter stacking amplifier is implemented using 0.18µm technology, from the obtained simulation it can be observed that only 2mV of weak input cardiac signal is applied to the input stage of amplifier which result in large output voltage swing which is 603mV at the output node, the resulting amplified signal will further be processed by the signal conditioning circuitry. The circuit is operated at the supply voltage of 1V.

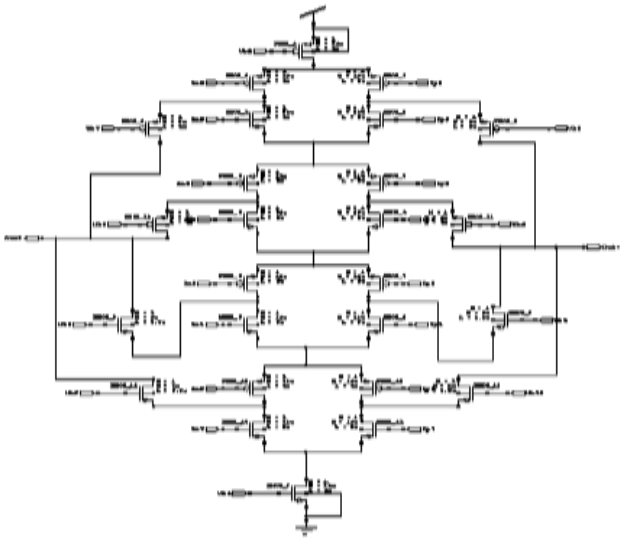

Fig 4: Schematic Implementation using Current Reuse Technique based Inverter Based Stacked Amplifier

The dc response is shown in the figure 5, The AC response plot is illustrated in figure 6 and Noise analysis is shown in figure 7, in which magnitude of input noise (inoise), output noise (onoise) and total noise (totnoise) is represented.

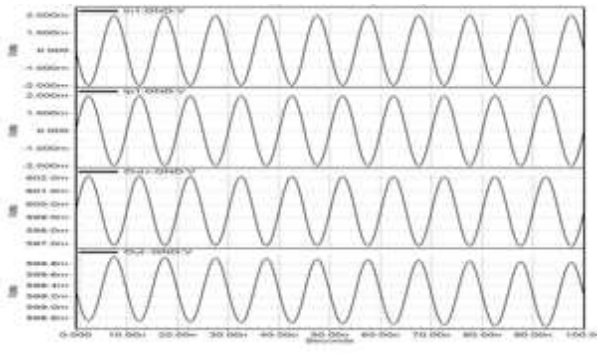

Fig 5: Simulation Waveform Current Reuse technique based Stacked Inverter Amplifier

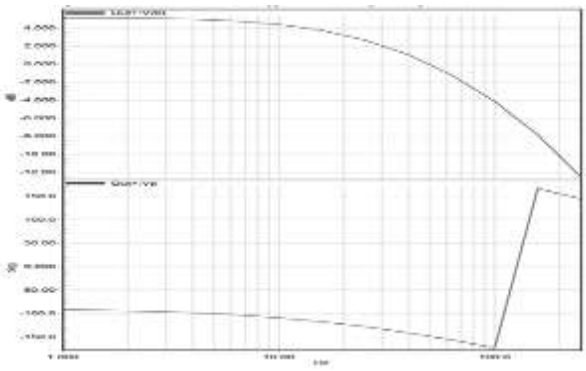

Fig 6: AC response of Op-amp (a).Magnitude Response (dB) (b).Phase Response (Deg)

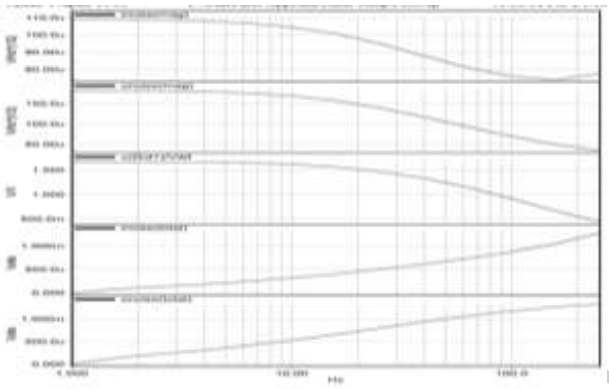

Fig7: Noise Analysis Response of Inverted Stacked Amplifier (Using Current Reuse Technique)

B. Design of Folded Cascode Stacked Amplifier with MCS using Current Reuse Technique

The circuit implementation as shown in figure 8 is folded cascode stacked amplifier with MCS, exploit MCS concept such that the current source transistors PMOS_1, PMOS_2 and NMOS_10, NMOS_11are driven together with the help of input pairs NMOS_5,NMOS_6 and PMOS_6 , PMOS_7 in order to obtain the current reuse and responsible to double the trans-conductance g_m. The transistors NMOS_7 and PMOS_5 form the MCS in design. Folded cascode amplifier input pairs shares the same bias current which is same to the MCS which takes the advantage of limited supply voltage. The current is reused four times through the MCS which results the reduction of NEF by half. The channels voltage noise is reduced by 0.707 to the original value because transistors PMOS_1, PMOS_2 and NMOS_10, NMOS_11 are driven together by the input pairs. The equivalent current consumed by the channel is cut by half which let the bias current to be with the help of MCS. The current obtained at the output stage is nearly about 5-10 percent of the input stage of that of folded cascode amplifier which will not detroit the NEF.

The transistors of this circuit are allowed to be driven in weak inversion region, as threshold are same in accordance to the 0.18 micron technology, for this reason only gate source bias voltage V_{GS} remains same for all the transistors. The current in the output stage can be given by equation 6.

$$\frac{P_{MCS}}{P_{reuse}} = \frac{2V_{GS}+V_{DS}}{2V_{GS}+V_{DS}} \quad \text{..... (6)}$$

P_{MCS} denotes the power consumption of amplifier with MCS and P_{reuse} denotes the power needed by the inverter stacked amplifier.

The circuit of folded cascode stacked amplifier with MCS using current reuse technique is implemented in 0.18 micron technology operated at 1volt as shown in figure 8; the signal extracted at the input node of amplifier is 2mV which amplified in order to amplify and obtained voltage swing of 414.8mV as a result the signal obtained at the output node further processed by conditioning circuitry to obtain the disease information.

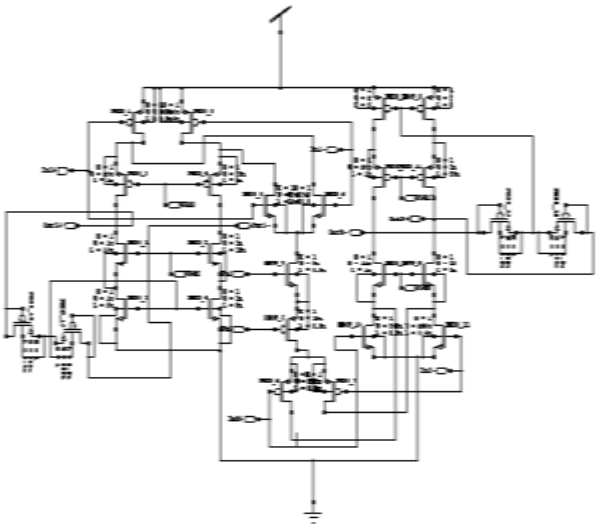

Fig8: Schematic Implementation of Folded Cascode stacked Amplifier with MCS using Current Reuse Technique

The dc response is shown in the figure 9, The AC response plot is illustrated in figure 10 and Noise analysis is shown in figure 11, in which magnitude of input noise (inoise), output noise (onoise) and total noise (totnoise) is represented.

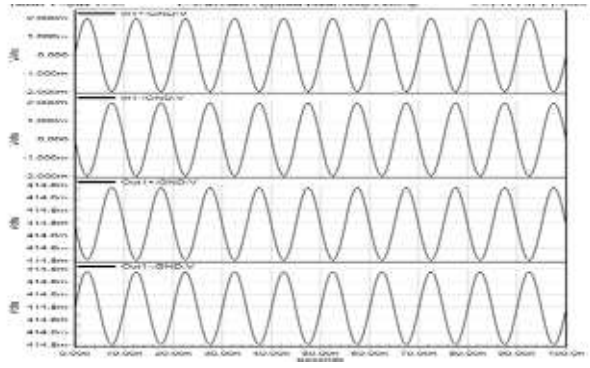

Fig 9: Simulation Waveform of Folded Cascode stacked Amplifier with Mid rail current sink/source (MCS) using Current Reuse Technique

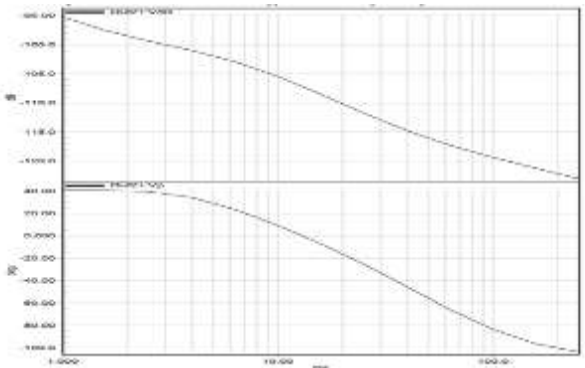

Fig 10: AC response of Op-amp (a).Magnitude Response (dB) (b).Phase Response (Deg)

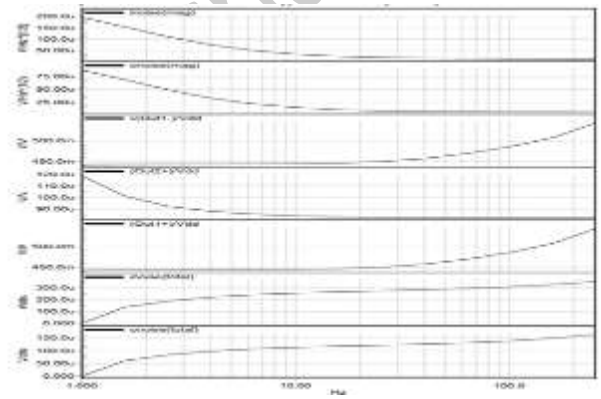

Fig 11: Noise Analysis Response of Folded Cascode Amplifier with MCS (Using Current Reuse Technique)

C. Analysis of Performance in between both Architectures

TABLE 1: COMPARISON BETWEEN VARIOUS PARAMETERS

S.No	Parameters	Units	Simulated Results	
			Inverter Stacked-4 Amplifier	Folded Cascode Stacked Amplifier
1.	MOS Technology	nm	0.18	0.18
2.	Supply Voltage	V	1	1
3.	Gain	dB	49.57	46.31
4.	Phase Margin	degree	90	50
5.	NEF	NA	1.5	1.7
6.	CMRR	dB	85.29	42.29
7.	PSRR	dB	45.22	32.69
8.	IRN @ 300Hz	V/√Hz	150u	200u
9.	Power Dissipation	W	1.89x10^-11	6.18x10^-11
10.	Current	A	74f	76f
11.	GBW	Hz	90.45k	62.1k
12.	Frequency	Hz	300	300
13.	Figure of Merit	NEF^2V_{dd}	2.25	2.89

4. DISCUSSIONS ABOUT PARAMETERS

Gain, Cardiac signal is first extracted with the help of transducer which is basically the Ag-Cl electrode, as result of which ECG is converted to the electrical voltage low in amplitude lies in the range of 1mV-5mV. The succeeding stage is the analog front end bio-potential amplifier, which is considered as predominant part of the whole signal conditioning circuitry, plays crucial role in order to determine the overall performance of recording system. The gain associated with both topologies is compared; the inverter stacked amplifier with current reuse technique reflects the gain of 49.57dB with 2mV voltage at the input node of amplifier and the other topology is folded cascode stacked amplifier with MCS using current reuse technique gives the gain of 46.31dB with same input voltage of 2mV. In accordance the comparison of both topologies a considerable amount of gain is obtained from inverter stacked amplifier.

CMRR, Amplifier's ability to reject the common mode signals can be determined by the common mode rejection ratio, the extracted signal get distorted when coupled with noise originated from ac sources, external noise and electrode noise due to which the performance of system get disturbed and ECG signal loses the obtained information from heart. The CMRR obtained from the Inverter stacked amplifier

is 85.29dB and from other architecture folded cascode stacked inverter with MCS is 42.29dB.

PSRR,The change in the output voltage of the amplifier due to change in the supply voltage is determined by the PSRR. Cardiac potentials are weak signals posses low amplitude, if such signals need proper amplification the variation in the supply voltage must be eliminated. Such disturbances detroit the performance of the recording system. The PSRR obtained from the inverter stacked amplifier using current reuse technique is 45.22dB and from other topology the folded cascode stacked amplifier with MCS obtained is 32.69dB. In order to amplify the weak bio-potentials rather than variation in supply voltage fact that such variation in supply voltage are large enough than weak bio-potential signals, it is necessary that topology must attain the high PSRR

IRN (Input referred Noise), The front end amplifier of bio-signal recording system is highly prone to noise, which is another important factor that dominates the performance and functionality of recording system. Cardiac system being weak and low frequency signals get easily contaminated with the noise. There are two types of noise which predominately affect the whole system is thermal and flicker noise are combinely know as input referred noise IRN. Thermal noise is generated by the electrode for recording and MOS of the amplifier. The IRN performance obtained from the architecture is the inverter stacked amplifier using current reuse is 150u V/√Hz and the folded cascode stacked amplifier with MCS using current reuse technique. The noise should low in order to avoid debasing of weak cardiac signal. So, that the useful signal can be collected to extract the information.

Phase Margin, The parameter that determines the stability of opamp is phase margin (P.M); in order to attain proper stability of op-amp adequate phase margin is required. The more value of P.M signifies lesser amount of ringing effect, but too much P.M again causes ringing. So P.M should be at least 45 degree, preferably opamp should have 60 degree. The P.M obtained after the simulation of Inverter stacked-4 amplifier is 90^0 and folded cascode stacked amplifier with MCS using current reuse is 40^0.

Power Dissipation, The lower power consumption circuitry finds its application in battery operated portable screening devices; the bio-potential screening devices are quite bulkier and are not portable which makes it quite difficult for ongoing diagnostics and causes discomfort. Power consumption is also related to the frequency. The low power consumption is desired, else causes the excessive tissue heating also which causes discomfort in diagnosis. The power consumption exhibited by the inverter stacked-4 amplifier is 1.89x10^-11W and Folded cascode stacked amplifier with MCS is 6.18x10^-11 W.

Noise Efficiency Factor, NEF defines the performance of the front amplifier considered as figure of merit, NEF describes the how many times the noise of associated with the system and bandwidth is higher when compared to the ideal polar transistor. NEF depend upon the current consumption, with the low value of current good NEF is obtained. The NEF obtained from the inverter stacked-4 amplifier is 1.5 and from the other topology folded cascode stacked amplifier with MCS obtained is 1.7.

5. CONCLUSION AND FUTURE WORK

In this research paper, I have designed and demonstrated Front End Cardiac Signal Amplifier for ECG system. The first and predominant stage of the signal conditioning circuitry AFE, which is decision making circuit which defines the overall functionality and performance of system. The front end bio-potentials amplifiers or Low noise amplifier are preferred responsible for observation and amplification of weak low frequency and amplitude signal as well rejection of noise which get coupled with cardiac signal which becomes the limiting factor. The crucial parameters identified which posses constraints on design of amplifier, such as gain, NEF, noise,CMRR,PSRR and power dissipation have been optimized to obtain the considerable values. Architectures selected satisfy the above mentioned parameters.

With vast examination of bio-inspired circuit topologies which makes use of current reuse technique, I have proposed two different architectures which were studied and implemented are Inverter Stacked-4 amplifier and folded cascode stacked amplifier with MCS designed using current reuse technique (without increasing current I_d, the g_m is boosted up).

Both the amplifiers were implemented in 180nm technology and simulated; parameters obtained were analyzed and compared. As a result the design of inverter stacked-4 amplifier proves to achieve the better performance and best suited design for the input stage of ECG recording system in comparison to the folded cascode stacked amplifier with MCS.

Performance further can be improved of front end amplifier in accordance to need of desired detection signals of heart related ailments by some techniques as mentioned is Noise cancellation techniques can be employed when need to detect precisely ultra low voltage, in which signal current flows through path are in same phase but noise current are in 180 degree out of phase results in cancellation of noise.

Feedback techniques can be implemented while designing bio-potential amplifiers which are responsible to shift optimum noise impedance to desired point; it reduces the non linearity of circuit.

Recording system in future should be completely implantable in order to avoid the infection risk, such that without any intervention of human tuning can be done.

In future, ECG recording system should be compact, so that they can be directly integrated with sensing electrode.

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