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AREA EFFICIENT MIXED MODE SCAN ARCHITECTURE WITH EFFICIENT SCAN FLIP FLOP ARCHITECTURE

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Abstract-- The performance overhead of scan design is due to the scan multiplexers added to the inputs of every flip-flop. In today's very high-speed designs with minimum possible combinational depth, the performance degradation caused by scan multiplexer has become magnified. Hence to maintain circuit performance the timing overhead of scan design must be addressed. A new scan f/f-based weighted built-in self-test (BIST) technique is proposed based on weighted pseudorandom test pattern generation by proposing a new scan flip-flop design that eliminates the performance overhead of serial scan. The proposed design removes the scan multiplexer from the functional path. The proposed design can help in improving the functional frequency of performance critical designs. Furthermore, the proposed design can be used as a common scan flip-flop in "mixed scan" test wherein it can be used as a serial scan cell as well as a Random Access Scan (RAS) cell. The mixed scan test architecture has been implemented using the proposed scan flip-flop. The experimental results show a promising reduction in interconnect wire length, test time, and test data volume, compared to the state-of-the-art random access scan and multiple serial scan implementations. During the pseudo-random testing phase, a weighted random test pattern generation scheme is proposed by disabling a part of scan chains.

***Keywords*----Scan flip-flop, Serial scan test, weighted test-enable signals, Random access scan test, Mixed mode scan test, Low power test, Test application, time, Test data volume.**

1. INTRODUCTION

The functionality of electronics equipments and gadgets has achieved a phenomenal growth over the last two decades while their physical sizes and weights have come down drastically. The major reason is due to the rapid advances in integration technologies, which enables fabrication of many millions of transistors in a single integrated circuit (IC) or chip. Every IC in the industry follows Moore's law. According to Moore's law, number of transistors (transistor density) in an IC doubles in every 1.5 years. With the recent advances in the technology, device shrinks to nanometer scale, but density and complexity of the ICs keep on increasing. This may result in many manufacturing faults and device failure. To accommodate more number of transistors, the device feature size is reduced. Reduction in the feature sizes results in increasing the manufacturing faults and fault detection becomes very difficult. VLSI testing is becoming more and more important and challenging to verify whether a device functions properly or not. Conventional automatic test equipment (ATE) based testing method is no longer able to handle the ever-growing test challenges.

Logic built-in self-test (LBIST) is widely being adopted as the testing technique for most current day scan based designs. Logic BIST does not alter the scan structure of the designs permitting them to have both ATE based testing and also Logic BIST. The nature of vectors in Logic BIST are usually pseudo random and so even for a moderately sized design, several thousands of patterns are to be generated in the Logic BIST compared to a few hundreds of deterministic test patterns in ATPG to achieve adequate fault coverage. So, methods to improve the fault coverage of Logic BIST by increasing the pattern efficiency are constantly explored.

LBIST found its use mainly in safety-critical (automotive, medical, military), mission-critical (deep-space, aviation) and high-availability (telecom) applications. However, process technologies plunging below 22nm, LBIST will become compulsory for application specific integrated circuits (ASICs), application specific standard products (ASSPs) and complex commercial ICs (Nan Li, et al., 2015). Any electronic system employed in safety critical applications is expected to have a periodical self testing scheme for sustained

error free operation. For example, medical electronic devices need to test themselves to assure continued safety of the patients. Another example is automotive electronics. With the explosion in the growth of the automotive semiconductors industry comes an associated and intense focus on high silicon quality and reliability. The last thing anyone wants is a brake 3 system failure due to a latent silicon defect, and concerns over reliability are driving changes in the testing requirements for these chips. The electronics must meet certain safety standards to accommodate the fast growing technological revolution.

There are various flip-flop structures even for the same type of flip-flop. However, they operate in a similar manner and are obtained by cascading two latches each showing input logic values at one of the two clock phases (clock = 1 and clock = 0). One of a scan cell implementation and bits based circuit as shown Figure 1. It is a positive edge triggered Mixed input D flip-flop (MD flip-flop) whose transition. The circuit highlighted by the dashed rectangle is the multiplexer used for selecting between the functional data-in (D) and test scan-in (TI) inputs. The circuit between the nodes DP and MD is the master latch of the flip-flop and this is connected to the slave latch, the circuit between the node MD and the output (Q). When the test enable signal (TE) is set to 1 (0), TI (D) is selected. The value of TI (D) then propagates into the master latch when clock (CP) is low. Meanwhile, the nodes in the slave latch retain the values from the previous clock cycle. When CP turns to high, the signal stored in the master latch propagates into the slave latch and to the output of the scan cell.

Built-in Self Test, or BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external automated test equipment (ATE).

BIST is a design-for-Testability (DFT) technique, because it makes the electrical testing of a chip easier, faster, more efficient, and less costly. The concept of BIST is applicable to just about any kind of circuit, so its implementation can vary as widely as the product diversity that it caters to. As an example, a common BIST approach for DRAM's includes the incorporation onto the chip of additional circuits for pattern generation, timing, mode selection, and go-/no-go diagnostic tests.

The main drivers for the widespread development of BIST techniques are the fast-rising costs of ATE testing and the growing complexity of integrated circuits. It is now common to see complex devices that have functionally diverse blocks built on different technologies inside them. Such complex devices require high-end mixed-signal testers that possess special digital and analog testing capabilities. BIST can be used to perform these special tests with additional on-chip test circuits, eliminating the need to acquire such high-end testers.

BIST is also the solution to the testing of critical circuits that have no direct connections to external pins, such as embedded memories used internally by the devices. In the near future, even the most advanced tester may no longer be adequate for the fastest chip, a situation wherein self-testing may be the best solution for.

Advantages of implementing BIST include: 1) lower cost of test, since the need for external electrical testing using an ATE will be reduced, if not eliminated; 2) better fault coverage, since special test structures can be incorporated onto the chips; 3) shorter test times if the BIST can be designed to test more structures in parallel; 4) easier customer support; and 5) capability to perform tests outside the production electrical testing environment. The last advantage mentioned can actually allow the consumers themselves to test the chips prior to mounting or even after these are in the application boards.

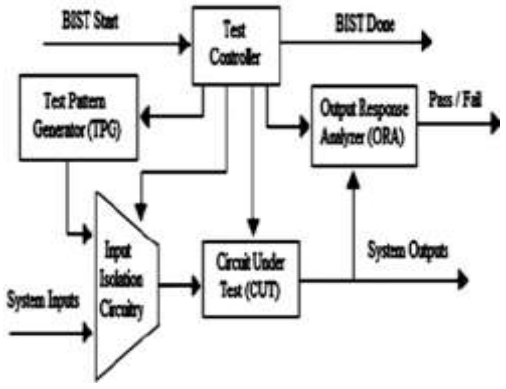

Fig 1: bits based circuit

BIST allows hierarchical decomposition of cascaded devices for test purposes -Example - Board with few chips: For the chip test system sends

control signal to the board activating BIST on chip. Results are sent back to the system. In case of errors BIST hardware indicates which chip was defective. BIST tests all the embedded designs and interconnects, leaving only functional verification of the cascaded design to system-level tests. Test generation, practically impossible to carry tests and responses involving hundreds of chip inputs through many layers of circuitry to chip-under-test. BIST localizes testing eliminating these problems Test application ,BIST saves significantly test application time compared to external testers z BIST testing capabilities grow with the VLSI technology, whereas test capabilities always lag behind VLSI technology for external testing z Low development cost, as BIST is added to circuits automatically through CAD tools.

- Linear feedback shift register (LFSR)

These are n-bit counters exhibiting pseudo-random behavior.

• Built from simple shift-registers with a small number of XOR gates.

• Used for: random number generation and counters and error checking and correction

- Multiple input signature register (MISR).

Problem with ordinary LFSR response is compactation:

- Too much hardware if one of these is put on each primary output (PO)
  Solution: MISR – compacts all outputs into one LFSR
- Works because LFSR is linear – obeys superposition principle
- Superimpose all responses in one LFSR – final remainder is XOR sum of remainders of polynomial divisions of each PO by the characteristic polynomial.

2. EXISTING SYSTEM

2.1 Scan Flip-Flop Design

The serial scan is obviously not free from drawbacks. There are some inherent penalties associated with the serial scan. These penalties include: 1) performance overhead, 2) test data volume, 3) test power consumption, and 4) test application time. The performance overhead of serial scan is due to the scan multiplexer. The scan multiplexer falls into each clocked path and adds performance penalty of approximately two gate-delays. A circuit without scan design and with scan design is shown in Figure. As it is observable in Figure 2(a), the critical path of a sequential circuit without scan insertion is decided by the longest combinational path between two flip-flops. However, in a scan inserted sequential circuit (see Figure 2b) the same critical path is elongated by a scan multiplexer at the end of the combinational path. The scan design also adds an extra fan out at the output of a flip-flop. Both of these factors increase the critical path delay, hence reduces functional clock speed by 5% to 10%.This makes it necessary to eliminate the performance overhead of the scan multiplexer.

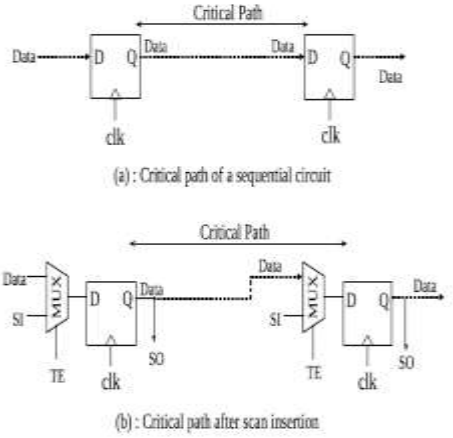

Fig2:Scan design performance overhead

Several solutions have been proposed to alleviate the performance penalty of scan design. One such solution that alleviates the performance overhead, as well as the other penalties associated with the serial scan design is the use of partial scan instead of full scan. In partial scan design, only subsets of all flip-flops in Circuit-Under-Test (CUT) are replaced by scan flip-flops to form a scan chain. This subset does not include flip-flops of the critical paths, hence reduces the performance penalty of scan.

Additionally, the partial scan design techniques also reduce test data volume and test application time which is directly related to test cost. However, the partial scan design techniques may lead to lower fault coverage of the CUT. The selection of flip-flops to be included into partial scan design can be testability measures based, structure-based, or ATPG based. The structure-based techniques select flip-flops to cut-off the feedback path. These techniques make use of heuristics based on network topology for selecting a minimum set of flip-flops and do not explicitly analyze the circuit behavior. The ATPG based techniques select flip-flops that are useful for test generation. These techniques first use sequential

ATPG to generate test vectors for all possible faults. For the faults which remain undetectable, the related flip-flops are found and these are included in partial scan design.

Most of the partial scan techniques require computationally demanding sequential ATPG, and cannot be afforded with ever increasing circuit complexity. Furthermore, partial scan design techniques do not provide high fault coverage as provided by the full scan design, and it is difficult to integrate them into the existing industrial design flow. Another approach for eliminating performance penalty of scan design is to use scan cell designs which provide high performance. Galbi et al. proposed a dual-edge pulse-triggered scannable flip-flop which is a high performance and low power scan cell. In a recent work, Satyadev. use a modified scan cell wherein the scan multiplexer is eliminated off the functional path by using separate master latch for functional and test mode. These high-performance scan cell designs can eliminate the performance overhead of scan design. However, such scan cells cannot be used in a mixed scan test architecture. Random access scan (RAS) is an alternative DFT technique that can alleviate the problems associated with the serial scan. Literature shows that RAS can greatly reduce test application time and test data volume along with test power reduction. However, the hardware overhead associated with RAS is prohibitively high. The routing congestion due to interconnect wiring is a serious issue that impedes the practical implementation of the RAS. In recent past, Baik. proposed some innovative changes to the basic RAS architecture to overcome routing congestion issue. In, Baik et al. proposed an improved version called Progressive Random Access Scan (PRAS) design to improve test time and routing wire length. The PRAS design uses separate row and column address decoders in place of a single address decoder. The same authors have shown that the arrangement of RAS cells in a square grid of size p N p N is optimal for improving routing congestion, where N is the number of scan cells. Mudlapur et. al further addresses the routing congestion problem by eliminating the scan-in and test-enable lines. However, it introduces an additional gate delay in the clock path due to clock gating. Adiga et al proposed a modified T flip-flop design to eliminate the clock gating introduced in the clock tree. In spite of these efforts, routing congestion is still a critical issue that needs to be resolved in order to make RAS implementation practical. Furthermore, observability of storage cell and RAC architecture implementation are some other issues which need to be addressed properly.

The first step in mixed mode scan architecture implementation is segregation of all the flip flops into two groups. One group of the flip-flops is assigned to serial part and the flip-flops from the second group go into RAS part. The segregation of scan cells among serial part and RAS part is very crucial for test time, test data volume, test power dissipation, and area overhead. For the current work, we have used a simple criterion based on test pattern care bits. The scan cells for which most of the patterns are specified with care bits are included in serial scan part. Where as those scan cells.

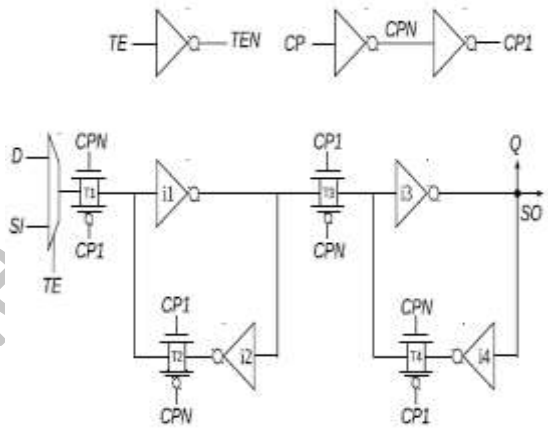

Figure 3.A conventional scan flip-flop design

A conventional scan flip-flop design is shown in Figure 3. This scan cell is a master-slave latch based positive edge triggered mixed input *D* type flip-flop. The transmission gate *T*1, and the inverter pair connected back to back via transmission gate *T*2 forms the master latch. The slave latch comprises of transmission gate *T*3 and the inverter pair connected back to back via transmission gate *T*4. The multiplexer at the input of master latch selects between functional input (*D*) and scan input (*SI*) depending upon the value of test control signal test enable (*TE*). In test mode, when *TE* is high (1), *SI* is selected and is connected to master latch's input. When the clock signal (*CP*) is low (0), the value of *SI* propagates to the master latch. In the meantime, slave latch retains the value from previous clock cycle. The value latched into the master propagates to slave latch when *CP* turns to high (1), and to the output *Q* of scan flip-flop. Similarly, when the test

enable signal (*TE*) is set to 0, functional input *D* is selected, and the circuit operates in functional mode. The architecture of mixed mode scan is shown figure 4.The mixed mode scan architecture has three main components: Multiple Serial Scan (MSS) part, *RAS* part, and the test controller. The multiple serial scan part is denoted by p-serial, and *RAS* part is denoted by p-random. The p-serial part consists multiple serial scan chains with inputs *SI*0, *SI*1, and *SI*2, and a *MISR* at the outputs to compact the test responses. The number of scan chains can vary depending upon the available number of test pins. The shift operation in p-serial is performed by using the scan enable cum scan clock signal *SCK*. The *RAS* part is denoted by p-random and implemented as *PRAS* architecture. The row address shift register and column driver are used for writing test data. Based on the column address the test controller generates control signals to drive the *bit* and bit-bar lines using the column driver. The Sense Amplifier and MISR block are used to read and compact the test response data. The *MISR* for p-serial and p-random are connected serially with the controller to shift out the test response signature via the scan *I/O* port. The two input signals test-mode0 and test-mode1 connected to the test controller are used to operate the circuit between functional mode and the test mode and exercising the test.

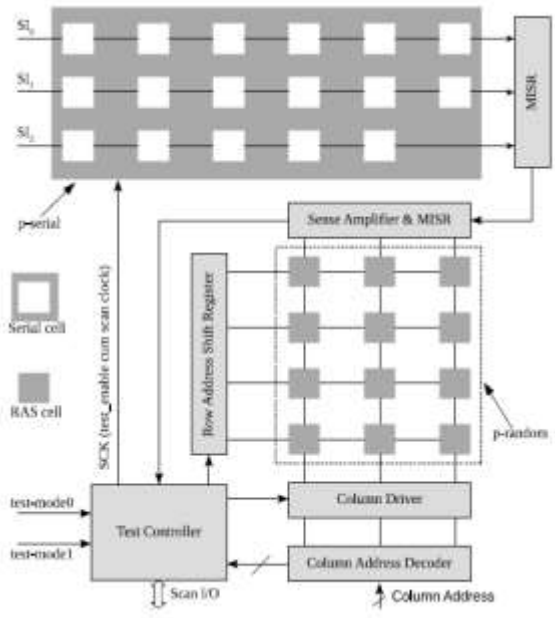

Fig 4: Mixed mode scan design architecture

3. PROPOSED METHOD

3.1. MIXED MODE SCAN DESIGN

This segment investigates the utilization of the RAS examine flip-failure to execute blended mode check design. In a blended output design, a portion of the flip-flops are utilized to frame sequential scan and rest of the flip-flops structure RAS engineering. Both sequential scan test engineering and RAS test design are worked simultaneously. In the simple execution of the blended output, the flip-flounders that are incorporated into sequential scan design are supplanted by a sequential output flip-flop and the flip-tumbles that are incorporated into RAS engineering are supplanted by RAS cell. In blended mode examine structure the clock should be kept high all through the test mode to perform RAS cell read/compose activity. Thus, the sequential output part can't be worked in simultaneous to RAS utilizing the regular sequential scan cell. The proposed scan cell conquers this issue by utilizing test control motion as a moderate recurrence filter clock and permits to work both sequential and RAS configuration in parallel.

The proposed scan design eliminates the need for two separate scan cell libraries for implementing serial scan part and RAS part. It provides a common scan cell that can be used both as a serial scan cell as well as a RAS cell. Schematic design of area and performance efficient, progressive random access scans cell is shown in figure 5 and serial part respectively. The first step in mixed mode scan architecture implementation is segregation of all the flip flops into two groups. One group of the flip-flops is assigned to serial part and the flip-flops from the second group go into RAS part.

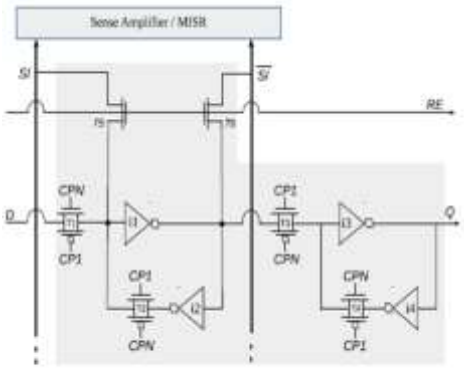

Figure 5: Random Access Scan (PRAS) Cell

For Proposed Work we can modify the architecture by removing the serial data processing unit and we use the RAS cells also for serial communication. The modified mixed mode scan design architecture is shown in figure 6.

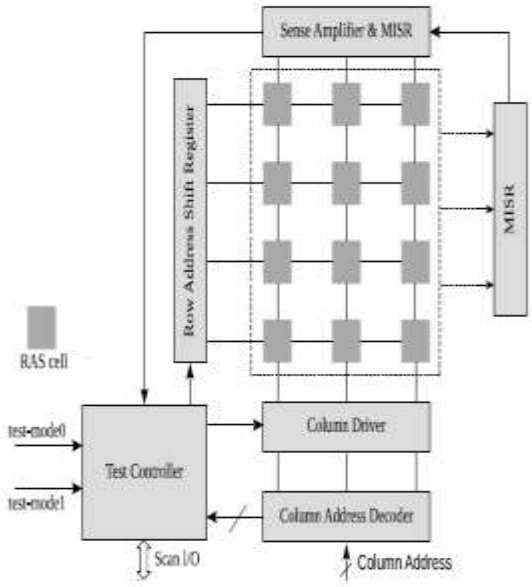

Fig6: Proposed Mixed mode scan design architecture

The segregation of scan cells among serial part and RAS part is very crucial for test time, test data volume, test power dissipation, and area overhead. For the current work, we have used a simple criterion based on test pattern care bits. The scan cells for which most of the patterns are specified with care bits are included in serial scan part. Whereas those scan cells for which most of the test patterns have unspecified or don't care bits are included in RAS part.

The functionality of the circuit is controlled by the two test mode control signals test-mode0 and test-mode1. Depending upon the states of the test control signals the circuit can operate in four modes. When both signals are 0, the circuit operates in normal functional mode. The remaining three states are mixed-mode (01), p-random mode (10), and p-serial-mode (11). The test process starts with mixed-mode with p-serial and p-random loading/unloading the test stimuli/response concurrently. The shift operation in p serial which is synthesized using the read/write operation in p-random is carried out in two steps. Note that the read/write operation in RAS corresponds to loading/unloading of test stimuli/response. First, the row enable signal is asserted to read the existing state of the RAS cells. The read operation is performed row by row using the sense amplifier.

4. SIMULATION RESULTS

The total designs are done and implemented in Xilinx ISE 14.7 with Verilog HDL coding.

Table I: Comparison of Existing and Proposed method.

Parameters	Mixed mode proposed	Mixed mode extension
Area	132 LUT's	89 LUT's
Delay	4.905 ns	4.805ns

5. CONCLUSION

The area efficient design for scan chain is proposed that which overcome the low performance due to critical path and high usage of multiplexers in design and replacing random scan architecture for mixed mode design. The new proposed design of mixed mode works for all conventional and test flow. Furthermore, the proposed scan flip-flop can be used both as a serial scan cell as well as a RAS cell, in the mixed mode scan test. The mixed mode scan design implemented with proposed scan flip-flop shows a promising reduction in interconnect wire length, test data volume, and test application time.

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