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OPTIMIZED VOLTAGE DETECTION USING NAND GATES FOR NAND FLASH MEMORY USING FSM

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ABSTRACT:

NAND flash memory is widely used in mainstream electronic products due to its high performance, low power consumption, non-volatility and high storage capacity. With the gradual reduction in feature size and more bits stored in each cell, NAND flash memory cells become more vulnerable to various channel noises, including data retention, cell-to-cell interference (CCI), program/erase (P/E) cycles and read disturb. The above noises significantly degrades the data-storage reliability. As a result, the data-storage lifetime is dependent on retention time and P/E cycles. Retention and CCI are recognized as the main sources of noise, which lead to significant performance deterioration of flash memory systems.

To analyse the current flash memory model we have proposed a switching-voltage detector and compensation circuits for an ultra-low-voltage CMOS inverter. The switching voltage of an inverter is an important design parameters for a digital circuit, and is determined by the difference in threshold voltages between MOSFETs. However, switching voltage varies significantly with fabrication process conditions and temperature. To address this problem, we have developed a threshold voltage difference detector circuit. We have also proposed a possible compensation technique for the inverter. Monte Carlo simulations demonstrated that the threshold voltage detector circuit can monitor the threshold voltage difference between pMOSFET and nMOSFET, and that the proposed inverter can achieve 80% reduction in switching-voltage variation with a 32nm CMOS inverter is utilized and implemented with HVTD compared to a conventional CMOS inverter. The Verilog version of the NAND flash memory is designed with the FIFO and FSM model for the FM which provides better results than existing design on NAND flash memory.

INTRODUCTION:

Ultra-low-voltage LSI devices that consist of subthreshold MOSFETs (MOSFETs that are operated in the region of weak inversion) have attracted much attention for use in “ubiquitous” smart sensor network systems [1]–[4]. Power dissipation for CMOS digital circuits operated in the subthreshold region can be 2 to 3 orders of magnitude lower than for conventional circuits. However, because the supply voltage of a digital circuit is lower than the threshold voltage of a MOSFET, variations in fabrication process conditions and temperature significantly impact circuit performance. In particular, the threshold voltage difference between pMOSFET and nMOSFET degrades circuit performance significantly, and changes the switching voltage of the CMOS inverter. Switching voltageis an important design indicator of performance and determiner of noise margin. Therefore, to enable stable operation of the subthreshold LSIs, a compact compensation technique for handing switching-voltage variations for the CMOS inverters required. In [5], a compensation technique for handing threshold voltage unbalance between pMOSFET and nMOSFET was presented. The technique is based on body biasing control techniques, and the switching-voltage detector is composed of a CMOS inverter whose input and output are shorted. However, the techniques require quite complicated circuit configurations—involving components such as a detector, comparators, shift registers, and a bias

circuit—to generate appropriate body-biasing voltages. These complicated configurations require significant power dissipation and chip area. Moreover, the output voltage signal of the switching-voltage detector fluctuates directly depending on supply voltage VDD. Therefore, more simple, robust, and compact compensation techniques are needed for an ultra-low-voltage CMOS inverter.

EXISTING MODEL:

A CMOS inverter operated in the subthreshold region displays different characteristics than a conventional inverter. We first describe a theoretical model of switching voltage and show the importance of the threshold voltage difference. We then present a threshold voltage difference detector circuit. A. Switching Voltage of a CMOS Inverter Figure 1 shows a CMOS inverter. When the circuit operates at a supply voltage lower than the threshold voltage of MOSFETs, MOSFETs are operated in the subthreshold region. Subthreshold current ID of a MOSFET can be expressed as:

$$I_D = K I_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \quad (1)$$

where K (=W/L) is the aspect ratio of the transistor, I0(= μCOX(η − 1)V 2 T) is a process-dependent parameter, μ is the carrier mobility, COX is the gate-oxide capacitance, η is the subthreshold swing factor, VT (= kBT /q) is the thermal voltage, kB is the Boltzmann constant, T is the absolute temperature, q is the elementary charge, and VTH is the threshold voltage of a MOSFET [6]. The switching voltage of the inverter VINV can be derived on the condition that currents flowing into both pMOSFET and nMOSFET are equal (IDP = IDN), and is given by

$$V_{INV} = \frac{1}{2}\left[V_{DD} - (V_{THP} - V_{THN}) + \eta V_T \ln\left(\frac{K_P I_{0P}}{K_N I_{0N}}\right)\right] \quad (2)$$

Impact on the switching voltage. Because the variations in preexponential factor and aspect ratio of the subthreshold currents for nMOSFET and pMOSFET (KN I0N and KP I0P) are small compared to variations in threshold voltage and are included in the logarithmic function, variations in these values can be ignored.

Reference Circuit Design for CMOS Inverter

A conventional switching-voltage detector in a CMOS inverter, that is an inverter whose input and output are shorted, generates the same output voltage as Eq. (2). Equation (2) depends on supply voltage and the detected signal changes with supply-voltage variations.

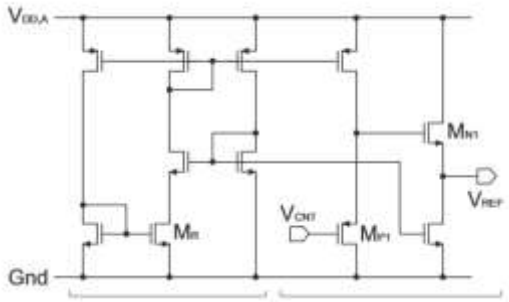

Figure 1.Schematic of the voltage reference circuit.

The circuit consists of a current source sub circuit and a threshold voltage difference detector sub circuit.For the first order of analysis, the current IP is tolerant of the threshold voltage variations, because the equation for IP does not contain the parameter of threshold voltage. As described below, although the output reference voltage VREF does not depend on the operating current, the current ensures stable operation of the circuit. The threshold voltage difference detector subcircuit consists of pMOSFET and nMOSFET source followers that are biased with the generated current through current mirrors. A gate voltage of pMOSFET (MP1) is biased with control voltage VCNT to control the output reference voltage level. In the detector subcircuit, gate-source voltages of transistors (MP1 and MN1) form a closed loop with control voltage VCNT and output reference voltage VREF , and the output reference voltage VREF is expressed as

$$\begin{aligned} V_{REF} &= V_{CNT} + V_{GS,P1} - V_{GS,N1} \\ &= V_{CNT} + V_{THP,P1} - V_{THN,N1} + \eta V_T \ln\left(\frac{K_{N1} I_{0N}}{K_{P1} I_{0P}}\right) \end{aligned} \quad (3)$$

The output reference voltage VREF can be expressed by the difference in threshold voltages between pMOSFET and nMOSFET (VTHP −VTHN). From

Eq. (3), the variations in output voltage due to process variations can be expressed as

$$\Delta VREF = \Delta VTHP,P\ 1 - \Delta VTHN,N1. \quad (4)$$

Therefore, the circuit can detect variations in threshold voltage difference that is independent of supply-voltage variations, with a simple circuit configuration. Note that the output reference voltage VREF does not depend on its operating current IP as shown in Eq. (3). The detected signal shows no supply-voltage dependence because the equation (3) does not contain the parameter of supply voltage.

Switching-Voltage Compensation

The switching voltage of the inverter changes with threshold voltage variations as shown in Eq. (2). Variation can be compensated for by using an on-chip signal of the threshold voltage difference detector. There are several possible compensation techniques, such as voltage scaling and body-biasing. In this design, voltage scaling is adopted to compensate for variations in switching voltage. From Eqs. (2), (3), and (4), the detected voltage VREF has different polarity from the switching voltage of the CMOS inverter. Therefore, if the detected signal is used as the supply voltage of the inverter, the switching voltage can be compensated. Figure 3 shows a switching-voltage compensated CMOS inverter. The circuit consists of three-stage CMOS inverters.

The output reference voltage VREF of the detector circuit is applied to the supply voltage of the first inverter. The supply voltage of the other inverters is set at a fixed digital supply voltage VDD,D. From Eqs. (2) and (3), the threshold voltage difference term is cancelled, and the switching voltage of the first inverter is compensated and is given by

$$V_{INV} = \frac{1}{2}\left[V_{CNT} + \eta V_T \ln\left(\frac{K_{N1}K_P}{K_N K_{P1}}\right)\right] \quad (4)$$

However, because compensation is performed by voltage scaling based on the on-chip detector's signal, the "high" level of the first inverter varies according to the supply voltage. To solve this problem, a fixed digital supply voltage VDD, D is used for the other inverters. The second and third inverters are normal CMOS inverters. However, because the logic function of the first inverter is already performed and the output voltage V1 is evaluated as "high" or "low", the effect of threshold voltage variations in the second and third inverters on the switching voltage is minimal.

PROPSOED DESIGN:

High Speed 1:1 N: P Inverter Using CMOS 32 nm:

The design aims to initiate the real time requirements of the NAND flash memory logic enhancing the design capabilities of each scenario of the design. Here the current scenario of the design from existing mathematical model section utilizes a formulation related to inverter design which have been modelled to utilize the memory design for LDPC decoder. From the design aspects of the proposed design we have utilized a FSM-FIFO based memory model utilizing the better approach for each set of the data transfers using HDL designer series.

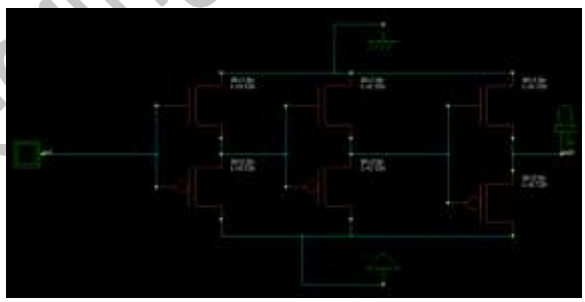

Figure 2a) Representing CMOS inverter high speed

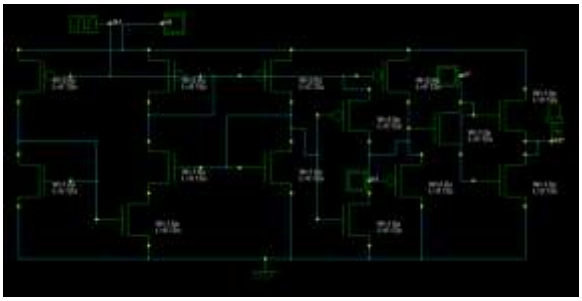

Figure 2b): Representing the final circuit model and its design using

IMPROVISED GATE CMOS VOLTAGE DETECTION FLASH MEMORY USING FSM CONTROL:

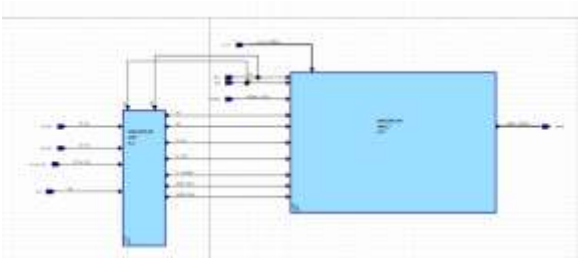

Figure 2c) Representing the block diagram of NAND flash memory

Our proposed design imparts the usage of front end modelling for the NAND flash memory would improvise the design with the different controlling inputs where the memory is modelling using FIFO. Each control input is to provide the control state and idle state of the read and write scenario each time interval.

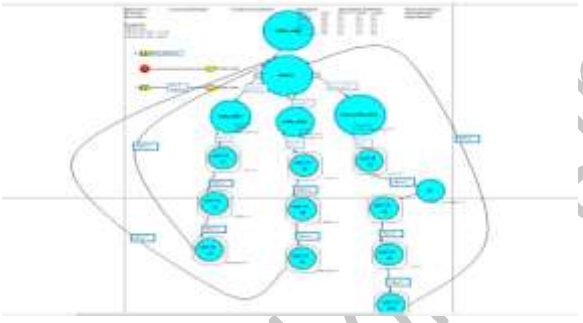

Figure 3: Representing the control input sequence for FIFO FLASH Memory.

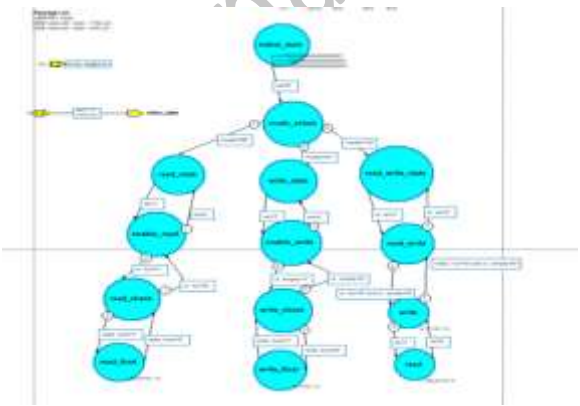

Figure 4: Representing the FSM BASED FIFO FLASH MEMORY

CONCLUSIONS:

The above study shows that the partial/quasi adiabatic logic circuit is a technique for the reduction of the energy dissipation, when compared to that with a conventional CMOS logic circuits switching under certain circumstances. All the input signals must be a controlled transition in the form of a ramp in adiabatic circuits, when compared with that of a conventional logic switching where only the input signals which have the different final logics state changes. The energy dissipation can be reduced by not switching instantaneous instead must be gradual process. In this paper, as we have examined with the circuits a low energy dissipation can be achieved with no significant improvements in rise/fall times. Due to the finite state of the threshold voltage of a MOS transistors these limitations are achieved and possibly to even a lesser extent of nonlinearity characteristics of the MOSFETs channel resistance.

RESULTS AND DISCUSSION:

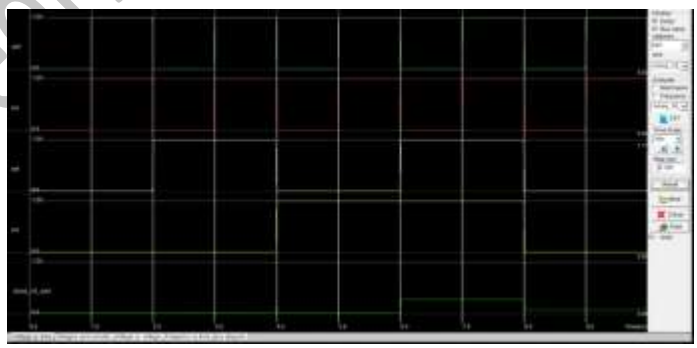

Figure 5a: Representing the Circuit wave form for inverter proposed

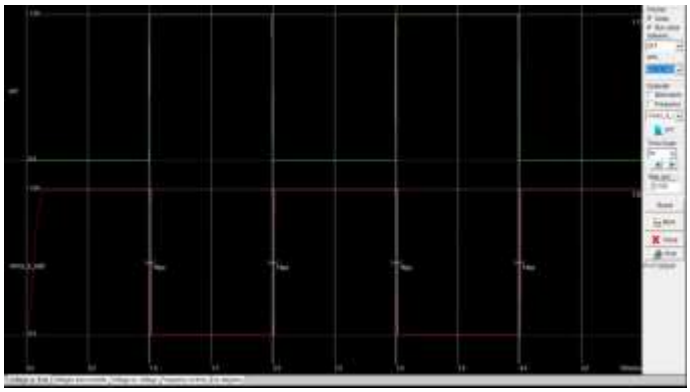

Figure 5b: Representing the Circuit wave form for existing inverter

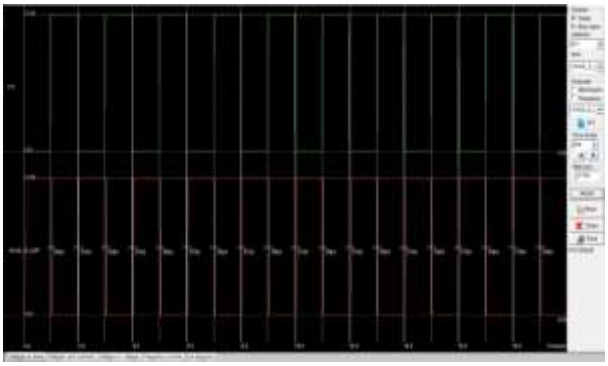

Figure 5c: Proposed wave form in 32 nm with 20ns time period

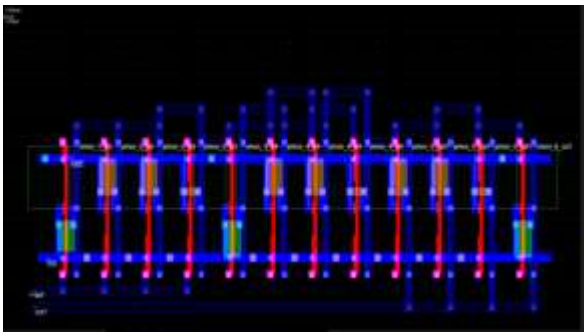

Figure 5d: Proposed layout in 32 nm for CMOS inverter

Table1: Representing comparison of Voltage detection Inverter with existing and proposed

SNO	PARAMETERS	AREA(nm²)				POWER(nw)				Delay			
	TECHNOLOGY	32	45	65	90	32	45	65	90	32	45	65	90
1	Existing Voltage detector inverter	24.68	36.53	70.54	105.57	5.25	14	18	32.5	18ps	20ps	12	18
2	Proposed Voltage detector inverter	14.8	23.2	46.5	68	0.2	0.3	0.3	0.1	15ps	17ps	7ns	4ns

Table2: Representing comparison of 16 bit Memory with existing and proposed

SNO	PARAMETERS	Existing LDPC Memory 16 bit	Proposed FSM FIFO memory 16 bit
1	AREA	11.3 %	5.8%
2	POWER	3.368W	1.38W
3	DELAY	34.87 ns	19.34 ns

The current design with LDPC decoder memory has more area and other performance factors which in turns enhances the same design model with inverter calculations for the FIFO FSM design have proved that existing has higher power compared with the proposed one also the Verilog implementation of 16 bit Memory has been implemented using HDL designer series.

FUTURE WORK

The study says that both the partial and fully adiabatic logic circuits can considers a primary task in designing any applications for which power conservation is the significant role like performance in any hand held digital portable systems those running upon batteries examples tablet computers, cell phones and other personal digital (PDA) assistants. With an adiabatic logic circuit approach, a pull-down circuit can conserve more energy rather than being dissipated through as a heat. In future depending upon the system requirements and its applications a suitable adiabatic logic circuit can be selected, designed and analyzed to reduce the power dissipation of such systems.

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