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PERFORMANCE ANALYSIS OF 64 BIT TRUNCATION ADDER USING CSA AND RCA ADDERS

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ABSTRACT:

Approximate addition is a technique to trade off energy consumption and output quality in error-tolerant applications. In prior art, bit truncation has been explored as a lever to dynamically trade off energy and quality. The data processed by many digital systems may already contain errors. In many applications, such as a communication system, the analog signal coming from the outside world must first be sampled before being converted to digital data. The digital data are then processed and transmitted in a noisy channel before converting back to an analog signal. During this process, errors may occur anywhere. Furthermore, due to the advances in transistor size scaling, factors such as noise and process variations which are previously insignificant are becoming important in today's digital IC design.

In this brief, an innovative bit truncation strategy is proposed to achieve more graceful quality degradation compared to state-of-the-art truncation schemes. This translates into energy reduction at a given quality target.This methodology is applied to minimizing the delay of representative carry-look ahead adders under energy constraints. Impact of various design choices, including the carry-look ahead tree structure and logic style, are analyzed in the energy–delay space and verified through optimization. The result of the optimization is demonstrated on a design of the fastest adder found.

Keywords: Adaptive precision, approximate computing, energy-quality scaling, error-tolerant systems, low-power design, VLSI.

INTRODUCTION

In conventional digital VLSI design, one usually assumes that a usable circuit/system should always provide definite and accurate results. But in fact, such perfect operations are seldom needed in our no digital worldly experiences. The world accepts "analog computation," which generates "good enough" results rather than totally accurate results. The data processed by many digital systems may already contain errors. In many applications, such as a communication system, the analog signal coming from the outside world must first be sampled before being converted to digital data. The digital data are then processed and transmitted in a noisy channel before converting back to an analog signal. During this process, errors may occur anywhere. Furthermore, due to the advances in transistor size scaling, factors such as noise and process variations which are previously insignificant are becoming important in today's digital IC design. Based on the characteristic of digital VLSI design, some novel concepts and design techniques have been proposed. The concept of error tolerance (ET) and the PCMOS technology are two of them. According to the definition, a circuit is error tolerant if: 1) it contains defects that cause internal and may cause external errors and 2) The system that incorporates this circuit produces acceptable results the "imperfect" attribute seems to be not appealing. However, the need for the error-tolerant circuit was foretold in the 2003 International Technology Roadmap for Semiconductors (ITRS). To deal with error-tolerant problems, some truncated adders/multipliers have been reported, but are not able to perform well in its speed, power, area, or accuracy. The "flagged prefixed adder" performs better than the non-flagged

version with a 1.3% speed enhancement but at the expense of 2% extra silicon area. As for the "low-error area-efficient fixed-width multipliers", it may have an area improvement of 46.67% but has average error reaching 12.4%. Of course, not all digital systems can engage the error-tolerant concept. In digital systems such as control systems, the correctness of the output signal is extremely important, and this denies the use of the error tolerant circuit. However, for many digital signal processing (DSP) systems that process signals relating to human senses such as hearing, sight, smell, and touch, e.g., the image processing and speech processing systems, the error-tolerant circuits may be applicable. The rest of the paper is organized as follows.

EXISTING DESIGN MODEL:

RCA Hybrid Model adder:

Increasingly huge data sets and the need for instant response require the adder to be large and fast. The traditional ripple-carry adder (RCA) is therefore no longer suitable for large adders because of its low-speed performance.

Many different types of fast adders, such as the carry-skip adder (CSK), carry-select adder (CSL), and carry-look-ahead adder (CLA) [18], have been developed. Also, there are many low-power adder design techniques that have been proposed [19].

However, there are always trade-offs between speed and power. The error-tolerant design can be a potential solution to this problem. By sacrificing some accuracy, the ETA can attain great improvement in both the power consumption and speed performance.

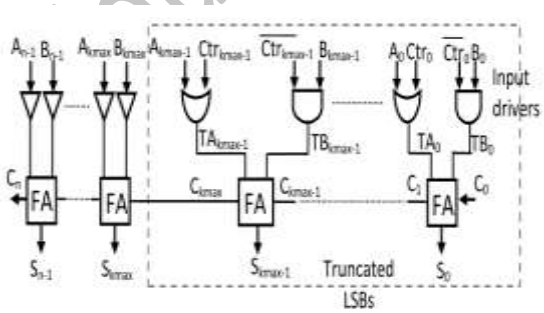

Figure1: Representing the Truncation adder using AND & OR gates.

The above bit truncation scheme can be easily implemented at circuit level in ann-bit RCA as shown in Fig. 2. No special cells are needed, as conventional full adders are used for all bit positions.OR&AND gates are employed as input buffers driving the full adders that receivekmaxLSBs of the operands, beingkmaxthe maximum number of LSBs that can be truncated. The control signals

Ctr_kmax−1...Ctr_0

Which allow dynamic adaptation ofk(withk<k_max), and hence of the energy-quality tradeoff at run-time. If signals Ctri(with 0≤i<k)are set to 1, the inputs Taiand TBiof thei_{th} fulladder are, respectively, 0 and 1, thus making its carry output equaltoCi=0. Once the truncation is applied, switching activity anddynamic energy are suppressed in allkfull adders associated withthe LSBs, regardless of the constant value used in thekLSBs.

In general, the above results need to be modified when considering different operations, such as subtraction. Indeed, the differenceA−Bis computed by first evaluating the 2s complement of thesubtrahendB, and then by adding it to the minuendA.Forthesubtraction operation, the output errorEdiffis the difference between the errorsEAandEBdue to the truncation ofAandB, respectively.Consequently,Ediffcan be reduced by ensuring thatEAandEBhave the same sign, instead of being opposite as in the addition operation. More precisely, the quality of the output of an approximate subtractoris maximized by truncatingkLSBs of the two operands by setting

Ai=Bi (with 0≤i<k), by simple extension of the above results.It is worth noting that the traditional zeroing bit truncation scheme automatically satisfies such a criterion, as it setsAi=Bi=0for0≤i<k. Hence, the bit truncation strategy in [15] is preferable when performing subtractions, not additions. When multiplication is considered, the energy of an approximate multiplier was found to strongly depend on the constant values chosen to truncate thekLSBsof the inputs. In other words, two different truncation schemes can lead to the same accuracy but to different energy consumptions, which makes the analysis much more complex.

MATHEMATICAL SCENARIO ON HYBRID ADDITION

In a conventional adder circuit, the delay is mainly attributed to the carry propagation chain along the critical path, from the least significant bit (LSB) to the most significant bit (MSB). Meanwhile, a significant proportion of the power consumption of an adder is due to the glitches that are caused by the carry propagation. Therefore, if the carry propagation can be eliminated or curtailed, a great improvement in speed performance and power consumption can be achieved. In this paper, we propose for the first time, an innovative and novel addition arithmetic that can attain great saving in speed and power consumption.

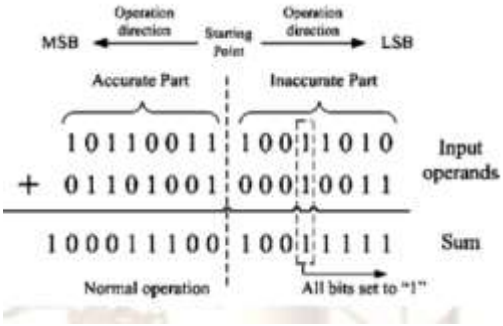

Figure 2: Representing the input inaccurate art and accurate apart addition

We first split the input operands into two parts: an accurate part that includes several higher order bits and the inaccurate part that is made up of the remaining lower order bits. The length of each part need not necessary be equal. The addition process starts from the middle (joining point of the two parts) toward the two opposite directions simultaneously.

In the example of Figure 2, the two 16-bit input operands, "1011001110011010" (45978) and "0110100100010011" (26899), are divided equally into 8 bits each for the accurate and inaccurate parts. The addition of the higher order bits (accurate part) of the input operands is performed from right to left (LSB to MSB) and normal addition method is applied. This is to preserve its correctness since the higher order bits play a more important role than the lower order bits. The lower order bits of the input operands (inaccurate part) require a special addition mechanism. No carry signal will be generated or taken in at any bit position to eliminate the carry propagation path. To minimize the overall error due to the elimination of the carry chain, a special strategy is adapted, and can be described as follow: 1) check every bit position from left to right (MSB to LSB); 2) if both input bits are "0" or different, normal one-bit addition is performed and the operation proceeds to next bit position; 3) if both input bits are "1," the checking process stopped and from this bit onward, all sum bits to the right are set.

PROPOSED MODEL FOR 8 BIT IMPLEMENTATION

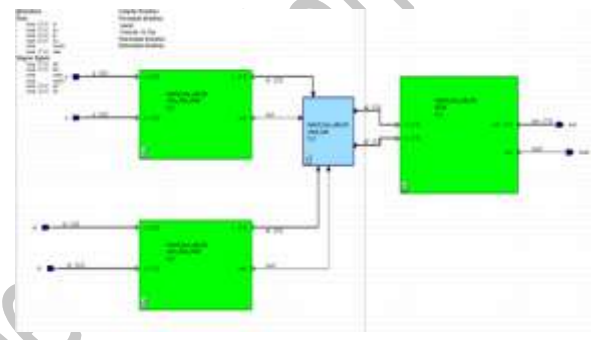

Figure3: Representing the Block diagram of proposed 8bit Hybrid Adder.

The block diagram of the hardware implementation of the design implementation using the circuit model based on HDL designer series would improvise the design scenario which imparts the different characteristics of the addition using CSA 8 bit and RCA 8bit via probabilistic approach for sum and carry equations. The most straightforward structure consists of two parts:

i. An accurate part and
ii. An inaccurate part.

The accurate part is constructed using a conventional adder such as the RCA, CSK, CSL, or CLA. The carry-in of this adder is connected to ground. The inaccurate part constitutes two blocks: a carry-free addition block and a control block. The control block is used to generate the control signals as shown in figure where the blue block is control cum input generator, to determine the working mode of the carry-free addition block.

Strategy of Dividing the Adder

The first step of designing a proposed ETA is to divide the adder into two parts in a specific manner. The dividing strategy is based ona guess-and-verify stratagem, depending on the requirements, such as accuracy, speed, and power.

With this partition method defined, we then check whether the accuracy performance of the adder meets the requirements preset by de-signer/customer. This can be checked very quickly via some software programs. For example, for a specific application, we require the minimum acceptable accuracy to be 95% and the acceptance probability to be 98%. The proposed partition method must therefore have at least98% of all possible inputs reaching an accuracy of better than 95%. If this requirement is not met, then one bit should be shifted from the inaccurate part to the accurate part and have the checking process repeated. Also, due to the simplified circuit structure and the elimination of switching activities in the inaccurate part, putting more bits in this part yields more power saving. Having considered the above, we divided the 32-bit adder by putting12 bits in the accurate part and 20 bits in the inaccurate part. Hence by virtue of the above design we model a 32 bit and 64 bit model using the 8 bit hybrid model.

64bit Implementation Adder using Hybrid CSA-RCA

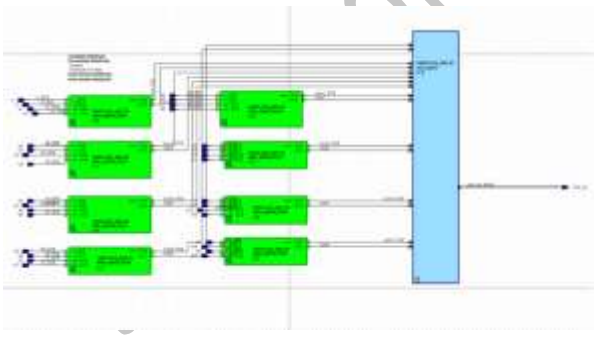

Figure 4: Representing the Hybrid Truncation Adder with CSA and RCA:

Our design improvises an 8 bit model and its implementation scenario as mention in figure 4. The structure of the figure represents the design of parallel scenario of 8 bit model which are suited with the current design platform of the implementing the CSA and RCA simultaneously.

The current design with truncation of the Hybrid proposed adder utilizes the parallel scenario on each set of output sum and carry generated from the 8 bit implementation. As per the design concept we have utilized 128 iteration when compared to 2^{64} iterations for each stage of the output observed in results and discussions.

RESULTS AND DISCUSSIONS:

Simulation results:

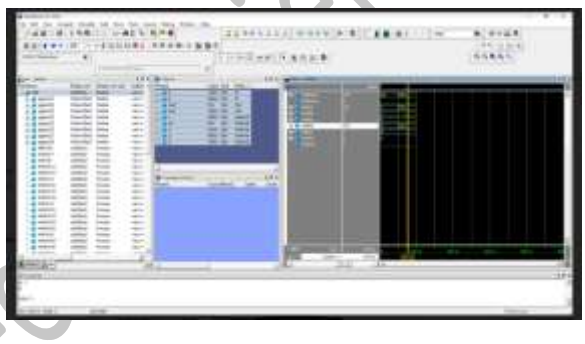

Figure5: Representing the design simulation of the circuit diagram mentioned

Figure 6: Simulation and Synthesis of 8bit CSA using Quartos tool Altera

Table 1: Representing the Existing Design adder and Proposed Hybrid Adder.

SNO	PARAMETERS	EXISITING 8 bit	EXISITING 16 bit	EXISITING 32 bit	Hybrid adder 8bit	Hybrid adder 16bit	Hybrid adder 32bit
1	AREA	9.3 %	34.56%	51.48%	7%	14.1%	22.71%
2	POWER	1.68W	5.86W	7.68W	0.92W	2.5W	5.76W
3	DELAY	26.67 ns	46.7 ns	70.5 ns	14.56 ns	24.8 ns	57.68 ns

The design with respect to RCA-8 bit from the existing model would improvise the proposed design with an area percentage about 9.3 for RCA8 bit ensuring the larger delay due to extensive forward feed awaiting for carry generation at each stage. In our design we have generated a carry skip scenario to utilize an approx. data addition which emphasizes the design model and its analysis as per the proposed model with 8, 16, 32 hence improves the delay and other performance factors.

CONCLUSIONS

This brief proposed a novel hybrid CSA –RCA approach for truncation scheme for the design of energy-quality scalable adders. In contrast to conventional zeroing bit truncation schemes, the proposed approach sets the inputs associated with the truncated digits equal to proper nonzero constant values that minimize the error on the output. The proposed technique is able to retain the dynamic energy-quality configurability of traditional reconfigurable approximate adders, while achieving more favorable energy-quality tradeoff which trades certain amount of accuracy for significant power saving and performance improvement, is proposed. Extensive comparisons with conventional digital adders showed that the proposed HTA outperformed the conventional adders in both power consumption and speed performance. The potential applications of the HTA fall mainly in areas where there is no strict requirement on accuracy or where super low power consumption and high-speed performance are more important than accuracy. One example of such applications is in the DSP application for portable de-vices such as cell phones and laptops.

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