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Renewable energy source fed Switched-Z-Source Inverter for EV applications

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Abstract—In this paper, a new topology Renewable energy source (Photo Voltaic(PV)) based Switched-Z-Source Inverter For EV applications. This inverter in comparison with the conventional Z-source inverter needs higher number of active elements, lower number of capacitors and inductors. Reduction of harmonics in voltage and current, weight, size and cost are the main advantages of the proposed topology. In addition, this inverter is able to solve the problem of short circuit across the inverter leg and consists of higher value of voltage gain when compared with the conventional switched boost inverter. Moreover, the developed topology of the proposed inverter based on switched inductor cells is introduced. Investigated and evaluate the performance of the proposed inverter in different operating modes. The proposed topologies are also compared with the conventional Z-source inverters in view of number of elements; the voltage gain and capability of fault tolerance. Finally, emulate the accuracy performance of the proposed inverter is reconfirmed by using the simulation results in MATLAB/SIMULINK software.

1 Introduction

Voltage and current source inverters are two kinds of conventional inverters. In voltage source inverter, the effective value of output voltage value is lower than the magnitude of the input dc voltage. In other words, this kind of inverter acts as a buck inverter. In the current source inverter, the effective value of output voltage value is higher than the magnitude of the input dc voltage. In other words, this kind of inverter acts as a boost inverter. As a result the voltage and current source inverters cannot work in buck-boost state. In addition, each kind of short circuit in voltage source inverter and open circuit in current source inverter has a bad influence in input sources.

To overcome the problems of the voltage and current source inverters, the Z-source inverter has been presented in [1]. This inverter is able to increase and or decrease the output voltage and does not use any time delay to turn on the power switches. As a result, it has high reliability. In [2–5], the control and modulation strategies of the Z-source inverter have been presented. The applications of this inverter [6–8] and its modelling and controller design [9–11] have been presented in literature. Other topologies for Z-source inverters have been presented in [12, 13].

In the conventional Z-source inverter, there is high voltage stress across the capacitor and the drawn current of the source is discontinuous. In order to overcome these problems, a new Z-source inverter has been presented in [14] that is called embedded Z-source inverter (EZSI). In this inverter, there is not common earth between the inverter and input voltage source. In addition, there is two input source in symmetric EZSI. These are main disadvantages of the EZSI. The other disadvantageous of the conventional Z-source inverter are its high voltage stress on capacitor, high inrush current and cost. In order to solve these problems, the series Z-source inverter (SZSI) has been presented in [15]. This inverter is able to solve the high voltage stress of the Z-source inverter but its boost factor is same Z-source inverter. The control method of the SZSI, desired design of elements and its application in photovoltaic systems to achieve maximum power point have been presented in [16–18]. In [19], the quasi Z-source inverter (QZSI) has been presented. In order to increase the voltage gain, the developed topologies of QZSI that are called diode assisted QZSI

(DQZSI) and capacitor assisted QZSI (CQZSI) have been presented in [20, 21]. The design and applications of the QZSIs in PV systems and motors drive have been presented in [22–24]. Common earth between the inverter and input voltage and also reducing the nominal values of the required elements are the main advantages of the QZSI but its boost factor is same SZSI. In order to increase the boost factor, series connection of Z-source inverters have been introduced [25–26]. The most important problems of series connection of inverters are high number of required dc voltage sources and capacitors. The other Z-source inverter is L–Z-source inverter [27]. This inverter consists of several advantages such as low inrush current but it is needed high value of duty cycle to obtain high voltage gain. In [28], a full-bridge topology for switched boost inverter (SBI) has been presented. Low voltage gain of this inverter in comparison with the conventional Z-source inverter is the main disadvantage but the size and cost is economically suitable.

In this paper, Renewable energy source (Photo Voltaic(PV))based Switched-Z-Source Inverter For EV applications is proposed. This inverter is able to generate higher voltage gain in comparison with the conventional switched Z-source inverter with the same number of elements. First, the proposed inverter and its operating modes are investigated. Then, the voltage gain, current inductor ripple and capacitor voltage are calculated. Moreover, a new topology based on switched-inductor cell is proposed. In order to determine the advantages and disadvantages of the proposed inverter, this inverter is compared with conventional Z-source inverters that have been presented in literature. Finally, the accuracy performance of the proposed inverter is reconfirmed through simulation results.

2 Proposed topology

Fig. 1 shows the power circuit of the basic proposed topology. In this topology, single-phase or three-phase inverter can be used. As shown in this figure, here the single-phase inverter is used. In addition, this topology consists of one switch, two diodes, one capacitor and an inductor with a voltage dc source.

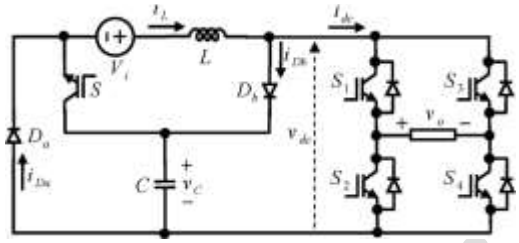

Fig. 1 *Power circuit of the basic proposed topology*

To simplify the analysis of the proposed topology, the following conditions are considered:

(i) All elements are considered ideally;
(ii) The dead time is ignored in stimulation pulses;
(iii) High capacitance is considered;
(iv) The resistive load is considered at the output.

2.1 *Operating modes of the proposed topology*

The on and off states of S_1, S_2, S_3 and S_4 switches and diodes of D_a and D_b determine the operating modes of the proposed topology. In this paper, the value of D_{ST} is defined by dividing the time interval of shoot-through (ST) state into total period. To have ST state happens in proposed inverter, the duty cycle of inverter switches (D) must considered higher than 0.5. The excitation signals of switches S_1 and S_4 has phase shift of 180° with excitation signals of S_2 and S_3 which causes two ST states at first and middle of T period. Duration of each ST states is considered $0.5D_{ST}T$. Due to two ST states during one period, total duration of ST states in one period is $D_{ST}T$. Under this circumstance, there are three operating modes.

2.1.1 *First operating mode (time intervals of $0 \le t < 0.5\ D_{ST}T_s$ and $0.5T_s \le t < 0.5(1 +$*

D_{ST})T_s):

In the first operating mode, all switches of the inverter in addition to the switch *S* are turned on and the legs of the inverter are in short circuit states. As a result, the circuit acts in ST state and the voltage across the diodes of D_a and D_b are negative that leads to turning off these diodes. In this operating mode, the voltage of the capacitor is reduced and so its stored energy is decreased. In addition, as the voltage of the inductor is positive, its stored energy is increased that leads to increase its current. The voltage of diodes is calculated as follows

$$v_{D_a} = v_{D_b} = -V_C$$

where v_{D_a} and v_{D_b} are the voltage of the diodes of D_a, D_b and V_C isthe average voltage of the capacitor *C*.

In addition, the capacitor current (i_C) is calculated as follows $i_C = -I_L$ (2)

Increasing the voltage gain value is the main aim of the proposed topologies. In order to determine the advantages and disadvantages of the proposed topologies, these are compared with several conventional Z-source inverters that have been presented in literature. The voltage gain value, number of elements in the proposed inverters and conventional Z-source inverters are shown in Table 2. As shown in this table, the proposed inverter (Fig. 1) voltage stress on capacitors and diodes and the required needs two passive elements and three semiconductors elements. This inverter needs lower number of passive elements in comparison with other Z-source inverters by considering same voltage gain value.

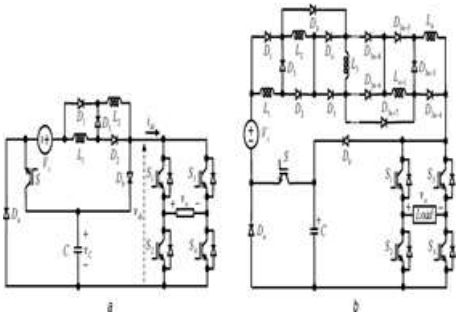

Fig. 3 *Proposed switched-inductors Z-source inverter*

a Developed switched-inductors cell ($n = 2$)

b Developed switched-inductors cell ($n \geq 2$)

Fig. 4*a* compares the boost factor in the proposed inverters with the conventional Z-source inverters. According to this figure, the proposed inverter with $n = 1$ has higher boost factor in comparison with the conventional SBI that has been presented in [28]. In addition, this parameter in the proposed inverter is same as the presented Z-source inverter in [1], while the number of required passive elements in the proposed inverter is half the conventional Z-source inverter. It is important to note that it is possible to obtain higher voltage gain value by increasing the value of ST state duty cycle and the number of switched-inductors cells.

For instance, by considering $D_{ST} = 0.15$, the voltage gain value of the conventional Z-source inverter is equal to 1.43 while in the same condition and by considering $n = 2$ the voltage gain value of the proposed inverter is equal to 2.09. It is pointed out that by considering $n = 3$, the voltage gain is increased to 3.25 and by considering $n = 4$, this value will be increased to 5.8.

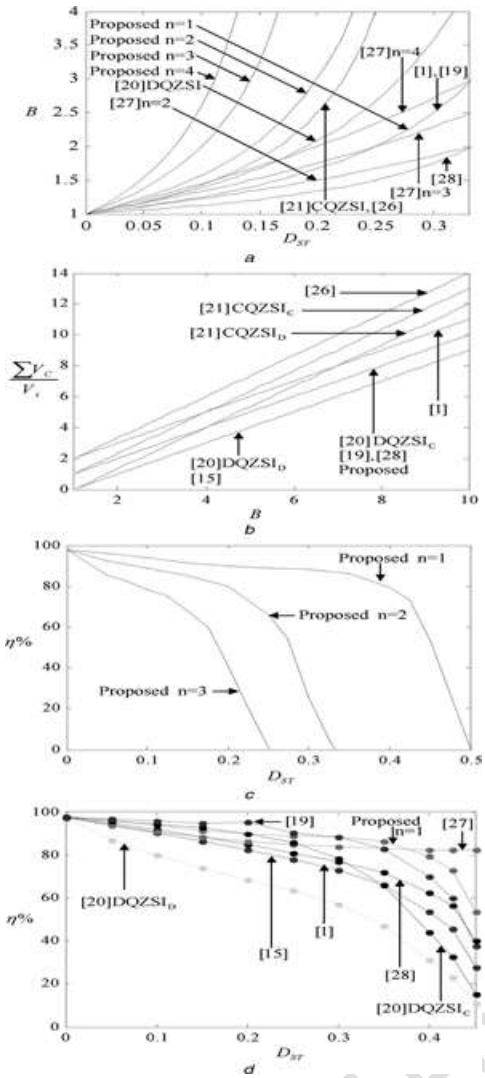

Fig. 4 *Comparisons of topologies*

a Comparison of boost factor

b Comparison of voltage stress on capacitors

c Comparison of efficiency between the proposed topologies

d Comparison of efficiency between the basic proposed topology and conventional inverters

Fig. 4*b* compares the total voltage stress on capacitors against *B* in the proposed inverters with the conventional Z-source inverters.

According to this figure, the proposed inverter has lower voltage stress on capacitors in comparison with the many conventional topologies.

Fig. 4*c* shows the comparison of efficiency between the proposed topologies based on the parameters which have been summarised in Table 3.

Table 3.Used parameters in obtaining of efficiency (case study)

Parameter	Value
V_i	50 V
r_L	0.2 Ω
r_C	0.1 Ω
R	55 Ω
$V_{F,D}$	0.6 V
r_D	0.1 Ω
$V_{F,S}$	0.5 V
r_S	0.5 Ω
f_s	5 kHz

According to this figure, the efficiency of the basic proposed inverter (n = 1) is higher than 80% for D_{ST} between 0 and 0.4. As expected, the efficiency of the proposed topologies decreases by increasing the number of switched-inductor cells. Fig. 4*d* shows the comparison of efficiency between the basic proposed topology and conventional topologies based on the parameters which have been summarised in Table 3. According to this figure, the proposed inverter by considering n = 1 has higher efficiency in comparison with the conventional Z-source inverter [1], SZSI [15], DQZSI [20] and SBI [28].

3. Simulation results and Discussion:

To verify the accuracy performance of the proposed topology, the simulation results are used. All simulation results are obtained by using MATLAB/SIMULINK software program. Table 4 shows the values of the used parameters and elements in the proposed inverters.

Table 4 Used parameters in simulation:

Parameter	Value
input voltage (V_i)	50 V
switching frequency (f_s)	15 kHz
Inductor (L)	1.2 mH

x_L%	36.67 %
Capacitor (C)	47 μF
x_C%	0.34%

3.1 Simulation results of the basic proposed inverter (n = 1)

Fig. 5 shows the waveforms of the basic proposed inverter with an inductor (n = 1). The load is resistive and its value is 55 Ω. The ST duty cycle (D_{ST}) is 0.2. The input voltage is shown in Fig. 5*a*. According to this figure, the value of input voltage is 50 V. The voltage across D_a diode is shown in Fig. 5*b*. According to this figure, the value of this voltage in ST state is −83.15 V.
This value is close to obtained value from (1) which is equal to −83.33 V. As expected, the value of the voltage across this diode in non-ST state is 0 V. The current of D_a diode is shown in Fig. 5*c*. This figure verifies the obtained results from theoretical analyses and this diode are turned off in ST state and in non-ST state, the current of D_a diode is equal to the current of the inductor. The voltage across D_b diode is shown in Fig. 5*d*. The value of this voltage is equal to value of voltage across D_a diode. The current of D_b diode is shown in Fig. 5*e*. This figure verifies the obtained results from theoretical analyses. The voltage across switch of S is shown in Fig. 5*f*. According to this figure, the voltage stress on the switch is 83.35 V. This value has a small difference with the obtained value from (14) which is equal to 83.33 V. The current through switch of S is shown in Fig. 5*g*. According to this figure, the maximum current of the switch is 2.39 A.

This value is coincident with the obtained value from (38) and (42). The inductor voltage is shown in Fig. 5*h*. According to this figure, the inductor voltage value in ST state is positive and equal to 133.17 V. This is close to the obtained value from (3) which is equal to 133.33 V. The inductor voltage value in non-ST state is equal to − 33.36 V that is close to its obtained value from (7) which is equal to − 33.33 V. The inductor current is shown in Fig. 5*i*. As shown in this figure, the inductor current's ripple and its average values are equal to 2.04 and 0.72 A, respectively. These are close to the obtained values from (17) and (22) which are 2.02 and 0.74 A, respectively. Fig. 5*j* shows the capacitor voltage waveform. The capacitor voltage ripple and its average values are obtained from (23) and (13) that are equal to 0.21 and 83.33 V, respectively.

These values verify the obtained results from simulation. Fig. 5*k* shows the dc-link voltage waveform. On the basis of this figure, the dc-link voltage value in ST state is equal to zero and in non-ST state is in its maximum value that is equal to 83.32 V. This has a small difference with the obtained value from (14) which is equal to 83.33 V.

The output voltage is shown in Fig. 5*l* that consists of positive level, negative level and zero level. These values reconfirm the obtained results from theoretical analysis and its maximum value is equal to 83.33 V

3.2 Simulation results of the developed proposed inverter (n = 2)

In this subsection, the simulation results of the proposed inverters based on switched-inductors cell are presented. The proposed inverter with switched-inductors cell consists of two inductors (n = 2). The load is resistive–inductive and its value is 55 Ω/120 mH. The proposed inverters can operate with different modulation methods.

Hence, to verify the accuracy performance of the proposed topology with different modulation techniques, the PWM control which has been presented in [28] is used. The ST duty cycle (D_{ST}) and modulation index are selected 0.25 and 0.7, respectively. In the output filter, the capacitor and inductor have the values of 10 μF and 1.2 mH, respectively.

Fig. 6 shows the waveforms of the proposed inverter based on switched-inductor cell consists of two inductors (n = 2). The input

voltage is shown in Fig. 6*a*. According to this figure, the value of input voltage is 50 V. The voltage across the diodes of D_a and D_b is shown in Fig.

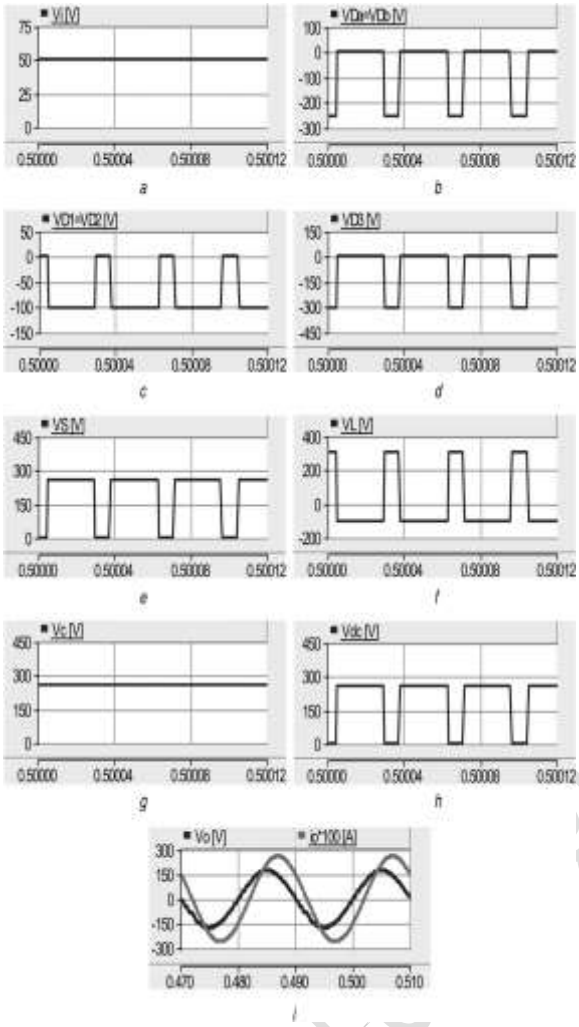

Fig. 5 *Simulation results of the basic proposed inverter (Output load=55 Ω)*
a Input voltage
b Voltage across diode D_a
c Current through diode D_a
d Voltage across diode D_b
e Current through diode D_b
f Voltage across switch *S*
g Current through switch *S*
h Voltage across inductor *L*
i Current through inductor *L*
j Voltage across capacitor *C*
k DC-link voltage
l Output voltage

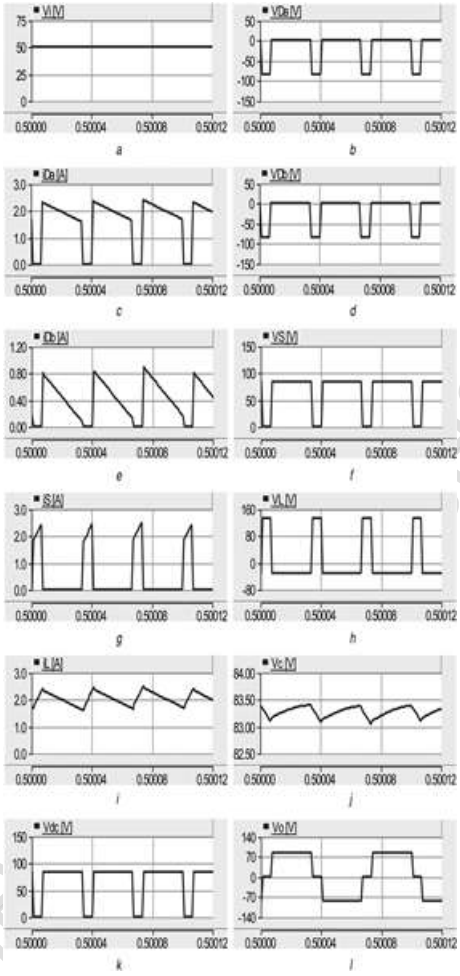

Fig. 6 *Simulation results of the developed proposed inverter based on switched-inductors cell with two inductors (Output load=55; Ω/120 mH)*

a Input voltage
b Voltage across diodes D_a and D_b
c Voltage across diodes D_1 and D_2
d Voltage across diode D_3
e Voltage across switch S
f Voltage across inductor L
g Voltage across capacitor C
h DC-link voltage
i Output voltage and current

6*b*. According to this figure, the value of this voltage in ST state is −249 V. This value is close to obtained value from (1) and (13) which is equal to −250 V. As expected, the value of the voltage across these diodes in non-ST state is 0 V.

The voltage across the diodes of D_1 and D_2 is shown in Fig. 6*c*. According to this figure,

the value of this voltage in non-ST state is −99.5 V. This value is close to obtained value from (32) which is equal to −100 V. As expected, the value of the voltage across these diodes in ST state is 0 V. The voltage across the diode of D_3 is shown in Fig. 6*d*. According to this figure, the value of this voltage in ST state is −298 V. This value is close to obtained value from (28) which is equal to −300 V. As expected, the value of the voltage across these diodes in non-ST state is 0 V. The voltage across the switch of *S* is shown in Fig. 6*e*. According to this figure, the value of this voltage in non-ST state is 249 V. This value is close to obtained value from theoretical analysis which is equal to 250 V. As expected, the value of the voltage across these diodes in ST state is 0 V. The inductor voltage is shown in Fig. 6*f*. According to this figure, the inductor voltage value in ST state is positive and equal to 299 V. This value is close to the obtained value from (30) which is equal to 300 V. The inductor voltage
value in non-ST state is equal to −99.5 V that is close to its obtained value from (32) which is equal to −100 V. Fig. 6*g* shows the capacitor voltage waveform. The average value of capacitor voltage obtained from (34) is equal to 250 V. This value verifies the obtained result from simulation. The obtained value from simulation is equal to 249 V. Fig. 6*h* shows the dc-link voltage waveform. On the basis of this figure, the dc-link voltage value in ST state is equal to zero and in non-ST state is in its maximum value that is equal to 249 V. This value has a small difference with the obtained value from (34) which is equal to 250 V. The output voltage and the current through the load are shown in Fig. 6*i*. According to this figure, the peak value of the output voltage is equal to 174.3 V. This value is close to obtained value from theoretical analysis which is equal to 175 V. As expected, the waveform of the output current has a phase difference with the output voltage.

4. Conclusion

In this paper, new topologies for Z-source inverter are proposed. In the proposed inverters, different operating modes are completely analysed and then the voltage gain, capacitor voltage ripple and inductor current ripple are calculated. It is also resulted that the required number of passive elements in the proposed switched-inductor inverter is lower than the conventional Z-source inverter. This advantage leads to reduce the size, weight and cost of the inverter. For instance, by considering $n = 1$, the number of used passive elements in the proposed inverter is half of the needed elements in the conventional Z-source inverter. Then, by using the switched-inductor cell the voltage gain value is increased in a way that in the proposed inverter by considering $n = 2$ and $D_{ST} = 0.25$, the voltage gain value is equal to 5, that is 2.5 times higher than this value in the conventional Z-source inverter. The obtained simulation results reconfirm the theoretical analysis and verify the correct performance of the inverter.

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