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DESIGN AND IMPLEMENTATION OF ALU AND PAL USING REVERSIBLE LOGIC GATES

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***Abstract*—The aim of this paper is to design and synthesize a Arithmatic Logic Unit (ALU) and Programmable array Logic (PAL) using reversible logic with minimum quantum cost. The PAL is a PLD which consists of programmable AND Gates and fixed OR gates array. The performance and reliability of digital systems which are now reversible logic gates, which pave for low power consumption and lesser quantum delays, thus increasing the speed of computation. The PAL is the PLD which contains programmable AND gate is trailed by fixed OR gate. The PLDs are the combinational circuits mainly used to realize Boolean functions on our interest. An n input and k output Boolean function f (a1, a2,a3, …., an) (referred as (n, k)) is said to be logically reversible if and only if, the number of inputs are equal to the number of outputs i.e., 'n' equals 'k' and the input pattern maps uniquely maps the output pattern. The reversible logic must run both forward and backward in such a way that the inputs can also be retrieved from outputs. There are many reversible logic gates in literature like NOT gate, Feynman Gate (CNOT gate),Double Feynman Gate, Peres Gate, TR gate, Seynman Gate and many more. Fan-out and Feed-back are not allowed in Logical Reversibility. To overcome the Fan out limitation, the signals from required output lines are duplicated to desired lines using additional reversible combinational circuits.Reversible Logic owns its applications in various fields whichinclude QuantumComputing, Optical Computing, Nanotechnology, Computer Graphics, low power VLSI etc.,Reversible logic is gaining its own importance in recent yearslargely due to its property of low power consumption and lowheat dissipation. In this paper, the design of ALU and PAL which has less heatdissipation and low power consumption isproposed. The designed circuits are analyzed in terms ofquantum cost, garbage outputs, number of constant inputs, number of gates used that is gate count and propagation delay Circuit has been designed and simulated using Xilinx 14.7 software.**

Keywords—Proposed reversible ALU design, reversible multiplier, reversible adder, reversible buffer, reversible xor, reversible xnor, reversible nand , PAL, PLDS, Quantum Cost, Reversible Gates, Garbage Outputs, Number of gates.

I. Introduction

In the past few decades, reversible logic has become one of the most promising research areas. In modern technologies, power dissipation is an important issue and overheating is a serious concern for both manufacturer and consumer. When information loss occurs, energy is also lost .It happens when an input cannot recover its output and it has been proved by Landauer [1]. He also expressed that, if a bit of information islost, then *KTln2* joules of heat generate ;Where *K* is Boltzman's Constant of1.38×10−23J/K and *T* is absolute temperature. To reduce energy waste, reversible circuit can be used and Bennet showed it [2]. Reversible logic follows one to one mapping system followed by input number and output number remains equal. Here no information loss and no energy dissipation occur. Miller proved that, if the number of gate increased, then it is not a good metric of optimization [3]. But reversible computing dissipates zero energy in terms of information loss and also it can detect errors of circuit by keeping unique input output mapping. circuits. Reversible Logic finds its own application in Quantum computing, Nano- technology, Optical computing, Computer graphics and Low Power VLSI. Ralf Launduer [1] told that heat dissipation in irreversible circuits is not because of the process involved in the operation, but it is due to the bits that were erased during the logical computation process. He demonstrated Launder's principle which describes the lower theoretical limit of heat dissipation in logical computation. Launder's principle states that losing a single information bit in the circuit causes the smallest amount of heat in the computation which is equal to KTln2 joules where K is Boltzmann constant (approximately $1.38\times10_{-23}$ J/K), T is Temperature and ln2 is natural algorithm of 2 (approximately 0.69315). The amount of heat dissipated in simple circuits is very small but it becomes large in the complex circuits. It is necessary to notice that there is a direct relationship between the number of information bits erased to the amount of heat dissipated in the circuit. Later in 1973 C. H. Bennett [2] described that the Power dissipation due to the bit loss can be overcome if each and every computation in circuit was carried out in reversible manner. Quantum networks are designed of quantum logic gates. As each gate perform a unitary operation, KTln2 Joules energy dissipation wouldn'toccur if the computation is carried out in reversible manner. He argued that for zero heat dissipation, the computation must be done in reversible manner. But if reversible logic is utilized to do logical computation, the heat dissipation will be less than KTln2 for one information bit in contrast to Launder. Thus computation done in reversible manner doesn't require erasing ofbits.

II. Concept

The Reversible Logic involves the use of Reversible Gates which consists of the same number of inputs and outputs i.e., there should be one to one mapping between input vector lines and output vector lines. In reversible computation [2], the reversible gates are made to run both forward and backward directions. If the device obeys abovetwo conditions, it satisfies the second law of thermodynamics which preserves the information bits without getting erased and guarantees that no heat is dissipated.Certain limitations are to be considered when designing circuits based on reversible logic (i) Fan out is not permitted in reversible logic and (ii) Feedback is also not permitted in reversible logic. In Reversible logic using outputs we can obtain full knowledge of inputs. To overcome the Fan-out limitation, by using additional reversible combinational circuits, the output lines are duplicated into required number of lines that are required to drive the inputs of consecutive device. Similarly for Feedback limitation delay elements are used.

Reversible logic conserves information. Some cost metrics [5][4] like Garbage outputs, Number of gates, Quantum cost, constant inputs are used to estimate the performance of reversible circuits. Garbage outputs are the extra outputs which help to make inputs and outputs equal in order to maintain reversibility. They are kept alone without performing any operations. Number of gates count is not a good metric since more number of gates can be taken together to form a new gate. Quantum Cost is the number of elementary or primitive gates needed to implement a reversible logic gate. It is nothing but the number of reversible gates (1×1 or 2×2) required to construct the circuit. The quantum cost plays an important role in logical reversibility. If the quantum cost is more, then the area of the circuit increases, thereby increasing the propagation delay. But quantum cost doesn't impact heat dissipation. Delay is one of the important cost metrics. A Reversible circuit design can be modeled as a sequence of discrete time slices and depth is summation of total time slices. In Digital Electronics the binary decoder is a combinational logic circuit that converts the binary integer value to the associated output pattern. Various proposals are given to design of combinational and sequential circuits in the undergoing research.

In this paper the design of Programmable Array Logic(PAL) and ALU using reversible logic with minimum Quantum cost is proposed and these circuits are implemented on Xilinx 14.7 software.

III. REVERSIBLE LOGIC GATES

The reversible logic gate consists of same number of inputs and outputs as shown in the figure1. The basic Reversible Logic Gates present in the literature are briefed below. The gates that are suitable for the design with optimum quantum cost can be selected.

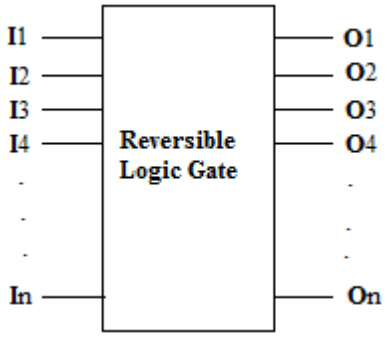
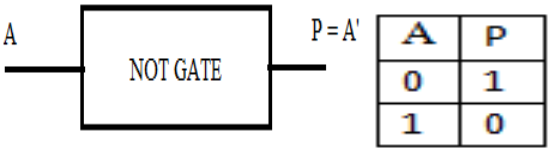


Fig.1 Simple reversible logic gate

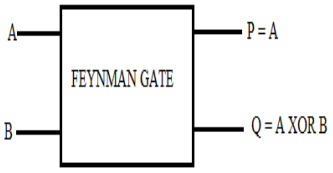
1. NOT GATE: The NOT GATE is the simple Reversible Logic gate. It is 1×1 Reversible Logic Gate with the quantum cost zero. The Not gate simply shifts the complementary of the input to output as shown in the figure2. It is the basic primitive gate which may involve in construction of reversible logic gate, thus owing its own importance in determining the quantum cost of designed Reversible logic gate.



A	P
0	1
1	0

Fig. 2 NOT Gate and its Truth Table

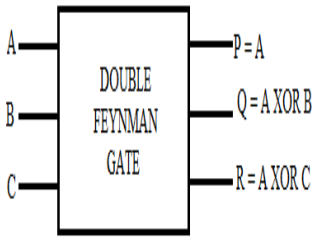
2. FEYNMAN GATE (FG): Feynman gate [4] is a 2×2 reversible gate as shown in below figure3. The Feynman ate is also called as CNOT gate i.e., controlled NOT gate. The eynman gate is used to duplicate of the required utputs since Fan-out is not allowed in reversible logic gates. The uantum Cost of FG is 1. This is also the primitive gate owing its importance in determining quantum cost metric.



A	B	P	R
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fig. 3 Feynman Gate and its Truth Table

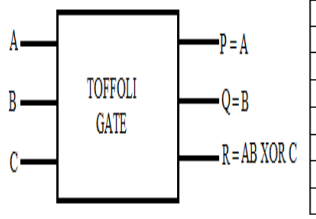
3. DOUBLE FEYNMAN GATE (F2G): Double Feynman Gate[4] is a 3×3 reversible gate. The outputs P, Q, R are defined as the functions of inputs as shown in the figure4. The quantumcost of F2G is 2. This gate can also be used for duplicatingoutputs.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Fig.4 Double Feynman Gate and its Truth Table

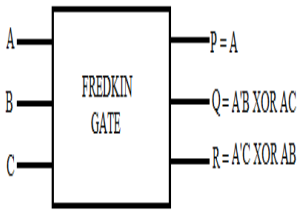
4. TOFFOLI GATE (TG): Toffoli Gate [8] is 3×3 reversiblegate. The outputs P, Q, R are defined as the functions of inputsas shown in the below figure5. The Quantum Cost of TG is 4.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Fig.5 Toffoli Gate and its Truth Table

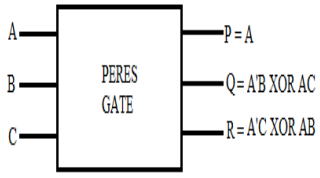
5. FREDKIN GATE (FRG): Fredkin Gate [12] is a 3×3 reversible gate. The outputs P, Q, R are defined as functions of inputs as shown in the below figure6. The Quantum Cost of FRG is 5. This paper mainly surrounds around Fredkin gate.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Fig.6 Fredkin Gate and its Truth Table

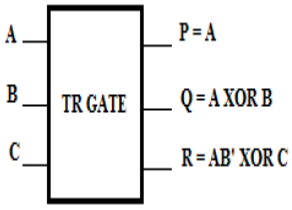
6. PERES GATE (PG): Peres Gate [5] is a 3×3 reversible gate. The outputs P, Q, R are defined as functions of inputs as shown in the below fig7. The Quantum Cost of PG is 4.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig.7 Peres Gate and its Truth Table

7. TR GATE: TR Gate [5] is a 3×3 reversible gate. The outputs P, Q, R are defined as functions of inputs as shown in the below figure8. The quantum cost of TRG gate is given by 4.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

Fig.8 TR Gate and its Truth Table

IV.EXISTING METHOD

The Design of Combinational circuits [6][9][16] and Sequential Circuits [10][11] using reversible logic has been ongoing in research. Various proposals are given for the design of combinational circuits like adders, subtractors, multiplexers, decoders etc., in the existing method the author has given a novel design of 4x16 decoder [15] whose Quantum Cost is less than the previous design. Replacing fredkin gates for designing 2×4 decoder with reversible gates like Peres gate, TR gate, NOT gate and CNOT gate are used. The whole design is done using Fredkin, CNOT, Peres gates which give better Quantum Cost when compared to the other reversible Logic gates. The number of gates required to design 4x16 decoder are 18 in which there are 12 fredkin gates, one peres gate, one TR gate, one NOT gate and 3 CNOT gates. The sum of all the quantum costs of each gate gives total quantum cost of 4x16 decoder. The sum of all the quantum costs of each gate used to design total circuit gives the quantum cost of total circuit.

PROGRAMMING ARRAY LOGIC

Main difference between PLA, PAL and ROM is their essential structure. In PLA, programmable AND gate is trailed by programmable OR gate. In PAL, programmable AND gate is trailed by fixed OR gate. In ROM, fixed AND gate array is trailed by programmable OR gate array. Depicting the PAL structure (programmable AND entryway followed by fixed OR gate).

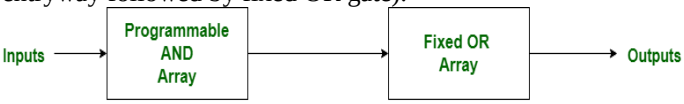


Fig.9 Basic model of PAL design

PALs were not the main business programmable logic gadgets; Signetics had been selling its field programmable logic array (FPLA) since 1975. These gadgets were totally new to most circuit designers and were seen to be too hard to even consider using. The FPLA had a moderately moderate most extreme working speed (due to having both programmable AND and programmable-OR arrays), was costly, and had gained reputation for testability. Another factor restricting the acknowledgment of the FPLA was the large package, a 600-mil (0.6", or 15.24 mm) wide 28-pin dual in-line package(DIP).

X=A'B+AC
Y=A'B+B'C
Z = A'B + A'C + AB'C

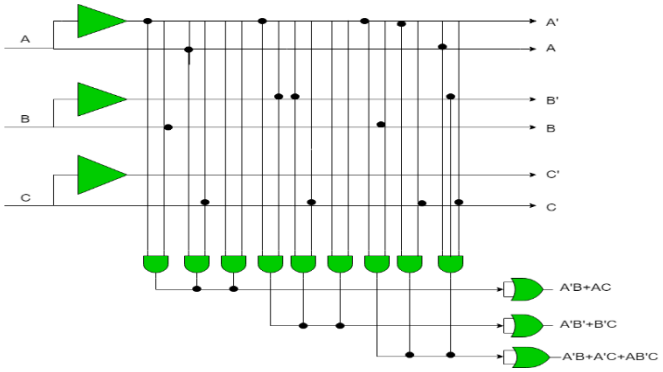


Fig.10 Logic diagram of SOP functions

Table 2 Truth table to finding X, Y, Z

A	B	C	X	Y	Z
0	0	0	0	1	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	1	0	1
1	0	0	0	0	0
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	1	0	0

Realize the given function by using PAL; any form from sum of product (SOP) form or product of sum (POS) can be used for realization of a Boolean function. There are three inputs A, B, C and three functions X, Y, Z. Using sum of product (SOP) terms to express the given function as follows. Following Truth table will be helpful in understanding function on number of inputs

Arithmetic And Logic Unit (ALU)

REVERSABLE ADDER SUBTRACTOR:

The Half and Full Adder/Subtractor Designs are used to create Reversible eight-piece Parallel Binary Adder/Subtractor is showed up in the Figure 11. The ctrl input is used to isolate eight-piece addition and subtraction limits. The two eight-piece twofold numbers are A0 to A7 and B0 to B7. Convey/Borrow is gotten after Addition/Subtraction is addressed by C_B1 to C_B7. The yields Sum/Difference and Carry are showed up as S_D0 to S_D7 and C_B8 exclusively. The execution requires seven Full Adder/Subtractor units and one half Adder/Subtractor units in which first stage is half Adder/Subtractor

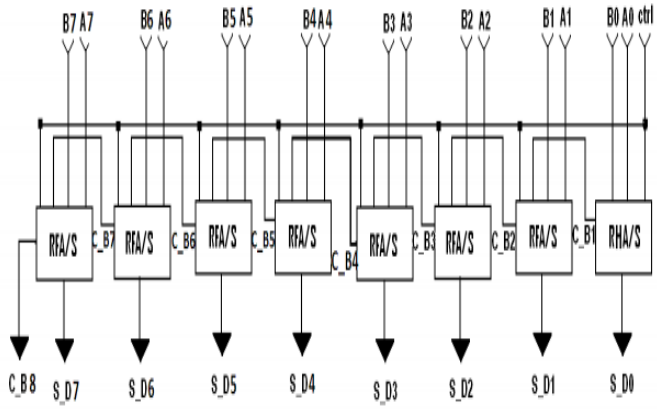


Fig 11 **Reversible Eight-bit parallel Binary Full Adder/Subtractor**

Array Multiplier in Digital Logic

An array multiplier is an digital combinational circuit utilized for multiplying two binary numbers by utilizing a variety of full adders and half adders. This exhibit is utilized for the almost simultaneous addition of the different item terms included. To shape the different item terms, a variety of and gates is utilized before the adder array [14].

b1 b0
a1 a0
---
a0b1 a0b0
a1b1 a1b0
---
c3 c2 c1 c0

Assuming A = a1a0 and B= b1b0, the various bits of the final product term P can be written as:-
1.P(0)=a0b0
2.P(1)=a1b0+b1a0
3. P(2) = a1b1 + c1 where c1 is the carry generated during the addition for the P(1) term.
4. P(3) = c2 where c2 is the carry generated during the addition for the P(2) term.

V.PROPOSED METHOD

The Programmable Array Logic (PAL) is realized using reversible Fredkin gate and Feynman gate as shown in the fig6 and fig3 respectively. The concept of duplicating a single output to required number of outputs using Feynman gate is introduced where Fan-out was not allowed in reversible computation. The standard

irreversible conventional PLDs can be programmed only once [11].

The irreversible PLDs consist of a series of fuses which can be burned to program the device. By burning the fuses the chip can be programmed which is an irreversible process [12]. In reversible PLDs structure, the fuses are replaced with a reversible fuse which is made of reversible Feynman gate and fredkin gate as shown below.The Feynman reversible gate acts as a duplicating circuit. It duplicates the output line into two output lines out of which one output line drives the next circuit and the other drives the second input of 2×1 reversible multiplexer [13]. The first input of reversible multiplexer is grounded so that when the enable signal 'E' is low it acts as an 'off' switch. The reversible multiplexer is made of Fredkin gate as shown below.

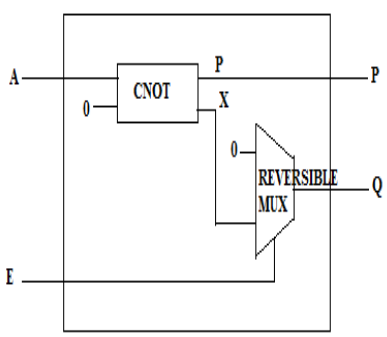


Fig.12(a) Reversible Fuse

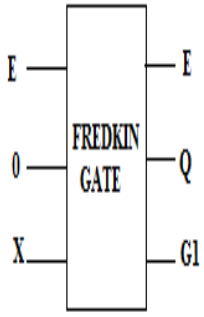


Fig.12 (b) Reversible MUX

The fixed connections are replaced by CNOT gates in which the second input is set to '0' always. The CNOT gates give solution for two remedies. It overcomes the feedback limitation and it acts as a fixed connection. The Design of PAL made of reversible logic which is programmed to perform
the operation of the below Boolean algebraic equations is shown in the below figure13. The PAL consists of fixed ORgates array and programmable AND gate array.

F1 = I[1]I[2] + I[1]I[3]' + I[1]'I[2]'I[3]…… Eqn (1)
F2 = I[1]I[2] + I[1]'I[2]'I[3] + I[1]I[3] ……..Eqn (2)
F3 = I[1]I[3]' + I[1]I[2]I[3] …….…… Eqn (3)
Contemporary to irreversible PAL, the fuses are replaced with programmable reversible fuses and the fixed connections are replaced with the CNOT gates as shown in the figure13.The 'P' output of fuse drives the subsequent fuse and the 'Q' output of fuse drives the input of AND gate as shown in figure12 (b). The output of AND gate drives the fixed connections i.e., CNOT gate. The 'P' output of CNOT gate drives the next fixed connection and the 'Q' output of CNOT drives the inputof OR gate.

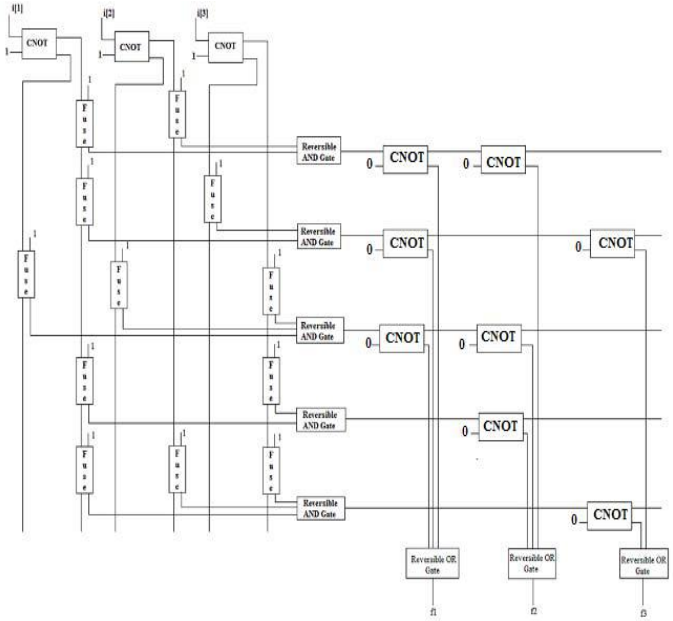


Fig.13 Circuit diagram of Reversible PAL to perform Boolean algebraic equations operation.

The OR Gates and AND gates used in PLDs are made of Reversible logic. The 'n' input OR gate consists of 'n' number of inputs. If any inputs are kept ideal without use they are to be driven with ground (binary value '0') so that the high impedance value is not driven to OR gate which effects the operation of OR gate. The fuses left without programming drives the value zero to the reversible OR gate which doesn't affect the operation of OR gate. Contrast to OR gate, for AND gate the left out inputs are driven with HIGH signal so that the operation of AND gate is not affected. The circuit diagram of a Programmable Logic Array constructed using reversible logic to program Boolean equations Eqn (1), Eqn (2), Eqn (3) is shown in the above figure15. In both the AND gate array and OR gate arrays are programmable. Hence reversible fuses are used to program the AND gate array and OR gate array of the device as shown in the figure12.

Proposed Methodology Of ALU

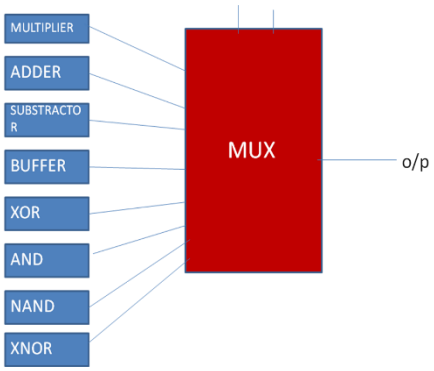


Fig. 15: Proposed single line diagram of reversible ALU

The proposed reversible ALU is design using MUX as shown in figure15 which performs the arithmetic and logic operations. The first block of ALU performs 8 operations

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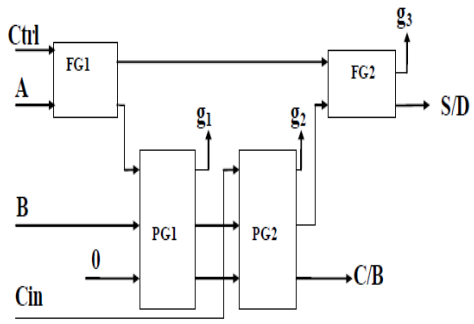

Fig:16 Full adder and subtractor

The Reversible Full Adder/Subtractor consists of two FG, two PG gates, and their interconnections are shown in the below Fig.The three inputs are A, B, and Cin, the outputs are S/D and C/B. For Ctrl value zero the circuit performs addition and Subtraction for Ctrl value one. The numbers of Garbage inputs are 1 represented by logical zero. The Garbage outputs are 3 represented by g1 to g3. The Quantum Cost for the design is 10

VI. SIMULATION RESULTS OF PROPOSED CIRCUITS

1. SIMULATION PROCESS AND RESULTS OF ALU

In this design, the control unit is constructed using a Feynman gate, a 4*4 Toffoli gate, and two Fredkin gates. HNG gate is used asthe full adder unit. The ALU shows the outputs separetly for adder/Substractor , multipiler and remaining all other ALU operation in single output as followes as

Fig 17: Output for Multiplier

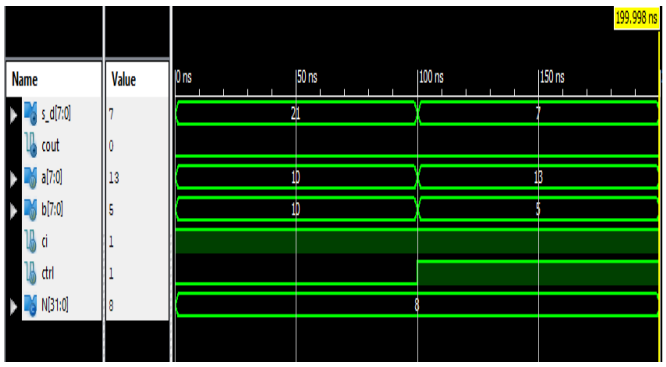

Fig 18 :Output for arithimatic opration Adder /Substractor

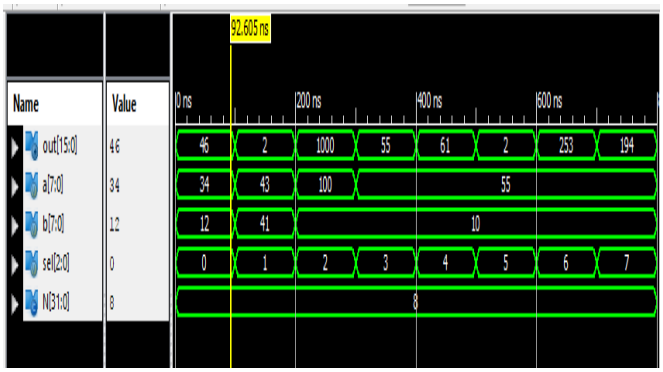

Fig19 : Output for logical opreations (and,or,b uffer,xor,nand,xnor)

2. REVESIBLE PROGRAMMABLE ARRAY LOGIC

The equations Eqn 1 to Eqn 3 are implemented using reversible PAL. The RTL schematic and simulated output for Eqn1 to Eqn3 implemented using reversible PAL is shown in the figure20.

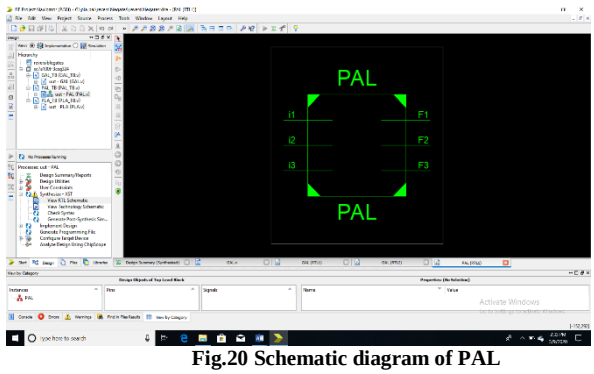

Fig.20 Schematic diagram of PAL

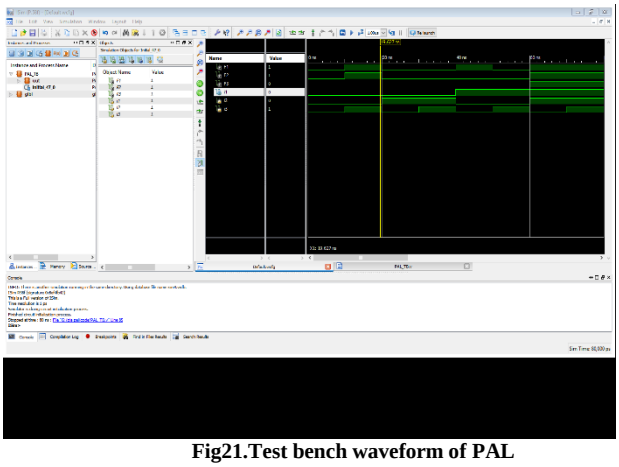

Fig21.Test bench waveform of PAL

The simulated output will be same for all the three devices, which gives clear assistance that the circuits are operating with genuine performance.

VII. CONCLUSION

In this paper, the method of realizing different Boolean functions using reversible ALU reversible PALare explained. These circuits are designed for minimum quantum cost and minimum garbage outputs. To overcome the fan-out limitation in reversible logic circuits

the concept of duplicating the single output to required number of output lines is implemented by using additional reversible combinational circuits. By using reversible logic gates we are implemented using a reversible fuse and fredkin gate. The reversible fuse is made of CNOT gate and fredkin gate which is used for programmable connections. Feynman gate with second input made zero is used for fixed connections. The reversible circuits used for designing programmable connections and fixed connections give minimum heat dissipation. By using this reversible PLDs eighty percentage of efficiency can be acquired in terms of heat dissipation. The time delay increases a little when compared to irreversible PLDs which can be termed as a disadvantage but it is negligible. The time delays for reversible PAL and ALU are 5.847nsec, 10.52nsec respectively. The time delay depends upon the Boolean expressions considered to program on the device. The time delay is the function of quantum cost. The quantum cost increases with increase in length of Boolean function, because the number of programmable reversible fuses and Fredkingates (fixed connectors) increases with increase in length of Boolean function. If quantum cost increases, the time delay also increases. The reversible PAL and ALU finds moreadvantages when compared to the reversible PAL and PROM,since both OR array and AND array are programmable. Because of using reversible decoder in PROM the quantum cost becomes less when compared to the remaining PLDs. The propagation delay can be reduced if the quantum cost of the circuit is reduced further more. This can be termed as future scope for this paper.

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