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MODELING AND SIMULATION OF FREQUENCY SYNTHESIZER BASED ON PHASE LOCKED LOOP FOR RF APPLICATIONS

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Abstract **- A low phase noise and fast frequency synthesizer based on phase-locked loop (PLL) is presented. The proposed circuit is designed using Cadence tool and simulated in UMC_18_CMOS, 180nm process with 1.8V supply. Main focus of this design is to achieve lower phase noise and less power consumption with less locking time. In Proposed design, VCO is realized using dual-delay path technique. The simulation results are presented with frequency range of 2.3 to 4.7 GHz. The locking time of frequency synthesizer is 300ns and Power consumption is 12.8 mW with phase noise of -109dBc/Hz at an offset of 1MHz. These simulation results are than back annotated to the behavior model and accurate model in Verilog-A has been presented.**

Keywords: Charge Pump, Frequency Synthesizer, Jitter, Loop Filter, Phase locked loop, Phase Noise, Voltage Control Oscillator.

1. INTRODUCTION

The present and future trend for electronic systems is the portability. This has make necessary to design the integrated circuits with more restricted specifications. It is also desirable to integrate analog and digital systems into the same chip. To accomplish this goal it is necessary to use advanced technologies and design techniques, as well as to process the signals in a more efficient fashion. For instance, in many communication systems it is necessary to generate a signal with intermediate frequency to translate high frequency signals to a frequency range where they are processed easier. The translation operation is necessary because if the signal processing were done in the high frequency domain (as the signals in the reception block) it would be very difficult to design the circuits capable to process the signal at that frequency and the power consumption would be enormous. Frequency translation can be achieved by the mixing operation between a high frequency signal and the signal generated in the system. The block generating the mixing signal in these systems is the Frequency Synthesizer (FS). A FS is a system that generates one or many frequency ranges using a single reference frequency [1]. FS have become an integral part of advanced communication systems in general and wireless communication systems in particular. FS are found applications in a variety of items like all types of wireless products to radio frequency equipment like spectrum analyzers and signal generators. FS offer high levels of stability and accuracy [2-3]. Phase FS using Phase Locked Loop (PLL) has many advantages over other

forms of oscillators. PLL frequency synthesizers (PLL-FS) are commonly used in all types of radio communications equipment nowadays. PLL-FS found in the most demanding satellite communication terminals as well as in most sophisticated radar systems [4] or in high speed data communication systems [5]. Now a days, the CMOS PLL circuits are widely used in digital and analog circuits in applications such as the cellular phones, microprocessors, RF front-end circuits and system-on-chip (SOC) implementations because of better performance on low power and low noise [6-8]. Other criteria such as the lock-in time, phase error and power consumption are also considered in a PLL-FS design.

The indirect frequency synthesizer using the PLL configuration [1] is the best way to generate a signal in an integrated circuit having the most stringent characteristics. The PLL configuration consist on a Voltage Controlled Oscillator (VCO), Phase Frequency Detector(PFD), Frequency Divider (FD), Low Pass Filter (LP) and Charge-Pump(CP); all of them arranged in a closed loop, shown in Fig. 1. PFD and CP generate current pulses which represent the phase difference between signals coming from reference and from FD. The current pulses are low pass filtered and filter's output tunes the VCO.

The signal at the VCO's output is divided by N to compare it latter to the reference signal and close the loop. In this architecture the generated signal has frequency that is entire multiple of reference frequency.

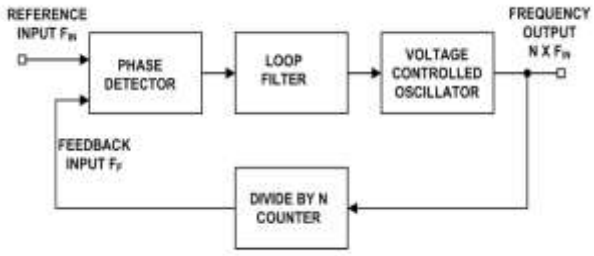

Fig. 1 : PLL based frequency synthesizer.

VCO and the FD are the blocks working at high frequency so they not only impose the output frequency limit, but also they are the most power consuming elements in the synthesizer. Every block in the loop adds noise to the synthesizer which degrades the output signal.

2. PHASE NOISE AND TIME JITTER

In order to properly design a Frequency Synthesizer with a PLL configuration, it is necessary to fully understand all the noise sources in the circuits building it. Phase noise is phase fluctuation because of random frequency variation. The purity of a periodic signal is the characteristic describing how much this signal deviates from the ideal representation as shown in fig 2. The goal of a frequency synthesizer is to generate a pure periodic signal to avoid the corrupted information. Nevertheless, noise sources in the blocks of frequency synthesizer make the output signal to change arbitrarily the phase so the noise sources affect the output signal's spectral purity. This can be measured as Phase Noise or as Jitter in the output signal. In PLL based frequency synthesizer VCO, PFD and FD are main contributor of phase noise. Phase noise also known as jitter in time domain. Jitter describes how far the signal period has wandered from its ideal value as shown in Fig. 2.

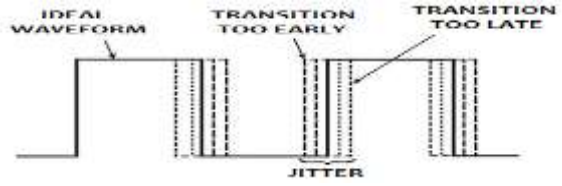

Fig. 2 : Jitter as the clock phase shifted from its expected position

In Fig. 2 solid line shows the ideal position of the clock and departure from this is known as jitter.

Phase modulated signal with the phase modulation term as a single tone is

$$x_{pm}(t) = \mathrm{A}\cos\left(\omega_o t + A_\theta \cos(\omega_m t)\right) \qquad (1)$$

For the case $A_\theta \ll 1$ the signal can be expressed

$$x_{pm}(t) \approx \mathrm{A}\cos(\omega_o t) + \frac{AA_\theta}{2}\left[cos\left((\omega_o - \omega_m)t\right) + cos\left((\omega_o + \omega_m)t\right)\right] \qquad (2)$$

In the frequency domain this phase modulation term adds two harmonics at a frequency $\omega_o \pm \omega_m$

(as shown in fig 3 b). If the phase modulation term contains more harmonics, the spectrum of a pure sinusoidal signal changes from a Dirac delta to the one shown in fig 3 c).

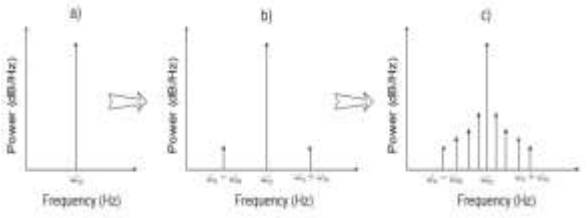

Fig. 3: Power spectrum degradation due to phase modulation terms.

Theoretically, if infinite phase modulation terms are added, power spectral density of the modulated signal takes form shown in Fig. 4. In fact, the noise which generates the phase disturbances can be modeled as an infinite number of phase components. From the last point of view, it can be said that the skirt shaped spectrum in Fig. 4, it is a measure of how the phase, and though the instantaneous frequency, is changed randomly. As this skirt shaped spectrum of a noise sinusoidal signal can be represented as phase fluctuations, it has received the characteristic name of *Phase-Noise*.

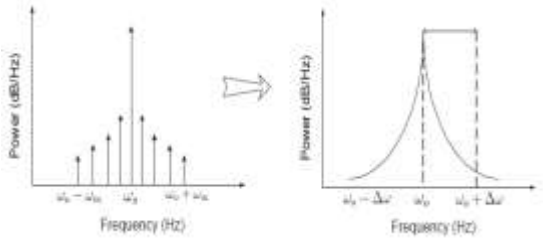

Fig. 4 : Power spectral density of a noisy sinusoidal signal.

Too much jitter and phase noise can create problem in communication signal by increase in bit error rate (BER). Several sources induced Jitter onto a clock signal and is not uniform over all frequencies. Thermal and 1/f or flicker noises are major source of phase noise or jitter. Phase noise and jitter degrades the performance and accuracy of the data transmission system

2.1 THERMAL NOISE

Thermal noise is a result of random thermal motion of charge carriers. This thermal motion results in random currents and voltage drops that can be seen when measuring a signal. In a resistor R at temperature T the mean squared voltage and current density of the noise can be calculated as:

$$\frac{\partial(v^2_{therm,res})}{\partial f}(f) = 4k_BTR \quad (3)$$

$$\frac{\partial(i^2_{therm,res})}{\partial f}(f) = \frac{4k_BT}{R} \quad (4)$$

where k_B is the Boltzmann constant.

Transistors also show this random thermal motion of charge carriers. it can either be modeled as a current source in parallel to the drain-source channel or a voltage source at the gate terminal as shown in Fig. 5

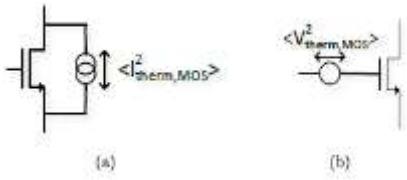

Fig.5: MOSFET noise modeled as
a) current source, b) voltage source

This stems from the fact, that the current flowing through the transistor is related to the voltage on the gate. Thus, these two methods are equivalent. The corresponding equations are given by :

$$\frac{\partial(v^2_{therm,MOS})}{\partial f}(f) = \frac{4k_BT\gamma}{g_m} \quad (5)$$

$$\frac{\partial(i^2_{therm,MOS})}{\partial f}(f) = 4k_BT\gamma g_m \quad (6)$$

The γ-factor depends on the technology used. For long transistors, L > 250 nm in 180 nm technologies, it is about 2/3. For shorter transistors (L < 250 nm in 180 nm technology) this factor increases.

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2.2 FLICKER NOISE

Noise in the low frequency regions is dominated by flicker noise. Its origin is still under investigation. One model - the charge carrier density fluctuation model - suggests that flicker noise stems from charge carriers being trapped and released. At the silicon bulk's surface underneath the gate oxide, the abrupt transition from bulk to oxide causes new energy states to appear. Charge carriers can get trapped here which stops them from contributing to the current flow until they are released again.

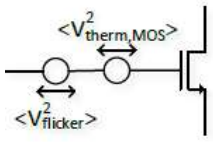

Fig. 6: MOSFET thermal and flicker noise contributions modeled as voltage sources in series at the gate.

This process of trapping and releasing causes fluctuations (noise) in the current flow through the conducting channel. Usually, this noise contribution is modeled by a voltage source at the gate as shown in Fig. 6. Its voltage spectral density can be calculated as:

$$\frac{\partial\left(v_{flicker}^2\right)}{\partial f}(f) = \frac{K}{C_{ox} W L}\frac{1}{f} \qquad (7)$$

2.3 NOISE IN DIFFERENTIAL PAIRS

Fig. 7 (a) shows the equivalent circuit of a differential pair with biased load transistors including thermal noise sources.

In order to keep the calculations simple, only thermal noise is taken into account. It can be proven that the noise spectral voltage density of a differential pair is twice the noise of a single stage common source amplifier as long as both sides are symmetric. Due to this, the following considerations will concentrate on the circuit shown in Fig. 7. The noise currents $I_{n1} = g_{m,1} V_{n,1}$ and $I_{n3} = g_{m,3} V_{n,3}$ generated in the transistors cause voltage drops on the transistor output resistances $r_{out,1}$ and $r_{out,3}$.

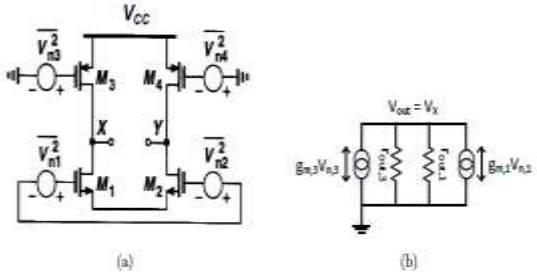

Fig. 7: a) Differential pair with load transistors and noise sources b) Equivalent small signal model for the left branch

In small signal calculations, constant voltages are set to ground which is why $r_{out,1}$ and $r_{out,3}$ act as parallel resistors to ground. Since the noise sources in the transistors are uncorrelated, their effect on the output voltage can be examined separately. Subsequently, Kirchhoff's current laws lead to the equations:

$$g_{m,1}^2 \frac{\partial(V_{n,1}^2)}{\partial f} = \frac{\partial(V_{out,M1}^2)/\partial f}{r_t^2} \qquad (8)$$

$$g_{m,3}^2 \frac{\partial(V_{n,3}^2)}{\partial f} = \frac{\partial(V_{out,M3}^2)/\partial f}{r_t^2} \qquad (9)$$

with $r_t = r_{out,1} \parallel r_{out,3}$. Here, $V_{out,M1}$ denotes the effect of the noise of transistor M1 on the output voltage. Solving for $V_{out,M1}$ yields:

$$\frac{\partial(V_{out,M1}^2)}{\partial f} = g_{m,1}^2 r_t^2 \frac{\partial(V_{n,1}^2)}{\partial x} \qquad (10)$$

$$\frac{\partial(V_{out,M3}^2)}{\partial f} = g_{m,3}^2 r_t^2 \frac{\partial(V_{n,3}^2)}{\partial x} \qquad (11)$$

The total output noise is then calculated by:

$$\frac{\partial V_{out}^2}{\partial y} = \frac{\partial V_{out,M1}^2}{\partial y} + \frac{\partial V_{out,M3}^2}{\partial y} = 4k_B T\gamma(g_{m,1} + g_{m,3})r_t^2 \qquad (12)$$

In order to compare the noise generated by an amplifier to that of other amplifiers, one has to

refer the output noise to the input. In short: Equation 12 has to be divided by the square of the amplifier's gain (= $g^2_{m1}r_{ll}$), the result is the input-referred voltage noise for one side of the differential pair:

$$\frac{\partial(V^2_{in,ref,cs})}{\partial f} = \frac{4k_BT\gamma}{g_{m,1}}\left(1+\frac{g_{m,3}}{g_{m,1}}\right) \quad (13)$$

Subsequently, the total input-referred voltage noise for a differential pair with the same loads is:

$$\frac{\partial(V^2_{in,ref})}{\partial f} = \frac{8k_BT\gamma}{g_{m,1}}\left(1+\frac{g_{m,3}}{g_{m,1}}\right) \quad (14)$$

This equation shows that in order to get low noise, the input transistors need to have a big transconductance $g_{m,1}$ while the load transconductance $g_{m,3}$ has to remain small.

3. DESIGN AND SIMULATION

3.1 PHASE FREQUENCY DETECTOR, CHARGE PUMP AND LOOP FILTER

PFD compares two input analog signals in terms of both frequency and phase and produces their difference as a digital output voltage. PFD build by two controllable D flip-flops and a AND gate is shown in Fig. 8. Fig. 9 shows the case when input reference clock has different phase but the same frequency with VCO output clock. When rising edge of input clock is leading the VCO output clock, the UP signal will turn on but in case when input clock rising edges and VCO output clock overlap, the DN signal only has positive pulses. This causes to dump charge in to the loop filter capacitor and hence increases in V_{ctr}l as shown in Fig. 12 is given by:

$$\Delta V_{ctrl} = \frac{I_{cp}}{C_1}.\frac{\phi_e}{2\pi}.\mathrm{T} \quad (15)$$

Average charge pumped in to the loop filter is

$$Q_{ctrl} = \frac{C_1.\Delta V_{ctrl}}{T} = I_{cp}.\frac{\Phi_e}{2\pi} \quad (16)$$

When the input clock is lagging the VCO output clock, the DN signal will turned on and the UP signal will have low level except has positive pulses while rising edges of VCO output and input reference clock overlap. The input clock is always leading VCO output clock; therefore DN is always low level with narrow spurs.

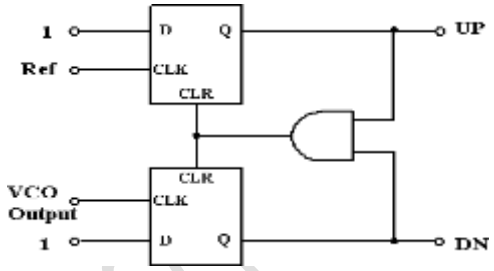

Fig. 8. : Phase frequency detector

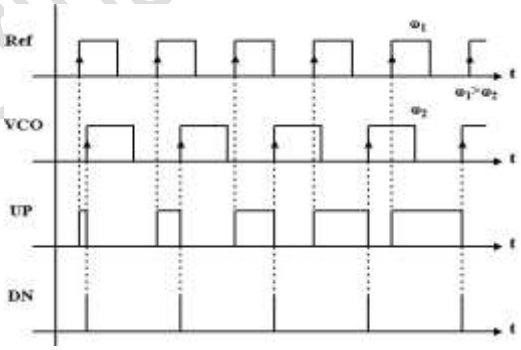

Fig. 9. : PFD outputs with a different frequency inputs.

CP generally consists of set of current sources that are switched on and off according to UP and DOWN signals from PFD. Equivalent circuit of CP and LP is shown in Fig. 10. CP is fed from the output of PFD. Whenever UP signal from PFD goes high, switch S_1 will turn on result in charging of filter capacitor C1, which causes increase of output voltage. C_2 is used to eliminate higher order noises from the PFD. On the other hand, when PFD output DN goes high, switchS_2 will turn on and charge pump is working in discharging mode. The current flowing in loop filter will decrease and result in decrease in output voltage. This output voltage is used to regulate VCO output frequency.

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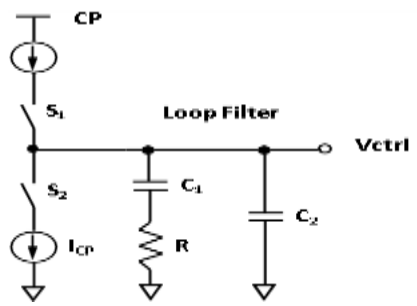

Fig. 10. : A passive loop filters following the charge pump.

Transfer function of loop filter is-

$$F(s) = \frac{s+\frac{1}{RC_1}}{C_2 s(s+\frac{C_1+C_2}{RC_1C_2})} \quad (17)$$

Fig. 11 shows the schematic of PFD with CP and LP. Two pulse sources are connected to PFD and output of this PFD are up and down signals which are fed to the CP. Output of the CP then filtered through LPF.

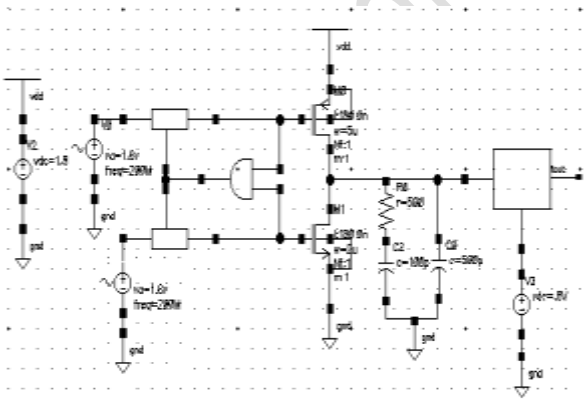

Fig. 11. : Schematic of Phase Frequency Detector with charge pump and loop Filter

Fig. 12 shows simulation results of PFD, CP and LPF when F_{ref} clock edge leads F_{fed} clock edge.

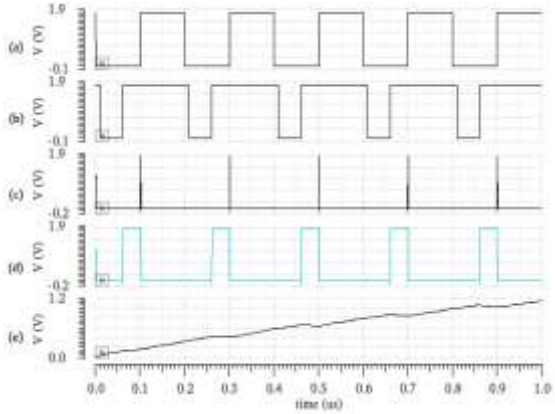

Fig. 12. : Simulation results of (a), and (b) inputs to the PFD, (c) up signals from PFD, (d) down signal (e) output of loop filter with PFD

3.2 VOLTAGE CONTROLLED OSCILLATOR

A VCO is a circuit whose output is periodic time varying signal having a semi-square or close to sinusoidal shape. The CMOS circuit bandwidth-limitations and the non-linear behavior for most VCO architectures make too much common the close-to-sine wave signal. The VCO is a feedback circuit whose closed loop transfer function makes possible to amplify its own noise in a controlled form up to a stable oscillation state. The VCO can be modeled as a two port network H(s) fed back with G(s) as shown in Fig. 13.

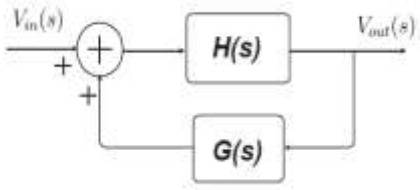

Fig. 13. : VCO feedback

The closed loop transfer function is given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{H(s)}{1-G(s)H(s)} \quad (18)$$

The circuit oscillates when the denominator of this transfer function is zero and the open loop gain is enough to maintain poles in the imaginary axis of

the root-locus plane. The situation can be resumed in the Barkhausen's criteria.

$$|G(j\omega_o) \| H(j\omega_o)| = 1$$

$$\angle\big(G(j\omega_o)\big) + \angle(H(j\omega_o)) = 0 \qquad (19)$$

There are several techniques to reach the Barkhausen's criteria in a CMOS circuit. The feedback of active circuits such as ring oscillators is one of them. In order to reduce noise in VCO, parasitic resistance must be as low as possible and the cross coupled pair trans-conductance must be high. Therefore, at a first glance the NMOS topology can be a good choice. The flicker noise contribution is much more significant at low frequencies. To reduce flicker noise contribution of PMOS differential pair is preferred. Besides the PMOS transistors have a better behavior for the trans-conductance degradation factor. With this encountered design consideration the election of the cross coupled VCO depends on the process used for the design and also the frequency tuning range can be crucial on this task.VCO and its output response is shown in Fig. 14.

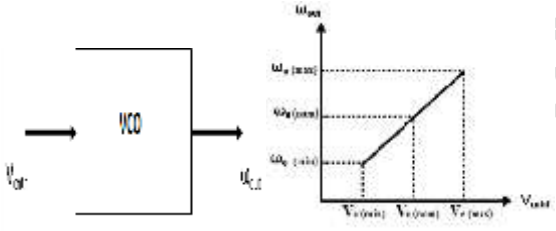

Fig. 14. : VCO and its response

The output frequency ω_{osc} can be expressed as:

$$\omega_{osc} = \omega_o + K_{vco} * V_{ctrl} \qquad (20)$$

Where, V_{ctrl} is a control voltage form CP, K_{vco} is gain or sensitivity of VCO and ω_o is a free running frequency. Mathematically the output of VCO is [9]:

$$V_{out}(t) = A * \sin(2 * phi * \int(\omega_{osc}\, t)dt) + V_{offset} \qquad (21)$$

where A and V_{offset} is amplitude and offset voltage respectively.

Fig. 16 shows a ring VCO with cascade four stages delay cells. Normal delay path and negative twisted delay path used to attach the delay cells has been used. Proposed delay cell of VCO is shown in Fig. 15 in which both outputs out- and out+ of one cell are connected to inputs Vin+ and Vin- of subsequent stage, this connection builds normal delay path. Now secondary inputs Vin2+ and Vin2- are coupled to inputs of second subsequent stage, this connection builds skewed delay. This advance signal turns on PMOS during the change in output and balance the performance of PMOS. This correction improves the rise time of the output and resulting in reduction of phase noise of the overall VCO This design has reduced number of stages with increase in frequency of operation. Fig. 17 shows the output of VCO for different control voltages.

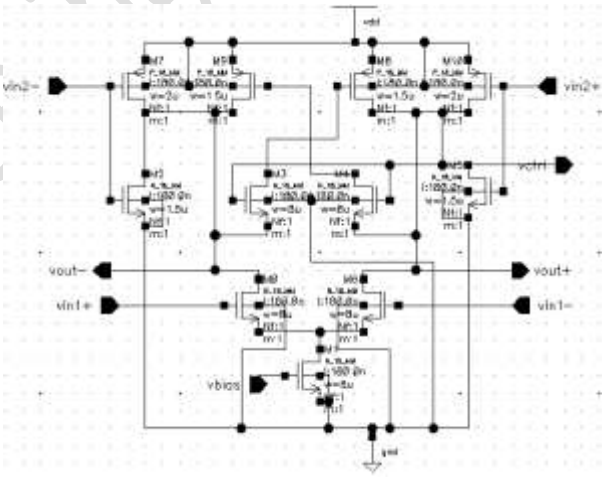

Fig. 15. Single differential cell of VCO

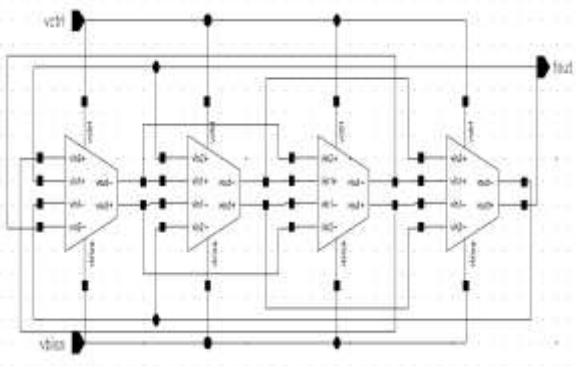

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Fig. 16. : Schematic Diagram of 4 stage Ring VCO

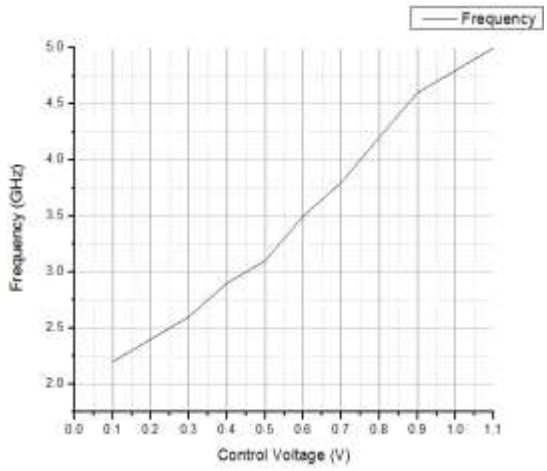

Fig.17. : Frequency range for different control voltage of Schematic

The frequencies at output for different control voltages are given in the Table I.

Table I : Control voltage versus output frequency of VCO

Control voltage (V_{ctrl})	Output frequency (f_{out})
0.2	2.3
0.3	2.5
0.4	2.7
0.5	3
0.6	3.5
0.7	3.7
0.8	4
0.9	4.5
1	4.7

3.3 FREQUENCY DIVIDER

Dividers come into play when the PLL is used as a frequency synthesizer. It converts high output frequency created by the VCO, in to lower. Dividers are usually built from a cascade of flip-flops (RS, JK or toggle). Fig. 18 shows a single D flip flop which divides frequency of input signal by 2.

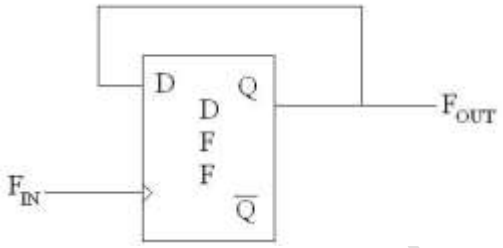

Fig.18. : Divide-by-2 frequency divider.

This block takes an input signal with a frequency f_{in} and divides it down to a lower frequency f_{FD}. The division factor N is given by an integer such that:

$$f_{FD} = \frac{f_{in}}{N} \quad (22)$$

P_{PFD} compares f_{fref} to the decease frequency f_{FD}. As a result the PLL will try to lock its VCO to a frequency N times larger than the reference frequency

$$f_{VCO} = N f_{ref} \quad (23)$$

Fig. 19 shows schematic of D flip flop used in divider circuit. We have used Divide-by-4 circuit for frequency synthesizer. Fig. 20 shows simulation results of divider circuit.

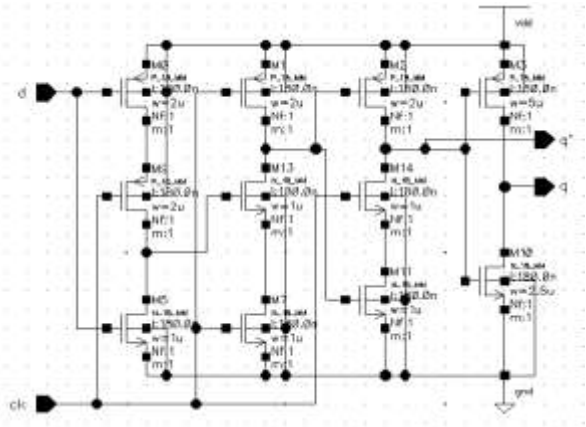

Fig.19. : Schematic of D Flip-Flop for Divider circuit

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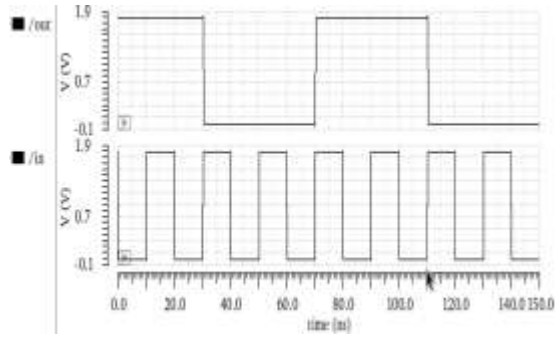

Fig. 20. : Output of divide-by-4 circuit

3.4. PHASE LOCKED LOOP BASED FREQUENCY SYNTHESIZER

Fig. 21 shows complete phase locked loop based frequency synthesizer schematic at supply voltage of 1.8V. Fig. 22 shows input and output of individual blocks when PFD fed externally. Control voltage in lock state shown in fig 23, PLL-FS get locked in 300ns. Fig. 24 shows the phase noise performance of PLL-FS. Layout of proposed PLL-FS is shown in Fig. 25. Comparison of performance parameter with other work is given in table II.

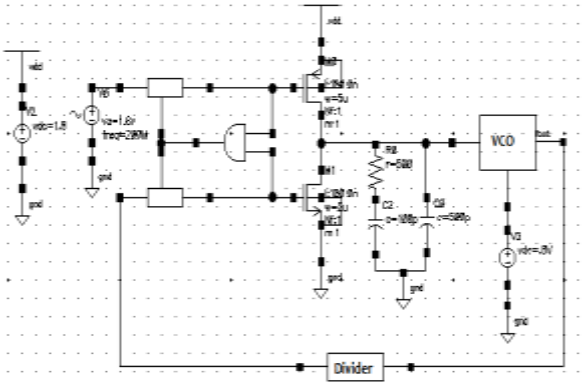

Fig. 21. : Schematic of PLL

$$H_{closed} = \frac{(R_1C_1+1)\left[I_{cp}K_{VCO}/2\pi C_1\right]}{s^2+\frac{(I_{cp}K_{VCO}R_1)s}{2\pi}+\frac{I_{cp}K_{VCO}}{2\pi C_1}} \qquad (24)$$

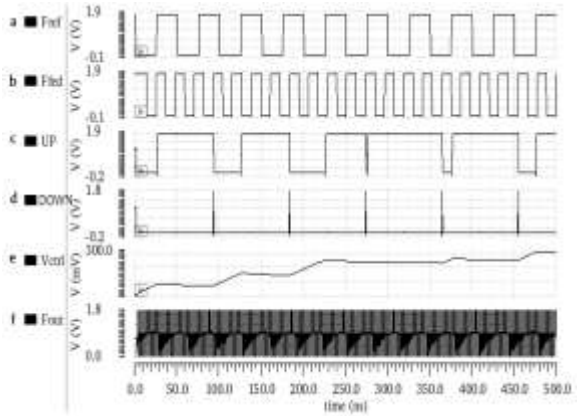

Fig. 22. : Simulation results of (a) and (b) inputs to the PFD, (c) up signals from PFD, (d) down signal (e) control voltage (f) Fout, output of VCO

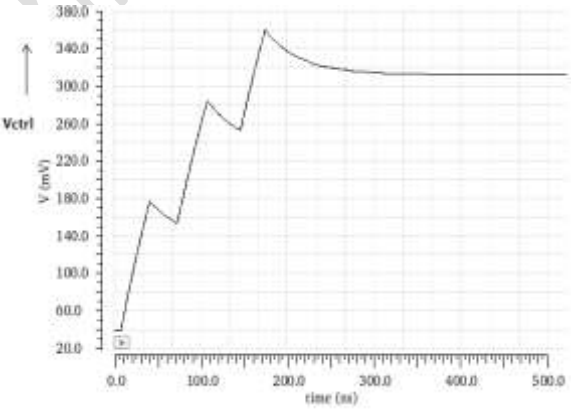

Fig. 23. : control voltage in lock state.

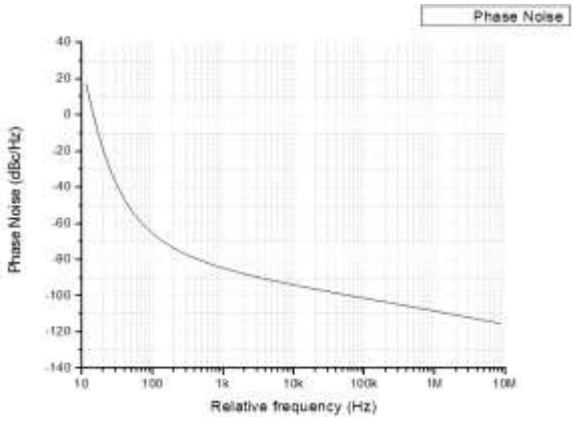

Fig. 24. : Phase Noise analysis of PLL

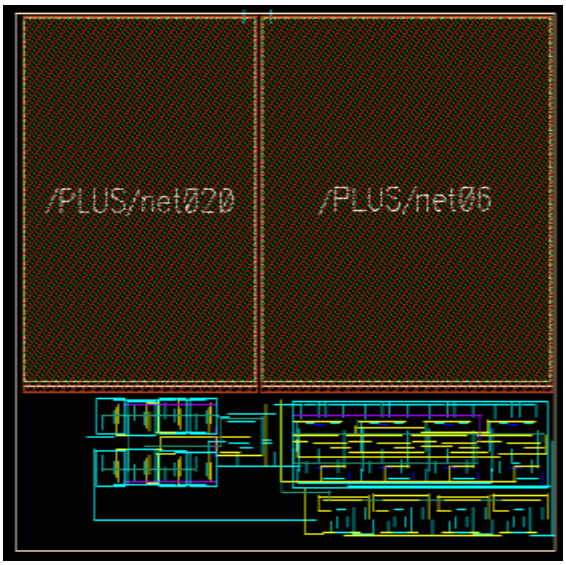

Fig. 25. : Layout of the complete frequency synthesizer circuit

Performance parameter	Proposed design	[10]
Technology	180nm CMOS	180nm CMOS
Supply voltage (V)	1.8	1.8
VCO	Ring	Ring
Reference Frequency (GHz)	2	5
Lock time(ns)	310	--
Locking range(GHz)	2.3- 4.7	2.5-7.3
Phase noise dBc/Hz (at 1MHz offset)	-109	-108.2
Power consumption (mW)	12.8	13.4

Table II : performance comparison of proposed circuit with other recent paper

4. MODELING USING VERILOG-A

When design of Fractional Synthesizers is realized, usually, it is necessary to run many transistor level simulations. This comes unpractical when the objective is to optimize the performance of the components one by one, because the simulation and design time grow significantly. Therefore, it is very useful to describe behavioral models for this mixed-signal system taking into account the noise and error sources during the circuit design. The behavioral models are high level hardware description scripts which are used in the netlist for the fast simulation of analog and/or digital blocks. To describe this model, a standard code like Verilog A is used. A circuit simulator (such as Spectre, Hspice or ADMS) is used to get the accurate values for the electrical variables of the network in a DC, transient or AC simulation. It is possible to simulate jointly a circuit modelled as a behavioral model and a circuit with device level models in Verilog A. A simulation of the frequency synthesizer, only with behavioral models, is also very useful when the specifications for every block in the synthesizers are obtained and a preliminary result is needed.

Beyond all this advantages, when the specifications and performance of a cell are evaluated, it is necessary to include as many non ideal characteristics as possible. The inclusion of this non ideal characteristics makes the behavioral simulation to describe more accurately the circuit performance.

By assuming good quality crystal reference, the close-in phase noise of output spectrum is mainly dominated by resistor noise in LP and CP current noise in VCO control signal path. Noise contribution by CP is modeled as multiplication results of the charge pump current noise and the ideal PFD output because CP contributes noise

when it is turned on by the PFD. Using transistor level simulation of noise performance of each block of PLL-FS, a Verilog-A model is presented for accurate extracted noise behavior of PLL-FS.

Model I. Verilog-A model for Voltage controlled oscillator with jitter/phase noise

```
// Voltage controlled oscillator with jitter/phase
noise:

'include "disciplines.h"
'include "constants.h"
module vco (vctrl, fout);
inout vctrl, fout;
electrical vctrl, fout;
parameter real Vlo=0;
parameter real Vhi=Vlo+1 from (Vlo :inf);
parameter real Flo=1 from (0:inf);
parameter real Fhi=2*Flo from (Flo:inf);
parameter real Vlo=0.5, Vhi=1.8;
parameter real tt=0.1/ Fh from (0:inf);
parameter real jitter=0 from [0:0.25/Fhi);
parameter real ttol=30n/Fhi from (0:1/hi);
real freq, phase, deT, delta;
integer k, seed;
analog begin
      @(initial_step) begin
      seed = –456
      freq = (V(vctrl) – Vlo)*(Fhi – Flo) / (Vhi – Vlo) +
      Flo;
      // phase noise delta = deT*freq;
      delta = delta/(1 – delta); freq = freq*(1 +
      delta);
      phase = 2*‘M_PI*idtmod(freq, 0.0, 1, -0.5);
      end
      @(cross(phase + ‘M_PI/2, +1, ttol) or
      cross(phase – ‘M_PI/2, +1, ttol)) begin
      deT = 1.414*jitter*$dist_normal(seed,0, 1);
      end
      //output
      k = (phase >= –‘M_PI/2) && (phase <
      ‘M_PI/2);
      V(fout) <+ transition(k ? Vhi : Vlo, 0, tt);
end
endmodule
```

Model II: Verilog-A model Phase-Frequency Detector with Charge Pump

```
// Phase-Frequency Detector with Charge Pump

`include “discipline.h”
`include “constants.h”
module pfdcp (ffref, ffeed,up, dn, vctrl);
input fref, ffed;
output out;
electrical ref, vco, out;
parameter real Iout=100u;
parameter integer ck= -1; // negative edge trigger
parameter real td=0 from (0:inf);
parameter real tt=1n from (0:inf);
parameter real ttol=1p from (0:td/5);
parameter real jitter=0 from [0:td/5);
integer state, seed; real det;
analog begin @(initial_step) seed = 450;
@(cross(V(fref), ck, ttol)) begin if (state > –1)
state = state – 1;
det = 0.707*jitter*$dist_normal(seed,0,1);
end
@(cross(V(vctrl), dir, ttol)) begin if (state < 1)
state = state + 1;
det = 0.707*jitter*$dist_normal(seed,0,1);
end
I(out) = <=transition (Iout*state, td + det, tt);
end
endmodule
```

Model III : Verilog-A model Frequency divider

```
// Frequency divider

`include “discipline.h”
`include “constants.h”
module divider (ffeed, fout);
input fout; output ffeed;
electrical in, out;
parameter real Vlo=–1, Vhi=1;
parameter integer ratio=2 from [2:inf);
parameter integer ck=-1; //  -1for negative edge
trigger
parameter real td=0 from (0:inf);
parameter real tt=1n from (0:inf);
parameter real jitter=0 from [0:td/5);
parameter real ttol=1p from (0:td/5);
integer count, n, seed; real det;
analog begin
  @(initial_step) seed = –296;
  @(cross(V(fout) – (Vhi + Vlo)/2, ck, ttol)) begin
  count = count + 1;
  if (count >= ratio) count = 0;
  n = (2*count >= ratio);
  det = 0.707*jitter*$rdist_normal(seed,0,1);
end
V(ffeed) = <+ transition(n ? Vhi : Vlo, td+det, tt);
endmodule
```

5. CONCLUSION

Design has been completed in cadence environment with 180nm Technology and simulated. Simulation results and Verilog-A model of PLL components are reported in this paper. Fig. 17 shows variation of frequency with respect to different voltages. Authors have observed the range of frequencies between 2.3 to 4.7 GHz with control voltage 0.1 to 1V. The lock time of frequency synthesizer is 300ns and Power consumption is 12.8mW. Phase noise of PLL is -109dBc/Hz at 1MHz offset. By describing the noise performance of each block of PLL-FS using transistor level simulation, Verilog-A model is presented for accurate extracted noise behavior of PLL-FS. Model are calibrated from circuit level noise simulations.

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