Journal of Engineering Sciences
Vol 11, Issue 3, MARCH /2020
ISSN NO:0377-9254

# A FAMILY OF CUK-ZETA- AND SEPIC BASED SOFT SWITCHING DC –DC CONVERTERS

[1]K. KRANTHI KUMAR, [2]Er. P. PEDDA REDDY, [3]Dr K .CHITHAMBARAIAH SETTY
[1]M.Tech Student, [2]Assistant Professor, [3]Associate Professor
Department of Electrical & Electronics Engineering

ST.JOHNS COLLEGE OF ENGINEERING & TECHNOLOGY, YERRAKOTA,YEMMIGANUR, KURNOOL

**ABSTRACT**

In this paper, a new class of dc-dc converter topologies based on capacitive link dc-dc converters—Ćuk, SEPIC, and Zeta converters—that operate under the critical conduction mode has been proposed. The proposed converters are the extensions of quasi-square-wave zero current-switching converters, which use an auxiliary circuit to provide zero-current and zero-voltage switching for all semiconductor switches at both turn-on and turn-off transitions and eliminate voltage ringing across the output switch. Using the proposed auxiliary circuit, the value of dv/dt has been diminished; hence, the EMI of the proposed topology is significantly reduced compared to the conventional quasi-square-wave zero-current-switching converters. To verify the operation of the proposed converter and confirm its advantages, an experimental prototype has been implemented, and the experimental results and the efficiency of the proposed converter have been compared with the conventional quasi-square-wave zero-current-switching converters.

## I.INTRODUCTION

With the rapid development of renewable energy systems, smart grid, and electric vehicles, the need for high performance non-isolated/isolated dc-dc converters has significantly increased in numerous applications. Since the main operation principles of the basic power converters are well understood, more attention is being paid to the power density and efficiency as the core priorities of recent researches in power electronics. The most straightforward approach to improve the power density is to increase the switching frequency as the size and volume of the incorporated passive components are highly dependent on it. However, an increase in switching frequency causes electromagnetic interference (EMI) problems and results in extra switching losses that lower efficiency in power converters [1]. The most effective way to increase the efficiency in high-frequency power converters is to decrease/eliminate the switching losses of the transistors with the help of soft-switching techniques.

Generally, soft-switching techniques aim to eliminate or minimize the overlap between the current and voltage waveforms of the transistors in every switching transition. Accordingly, numerous soft-switching techniques have been proposed in the literature to increase the efficiency of the power conversion by providing either zero voltage transition (ZVT) or zero current transition (ZCT) or a combination of the two. ZVT and ZCT are typically attained with the help of an auxiliary circuit, called active snubber. Although the performance of the active snubbers is evaluated as excellent in terms of efficiency and power density, they are often considered too complex for practical applications [2].

Certain complexity must be justifiable since active snubbers always require additional components to achieve ZVT and/or ZCT [3]. Utilizing an auxiliary circuit, including auxiliary switches as well as auxiliary inductors and/or capacitors, to provide soft switching for the main switch has been widely studied in the literature, as will be reviewed in the following [4-12]. In [4], a class of ZVT PWM converters is presented to turn on the main switch with zero-voltage during a short transition provided by a resonance. This contributes to the soft-switching operation of the main switch and diode by providing zero-voltage switching (ZVS). However, the auxiliary switch is turned off under hard switching and the operation of the circuit is dependent on the load conditions. Accordingly, a number of approaches were proposed to address this problem [5-7]. A family of ZCT PWM converters was proposed in [8] to implement zero-current switching (ZCS) during the turn off process of the main switch by adding a resonance mode. However, the main switch still has hard-switching during turn on; the switch of the auxiliary circuit is also turned off under hard-switching conditions. In order to address these problems, different approaches have been proposed in the literature such as [9]. In [10] and [11], an auxiliary circuit consisting of an auxiliary switch, diode, inductor, and capacitor is used to provide ZCT for all semiconductor switches. Even though employing an auxiliary circuit can facilitate soft switching operation of the transistors, it might also negatively affect the performance of the whole converter. In [12] for instance, the proper operation of a soft-switching technique for turn-on and turn-off of both main and auxiliary switches is proposed; however, the current stress on the main switch is twice the input current.

The high current stress can also be observed on the auxiliary switch. High current stress can negatively impact the reliability of the converter, although the improved efficiency is reported in this work. A new active snubber cell for a boost dc-dc converter, which provides ZVT turn on and ZCT turn off with no extra voltage or current stress on the main switch, was proposed in [1]. Although the efficiency of the proposed scheme is reported to be improved, high current stress is observed on the auxiliary switch. Also, the auxiliary circuit (active snubber cell) seems to be too complex and has a large number of active and passive components. This results in a more complex control and jeopardizes the highpower density. A similar auxiliary circuit is added to the boost dc-dc converter in [13] to implement soft-switching of all the switches without extra voltage stresses. However, the auxiliary circuit includes one switch, one inductor, two capacitors, and two extra diodes, which increase the complexity of the whole system and reduce the power density. The high current stresses can also be observed in [14], in which an auxiliary circuit is added to the PWM boost dc-dc converter to practically implement ZCS of the main switch. Furthermore, higher voltage stresses are applied to the auxiliary switch. In [15] and [16], the auxiliary circuit used to provide soft-switching brings about extra oscillations with snubber capacitors, even though the circulating current of the auxiliary circuit is minimized. Among the drawbacks of utilizing auxiliary circuits with extra semiconductors [17], the power dissipation of the auxiliary circuit, especially the auxiliary switch [18], more voltage and/or current stress on the main and/or the auxiliary switch, and higher volume and weight of the converter can be named. To address these drawbacks, soft-switching techniques by adding only extra passive components, i.e., L and/or C, without any auxiliary semiconductor, were proposed. In [19] for instance, only a series LC tank is added to provide ZVS turn-on for the source-side switch, while there are still power losses at the turn-off transition of the switch. Moreover, since the duration of the discharging interval is controlled by the resonance tank parameters, the converter can be regulated only by changing the switching frequency, rather than the duty cycle; this leads to very high switching frequencies at light loads, which might be practically impossible to achieve. In another work [20], coupled inductors are used to provide ZVS for the boost converter; however, this approach has led to lower power density and higher weight of the converter. Operating in critical conduction mode (CRM) and adding a passive component to form quasi-square-wave (QSW) converters is another approach that has been proposed in the literature to provide soft-switching for the main switch. Operating the converter in CRM for the voltage or current of the main energy storage element is one of the most reliable methods to achieve high power density and fast transient response, too [21], because smaller energy storage elements are needed. Since the waveform (voltage or current, depending on the topology) of the main energy storage element reaches zero in CRM, a natural zero voltage/current switching happens at this moment. In QSW converters an auxiliary passive component is added to form partial resonant transients between the regular power transferring states of dc-dc PWM converters operating in CRM and further improve the efficiency.

Considering the advantages of QSW converters, including natural zero voltage/current moments, small size link energy storage element, high power density, high efficiency, and single-stage power conversion feature; lots of researches have been conducted on these converters. In most cases, the attention is given to the ZVS buck-boost-based converters, in which the inductor current operates in CRM and an auxiliary capacitor is added to assure soft-switching during all switching transitions. In these cases, the auxiliary circuit includes only a passive component and the soft-switching techniques are implemented without adding extra semiconductor devices [21-28]. This approach helps the soft-switching transition of the main switch during turn-on; however, this switch may still turn off in hard switching, especially when the switching frequency is high, and this can cause EMI problems and lower efficiency. The operation of the QSW converters will be discussed in detail in Section II. By taking the advantages of QSW converters and auxiliary circuits, in this paper, a new family of soft-switching ac-link dcdc converters is proposed to overcome the demerits of both QSW and auxiliary-circuit-based converters. The proposed family of dc-dc converters adds an auxiliary circuit with semiconductor devices to the well-known Ćuk-, SEPIC-, and Zeta-based QSW converters. Although an auxiliary circuit is added to the converter, it does not increase the control complexity as opposed to several soft-switching techniques that are proposed in the literature. The main contributions of the paper to improve conventional QSW-ZCS converters are (i) providing ZVS in addition to ZCS for the all incorporated semiconductor devices, leading to higher efficiency, (ii) eliminating the severe high frequency voltage ringings and spikes across the output switch of the conventional QSW-ZCS converters, which lowers the voltage stress of the switch and enables the designer to choose semiconductor devices with lower voltage rating for the output switch and eliminates the need for passive RC snubbers, and (iii) reducing the value of dv/dt, which brings about EMI improvement. The paper is segmented into the following sections. Section II reviews the conventional QSW converters and specifies the advantages and drawbacks of this family of converters.

A new approach for addressing the problems associated with QSWZCS converters is proposed in further chapters as the main contribution of the paper, which is followed by detailed explanation of the operating modes and waveforms for the Ćukbased converter. The proposed auxiliary circuit can also be employed in Zeta- and SEPIC-based converters.

## II.DC-DC CONVERTER BASICS

A DC-to-DC converter is a device that accepts a DC input voltage and produces a DC output voltage. Typically the output produced is at a different voltage level than the input. In addition, DC-to-DC converters are used to provide noise isolation, power bus regulation, etc. This is a summary of some of the popular DC-to-DC converter topologies.

### BUCK CONVERTER STEP-DOWN CONVERTER

In this circuit the transistor turning ON will put voltage $V_{in}$ on one end of the inductor. This voltage will tend to cause the inductor current to rise. When the transistor is OFF, the current will continue flowing through the inductor but now flowing through the diode.

We initially assume that the current through the inductor does not reach zero, thus the voltage at $V_x$ will now be only the voltage across the conducting diode during the full OFF time. The average voltage at $V_x$ will depend on the average ON time of the transistor provided the inductor current is continuous.

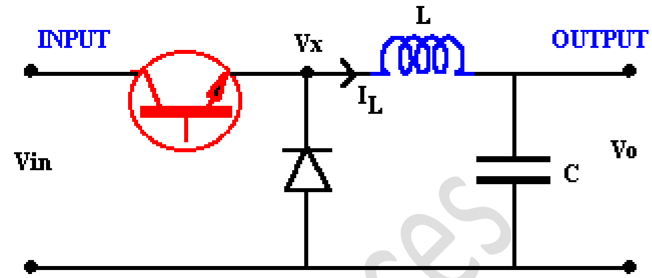



Fig 1 Buck Converter

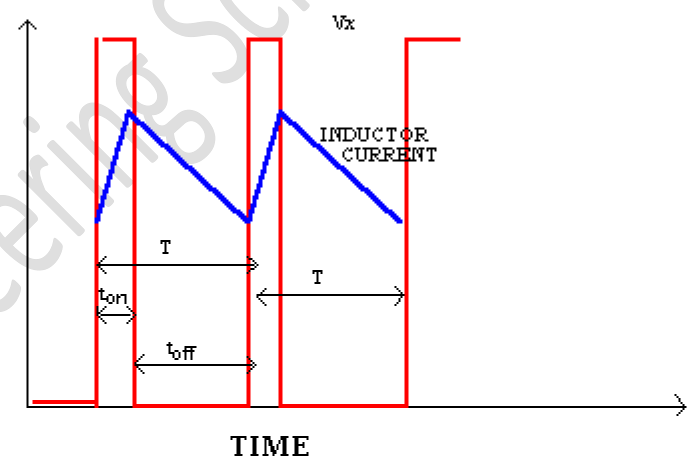



Fig .2 Voltage and current changes

### BOOST CONVERTER STEP-UP CONVERTER

The schematic in Fig. 6 shows the basic boost converter. This circuit is used when a higher output voltage than input is required.

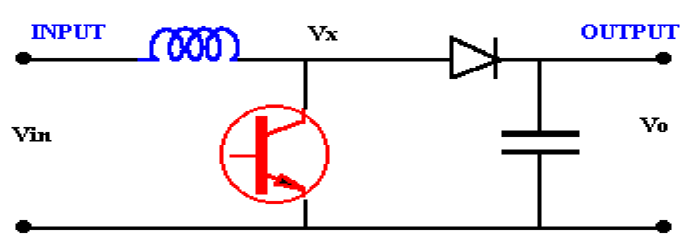



Fig 3 Boost Converter Circuit

Vol 11, Issue 3, MARCH /2020
ISSN NO:0377-9254

While the transistor is ON $V_x = V_{in}$, and the OFF state the inductor current flows through the diode giving $V_x = V_o$. For this analysis it is assumed that the inductor current always remains flowing (continuous conduction).

**BUCK-BOOST CONVERTER**

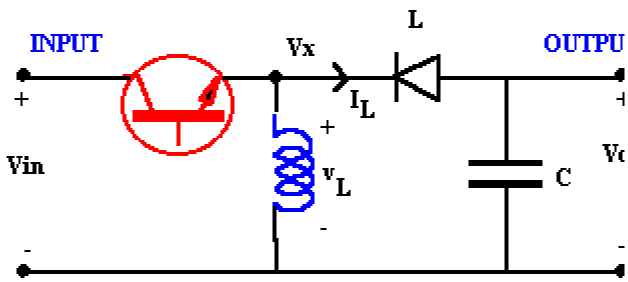



Fig 4 schematic for buck-boost converter

With continuous conduction for the Buck-Boost converter $V_x = V_{in}$ when the transistor is ON and $V_x = V_o$ when the transistor is OFF.

**III.PROPOSED TOPOLOGY AND ITS PRINCIPLES OF THE OPERATION**

This chapter describes operation modes and the main waveforms of the proposed Ćuk-based dc-dc converter in detail. Due to the page limitation, for the proposed Zeta- and SEPIC based converters, only the schematics and key waveforms are shown. The principles of the operation of Zeta- and SEPIC based converters are similar to the Ćuk-based converter.

**3.1 Proposed Topology: Ćuk-based**

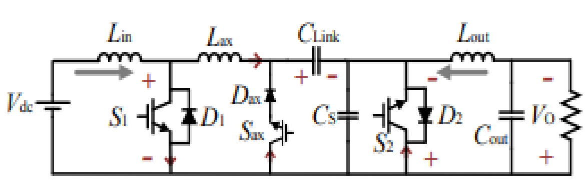



Fig. 4. Proposed Ćuk-based topology

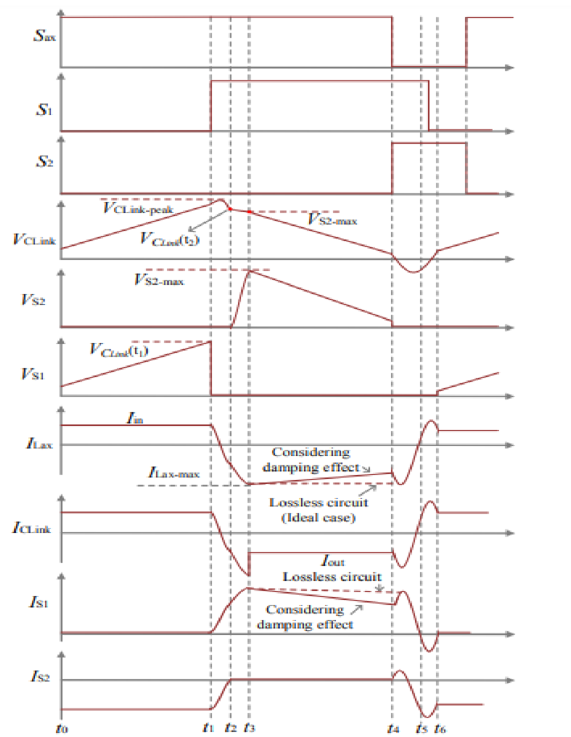



Fig. 5. Key waveforms of the proposed Ćuk-based converter.

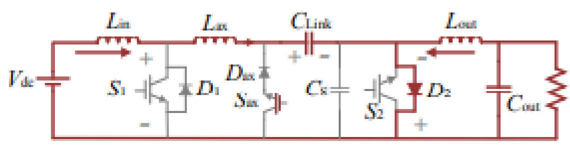
Fig. 4. shows the proposed Ćuk-based dc-dc converter topology in which the link capacitor, $CLink$, operates in CRM enabling the designer to utilize a very small film capacitor instead of a bulky and unreliable electrolytic capacitor. As a result, the lifetime of the converter is expected to be improved. In order to prevent the voltage across the switch $Sout$ from ringing at $t2$ [see Fig. 5], it should be blocked by the link voltage at this time and be limited to $VClink$. This is accomplished by adding a diode and finding a suitable location for inserting this diode. Diode $Dax$ in Fig. 6 by itself can effectively eliminate all the ringing across $S2$ ($Sout$ in Fig. 4.) by impeding the voltage across the switch going above the link voltage. This diode does not affect the operation of the converter in all other modes but the last resonance mode. So, a switch can be placed in series with it to make sure the diode does not conduct

Journal of Engineering Sciences
Vol 11, Issue 3, MARCH /2020
ISSN NO:0377-9254

whenever it is not expected. A capacitor in parallel with a switch, also, adds more resonant intervals to help providing ZVS for the converter. Fig. 4.3 and Fig. 4.4 show the details of each operating mode as well as the corresponding waveforms, respectively. The current directions and the voltage polarities of the waveforms of Fig. 8 are specified in Fig. 4.

**Interval-1 (t0 — t1):**

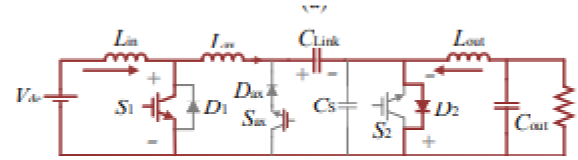
at this interval, the switch S1 is off, and the input current, which is considered to be dc during each switching cycle, charges the link capacitor, $CLink$. Pathing this dc current through $Lax$ generates no voltage across it, so $Lax$ does not play any role during this mode. The input current, $ILin$, closes its path via the anti-parallel diode of S2 (D2). This operating mode is terminated by turning S1 on.



(a)

**Interval-2 (t1 — t2):**

By turning S1 on, the link components, which are the series connection of $CLink$ and $Lax$, see a short circuit path and start to resonate. Fig. 9 indicates the equivalent circuit of the converter during this mode and its corresponding state plane diagram. According to the state plane diagram of Fig. 9 (b), the current of the auxiliary inductor, , starts decreasing from its initial value, which is $Iin$ , and becomes negative. At the same time, the current of the anti-parallel diode of S2 (D2) gradually decreases until it reaches zero. This is the time at which $iLax$ is equal to − . D2 turns off in ZCS, so the reverse recovery effects are ignorable for this diode.



(b)

**Interval-3 (t2 — t3):**

once D2 is turned off, the resonance circuit becomes completely different. The equivalent circuit of the converter during this interval is shown in Fig.4.6 (a). $Iin$ closes its path through the input switch, so it does not affect the resonance circuit and can be omitted in the resonance small signal mode. As a result, $CS$ and $CLink$ are placed in series, and since the capacitance value of $CS$ is much smaller than that of $CLink$, the resonance occurs between $Lax$ and , and $CLink$ can be modeled as a dc voltage source since its voltage is almost constant during this mode. As shown in the state plane diagram of Fig. 4.6(b), the state parameters are the current of the auxiliary inductor, $iLax$, and the voltage of . During this resonance interval, state parameters start to resonate from their initial values that are equal to

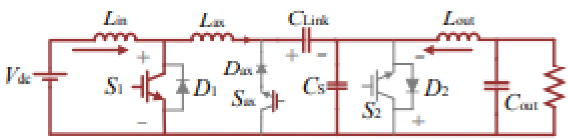
$(t2\ ) = -Iout$ (3)

$(t2\ ) = 0$ (4)

, which is the voltage across the S2, starts to gradually increase during this mode providing the ZVS turn off for D2. This gradual increase of voltage across the switch reduces the amount of , which is one of the main sources of EMI generated in a power converter. Since the auxiliary switch Sax is kept on during this mode, Dax is off as long as $vCs < VClink$. This mode continues until $vCs$ becomes greater than the link capacitor voltage and Dax turns on. Even though considering a constant voltage for the link capacitor can be a valid assumption to simplify the behavior of the circuit during this

Vol 11, Issue 3, MARCH /2020
ISSN NO:0377-9254

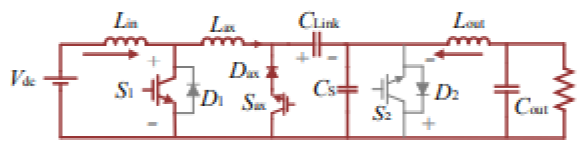
interval, this voltage drops slightly from $VClink(t2)$ to $VS2{-}max$ (as indicated in Fig.4.7) during this interval. Therefore, by equating the energy of the passive components at $t2$ and $t3$,




(c)

**Interval-4 (t3 — t4):**

This mode is a power transferring mode in which the energy stored in the $CLink$ will be discharged to the output load. From another point of view, the output current, which is considered to be constant in each switching cycle, flows to the link capacitor and discharges it; therefore, the voltage of the link capacitor decreases. The current of the auxiliary switch (Sax) and diode (Dax) at the beginning of this interval is equal to $ISax = ILax{-}max - Iout$ (8) In an ideal situation, the energy stored in $Lax$ will be fully transferred to the load at the end of the last switching interval (at $t6$ ) through $CLink$, and the current of $Lax$ remains constant during interval 4. However, due to conduction losses of the semiconductors and the resistances of the path, a portion of this energy is dissipated and the rest of it will be transferred to the load through . As shown in Fig. 8, the reason that the current of auxiliary inductor, $ILax$, gradually reduces is indeed the path losses. The damping factor of the circuit during this time interval determines the amount of decrease in $ILax$. This damping factor is equal to the damping factor of Fig. 5 in which the ringings are damped after a moment, otherwise (considering a lossless path) the ringings would continue without any damping in their amplitudes. This mode terminates when the voltage of the link capacitor reaches zero, or the link capacitor ( ) is completely discharged. To assure ZCS of S1 regardless of the voltage gain, this mode can be ended before the link capacitor is fully discharged. Ending this mode before the link voltage is zero, will result in higher amplitude of the link current during intervals 5 and 6. Therefore, by comparing the link voltage with a constant voltage ( ), and detecting the moment at which the link capacitor voltage becomes lower than the constant voltage, Interval 4 can be terminated at this moment by turning S2 on. $Vconst$ should be chosen such that it assures there is enough energy at the link at $t4$ in order to bring the link current up to a value equal to at least input current during the resonance.

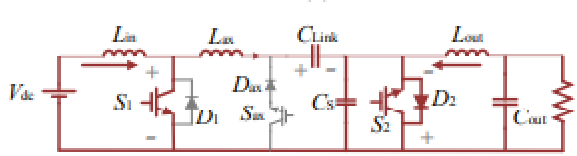



(d)

**Interval-5 (t4 — t5):**

the main purpose of this mode is to provide the ZCS turn off for the input switch (S1). In order to do so, a resonance mode is needed to make the current of S1 negative; therefore, the anti-parallel diode of it conducts. As a result, the following situation should be met: $iLax > Iin$. To make sure the aforementioned conditions are provided and extend the softswitching range, S2 turns on at the end of Interval 4 once the link capacitor voltage is a little bit higher than zero so that the link components have enough energy for a full resonance. It is worth mentioning that since the link capacitor voltage ($vClink$) is almost zero (or very small) S2 turns on under ZVS condition. Fig. 11 shows the equivalent circuit of the converter and its state plane diagram during intervals 5 and 6 (t4 — t6). During interval 5, the current of S1 is still positive.

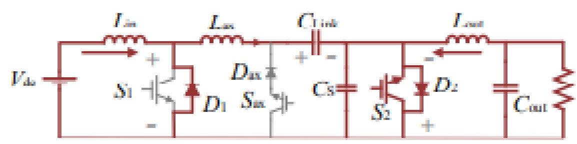
Vol 11, Issue 3, MARCH /2020
ISSN NO:0377-9254



(e)

**Interval-6 (t5 ─ t6):**

The converter model in this interval is similar to that of the previous interval, but during this interval, the antiparallel diode of S1 conducts. Therefore, S1 can be turned off at any time during this time interval in ZCS It is worth mentioning that switch S2 can be turned off any time after $t5$ and before the start of the next switching cycle in ZVS since its antiparallel diode conducts.



(f)

## IV.FUZZY LOGIC

In recent years, the number and variety of applications of fuzzy logic have increased significantly. The applications range from consumer products such as cameras, camcorders, washing machines, and microwave ovens to industrial process control, medical instrumentation, decision support systems, and portfolio selection. To understand why use of fuzzy logic has grown, you must first understand what is meant by fuzzy logic.

Fuzzy logic has two different meanings. In a narrow sense, fuzzy logic is a logical system, which is an extension of multivalve logic. However, in a wider sense fuzzy logic (FL) is almost synonymous with the theory of fuzzy sets, a theory which relates to classes of objects with un sharp boundaries in which membership is a matter of degree. In this perspective, fuzzy logic in its narrow sense is a branch of FL. Even in its more narrow definition, fuzzy logic differs both in concept and substance from traditional multivalve logical systems.

**What is fuzzy logic?**

Fuzzy logic is all about the relative importance of precision is how important is it to be exactly right when a rough answer will do?

You can use Fuzzy Logic Toolbox software with MATLAB technical computing software as a tool for solving problems with fuzzy logic. Fuzzy logic is a fascinating area of research because it does a good job of trading off between significance and precision something that humans have been managing for a very long time. In this sense, fuzzy logic is both old and new because, although the modern and methodical science of fuzzy logic is still young, the concept of fuzzy logic relies on age old skills of human reasoning.

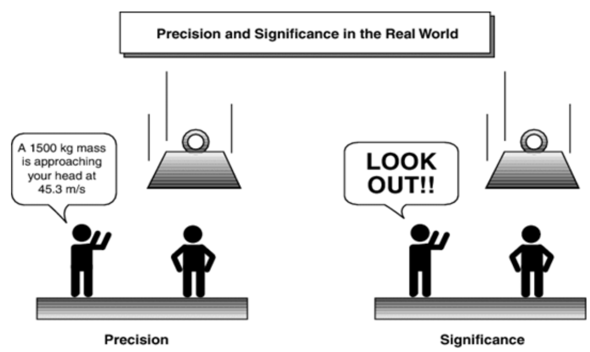



**Fig.6** Fuzzy descriptions

**Building a fuzzy inference system**

Fuzzy inference is a method that interprets the values in the input vector and, based on user defined rules, assigns values to the output vector. Using the GUI editors and viewers in the Fuzzy Logic Toolbox, you can build the rules set, define the membership functions, and analyze the behavior of a fuzzy inference system (FIS). The following editors and viewers are provided.

Vol 11, Issue 3, MARCH /2020
ISSN NO:0377-9254

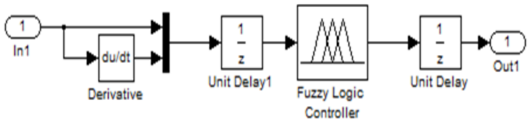



**Fig.7** Fuzzy interference system

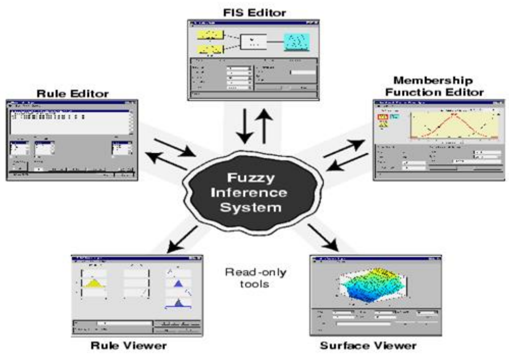



**Fig.8** The primary GUI tools of the fuzzy logic toolbox

**V.MATLAB DISCUSSION&SIMULATION RESULTS**

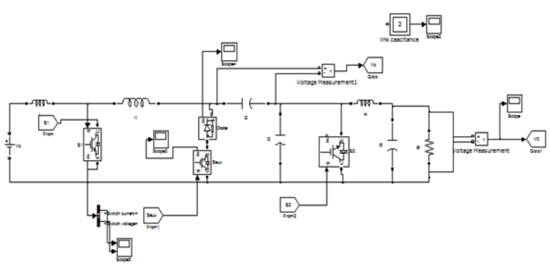


**Fig 9 Cuk –Based Topology**

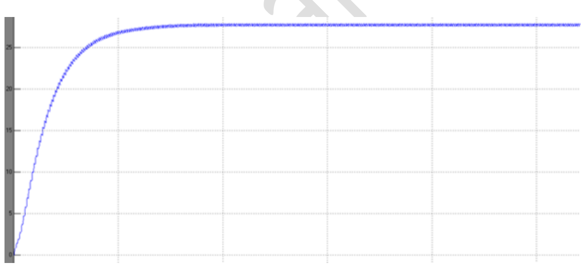


**Fig 10 Key Waveforms of the Proposed Cuk –Based Topology**

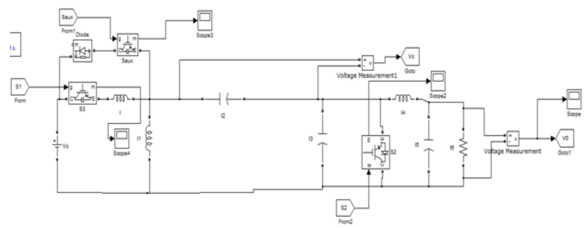


**Fig 11 Zeta –Based Topology**

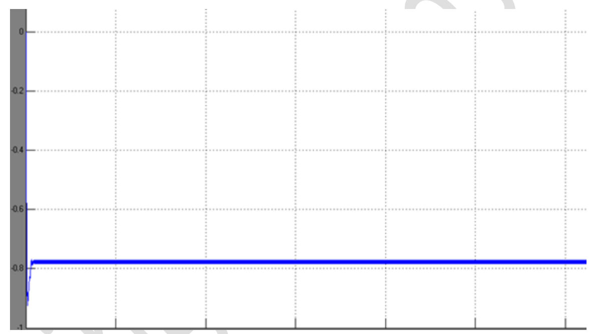


**Fig 12 Key Waveforms of the Proposed Cuk –Based Topology**

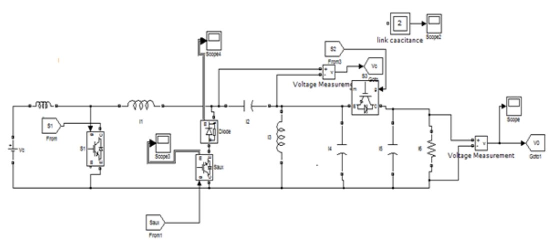


**Fig 13 SEPIC –Based Topology**

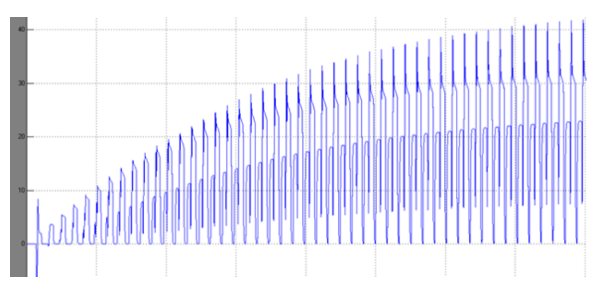


**Fig 14 Key Waveforms of the Proposed Cuk –Based Topology**

## VI.CONCLUSION

This project introduced a family of soft-switching dc-dc converters based on Ćuk, SEPIC, and Zeta converters that operate in CRM. By adding auxiliary components, not only the voltage riggings across the output switch are eliminated, but also a soft-switching transition is provided, which significantly increases the efficiency of the converter. As a result, all semiconductor switches benefit from ZCS and ZVS during both turn-on and turn-off transitions. Moreover, by providing ZVS at the turn-on moment of the input switch, the dv/dt value of the converter has been confined, resulting in reduction of EMI. All the above-mentioned benefits have been verified in simulation by comparing the proposed circuit with conventional QSWZCS dc-dc converters.

## REFERENCES

[1] B. Akın, "An Improved ZVT-ZCT PWM DC-DC Boost Converter With Increased Efficiency," IEEE Transactions on Power Electronics, vol. 29, no. 4, pp. 1919-1926, 2014.

[2] H. Bodur and A. F. Bakan, "A new ZVT-ZCT-PWM DC-DC converter," IEEE Transactions on Power Electronics, vol. 19, no. 3, pp. 676-684, 2004.

[3] M. Pavlovský, G. Guidi, and A. Kawamura, "Buck/boost DC–DC converter topology with soft switching in the whole operating region," IEEE Transactions on Power Electronics, vol. 29, no. 2, pp. 851-862, 2014.

[4] H. Guichao, L. Ching-Shan, J. Yimin, and F. C. Y. Lee, "Novel zerovoltage-transition PWM converters," IEEE Transactions on Power Electronics, vol. 9, no. 2, pp. 213-219, 1994.

[5] H. Bodur and A. F. Bakan, "A new ZVT-PWM DC-DC converter," IEEE Transactions on Power Electronics, vol. 17, no. 1, pp. 40-47, 2002.

[6] L. Dong-Yun, L. Byoung-Kuk, Y. Sang-Bong, and H. Dong-Seok, "An improved full-bridge zero-voltage-transition PWM DC/DC converter with zero-voltage/zero-current switching of the auxiliary switches," IEEE Transactions on Industry Applications, vol. 36, no. 2, pp. 558-566, 2000.

[7] C. M. d. O. Stein and H. L. Hey, "A true ZCZVT commutation cell for PWM converters," IEEE Transactions on Power Electronics, vol. 15, no. 1, pp. 185-193, 2000.

[8] H. Guichao, E. X. Yang, J. Yimin, and F. C. Lee, "Novel zerocurrent-transition PWM converters," IEEE Transactions on Power Electronics, vol. 9, no. 6, pp. 601-606, 1994.

[9] M. Hengchun, F. C. Y. Lee, Z. Xunwei, D. Heping, M. Cosan, and D. Boroyevich, "Improved zero-current transition converters for high-power applications," IEEE Transactions on Industry Applications, vol. 33, no. 5, pp. 1220-1232, 1997.

[10] E. Adib and H. Farzanehfard, "Family of Zero-Current Transition PWM Converters," IEEE Transactions on Industrial Electronics, vol. 55, no. 8, pp. 3055-3063, 2008.