CMOS Reversible Gates for Low Power Applications Power Delay Review

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Abstract— At present, circuits with low power and less computation time are in high demand in VLSI technology. In this context, the applications of reversible logic are far-reaching. In this paper, the detailed evaluation of certain reversible gates, namely, Feynman gate, Peres Gate, Modified Fredkin Gate, Modified Toffoli Gate, and TS Gate is set forth. Evaluation comprises of transistor implementation, simulation results and average power and delay measurement. The utilization of TSG to form a completely reversible full adder has also been evaluated in details. The implementations are completely reversible in nature and finds their applications in circuits with low power and high speed which are suitable to implement in silicon.
Keywords—Reversible Gates, Reversible Logic, Reversible Full Adder

I. INTRODUCTION

Circuits constructed using irreversible logic have certain limitations, the most important of those being considerable heat dissipation during calculation. Heat energy amounting to kTln2 Joules is given out corresponding to a single bit of lost information. Here, T refers to temperature in Kelvin which is the temperature for execution of calculation and k stands for Boltzmann's constant [1], Number of bits lost while computing has a direct relationship with amount of heat energy dissipation. Therefore, as shown by Bennett, the said quantity of heat loss can be effectively controlled by conducting reversible computation [2], Reversible logic gates usually construct reversible logic circuits because no information is lost by them, thus they are needed in CMOS circuits characterized by high speed and low power. By combining reversible gates, reversible circuits are constructed which are capable of executing complicated arithmetic functions and logical operations. Inputs as well as outputs undergo the realization of one-to-one mapping among themselves. This paper presents the design and evaluation of following logic gates which are reversible in nature, viz., Feynman gate [3] [4], Peres Gate [5], Modified Fredkin Gate [3] [4], Modified Toffoli Gate [3] [4], TSG gate [6] [7] [8] with a view to its transistor level implementation and evaluation in terms of number of gates used, simulation results, power dissipation and propagation delay. The application of TS gate in designing a full adder [10] is also shown. The aforesaid reversible designs can be practically implemented in silicon chips.

This paper is organised in the following manner: Section II talks about the aforesaid reversible logic gates, their implementation using CMOS and their detailed evaluation. Section III details the conclusion.

II. EVALUATION OF SOME REVERSIBLE GATES

This segment describes in details some reversible gates, mentioning their features like transistor implementation, simulation results, power and delay measurement.

A. Feynman Gate

Feynman gate [3] [4], a 2*2 reversible logic gate is given in Fig. 1. Here, one input variable is equivalent to one of the outputs, i.e. it is a one-through gate. The other output denotes XOR operation.

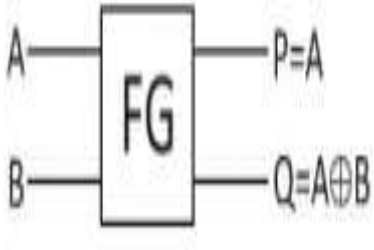


Fig. 1. Block diagram of Feynman gate

a) Schematic ofFeynman gate in transistor level

Fig. 2 gives the fully reversible schematic of Feynman gate using transistors. The first output (P) is a buffer of the first input (A). The said implementation requires 8 transistors and involves the approach of reversible logic as opposed to pass transistor logic [13],

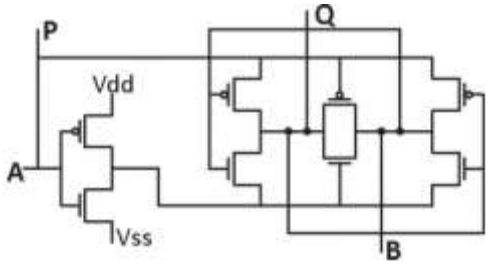


Fig. 2. Schematic of Feynman gate in transistor level

Here, while computing in forward direction, it is seen that output P is equivalent to input A. Now, if input A = 0, output Q = B ,or Q = B' when A = 1.
Similarly, A = P during reverse computation. If P is set to 0, then B is found to be equal to Q, otherwise B = Q'.

b) Results of Simulation

Effective simulations have been carried out using TSPICE at 298K (room temperature) with CMOS of channel length 180nm. Voltage ranging from 1 V to 2 V have been supplied, with steps of 0.2 V[14].

As a result of those simulations we have provided the simulation input patterns with output wave-forms at a supply voltage of 1.8V in Fig. 3 as well as the average power dissipation and delay curves in Fig. 4 below[15].

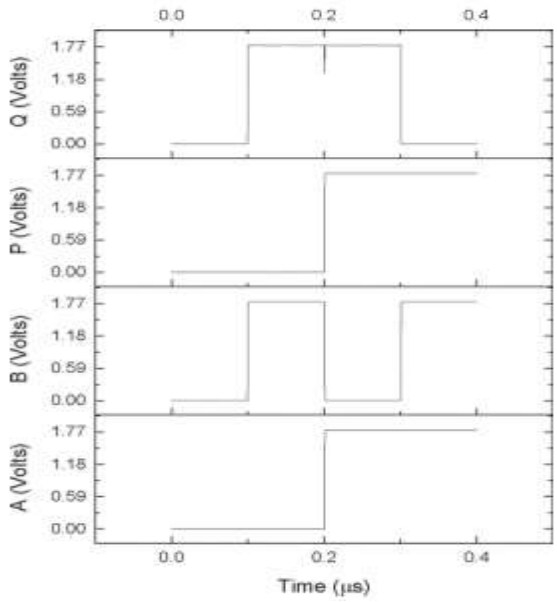


Fig. 3. Simulation input and output wave-form

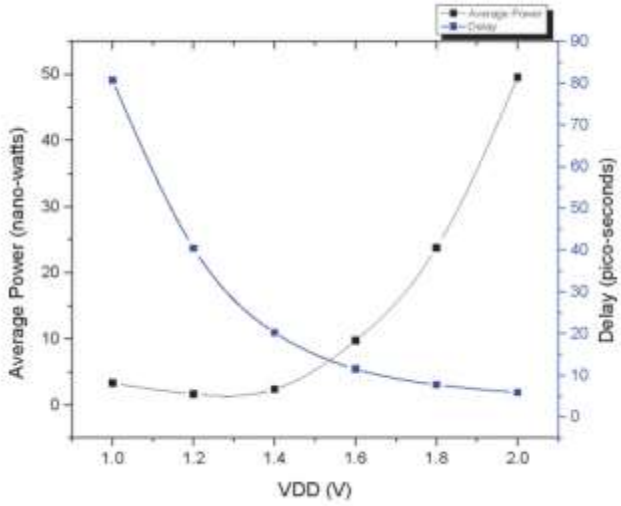


Fig. 4. Average Power Dissipation and Delay Curves

B. Modified Fredkin Gate (MFG)

Another important reversible gate is Fredkin gate, conservative in nature [3] [4] having 3 inputs and 3 outputs. Fig. 5 shows the Modified Fredkin Gate [11],

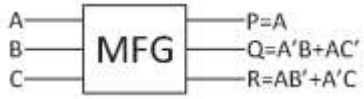
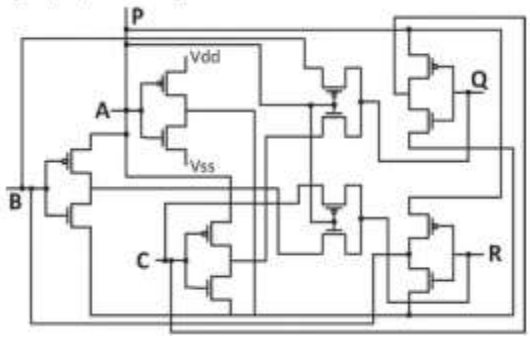


Fig. 5. Blockdiagram of MFG

a) Schematic ofMFG in transistor level

Fig. 6 gives the fully reversible schematic of MFG constructed with transistors. Computation can be carried out in forward as well as reverse direction, thus making it completely reversible. The first output (P) is a buffer of the first input (A). This implementation is with 14 transistors[16].



Here, while computing in forward direction, it is seen that output P is equivalent to input A. Now, if input A = 0, output Q = B, also output R = C, again Q = C' as well as R = B' when A= 1.

Similarly, A = P during reverse computation. If P is set to 0, then B is found to be equal to Q and C becomes equivalent to R, otherwise terminal C = Q' and terminal B = R'.

b) Results of Simulation

Effective simulations have been performed using TSPICE with room temperature set to 298K. 180nm CMOS has been used. Voltage ranging from 1 V to 2 V with intermediate steps of 0.2 V have been provided. As a result of those simulations we have given the simulation input patterns with output wave- forms at a supply voltage of 1.8V in Fig. 7 above as well as the average power dissipation and delay curves in Fig. 8 below. The output wave-forms show some degradations in voltage levels. But it does not bring a considerable change in the desired output, and so may be accepted in order to minimise the number of transistors used[17].

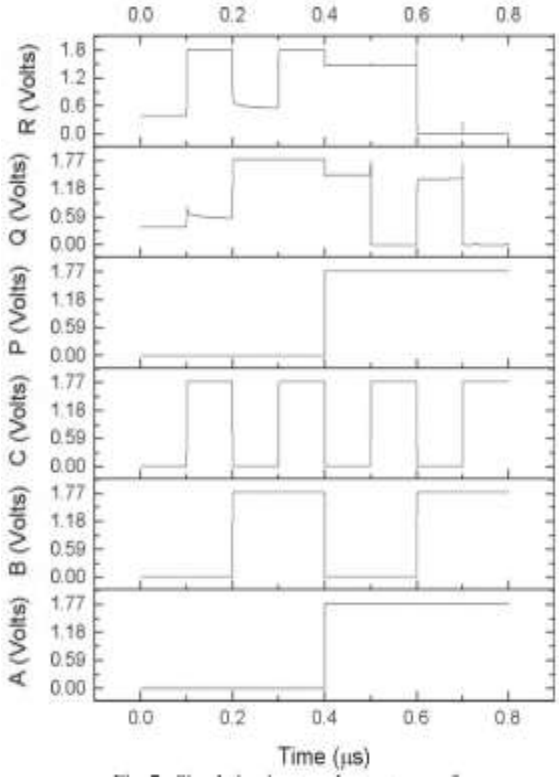


Fig. 7. Simulation input and output wave-form

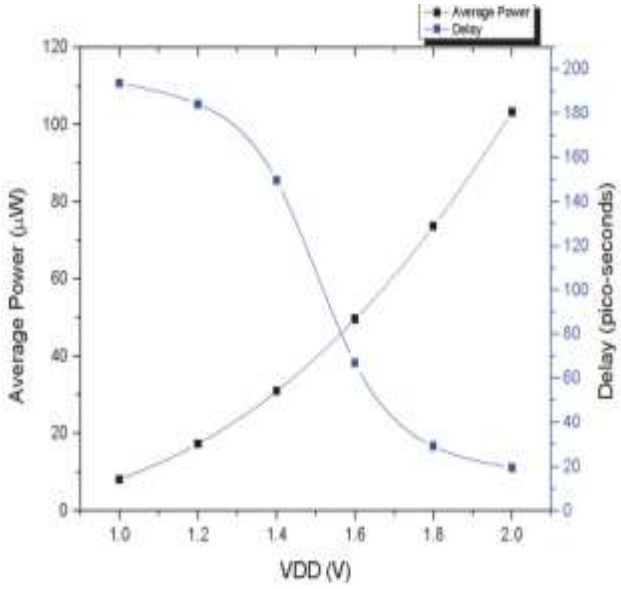


Fig. 8. Average Power Dissipation and Delay Curves

C. Modified Toffoli Gate (MTG)

Toffoli Gate [3] [4] is one fully reversible gate whose inputs and outputs are each 3 in number. This gate has 2 of its inputs equal to 2 outputs. Therefore, this gate is a two-through gate. Modified Toffoli gate's block diagram has been given below in the Fig. 9. [11],

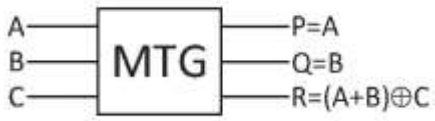


Fig. 9. Block diagram of MTG

a) Schematic ofMTG in transistor level

Fig. 10 gives the transistor-level schematic ofMTG. The said design is a fully reversible one and 12 transistors have been utilized. In this circuit, one output terminal P can be obtained straight from one input terminal A, and Q and B are simply hardwired. Here, while computing in forward direction, it is seen that input terminals A and B are equivalent to output terminals P and Q, respectively. If either input B = 0 or input A = 0, we have output R = C', or otherwise R = C.

Similarly, terminal A = P and terminal B = Q during reverse computation. When either terminal P or terminal Q is set to 0, then C is found to be equal to R, otherwise C = R'.

b) Results of Simulation

Results obtained from TSPICE simulations implemented at room temperature in a standard 180nm CMOS are shown here. Initially supply voltage was taken to be 1 V and then increasedby0.1V in each step, up to 1.8V. As a result of those simulations we have provided the simulation input patterns with output wave-forms at a supply voltage of 1.8V in Fig. 11 as well as the average power dissipation and delay curves in Fig. 12 below.

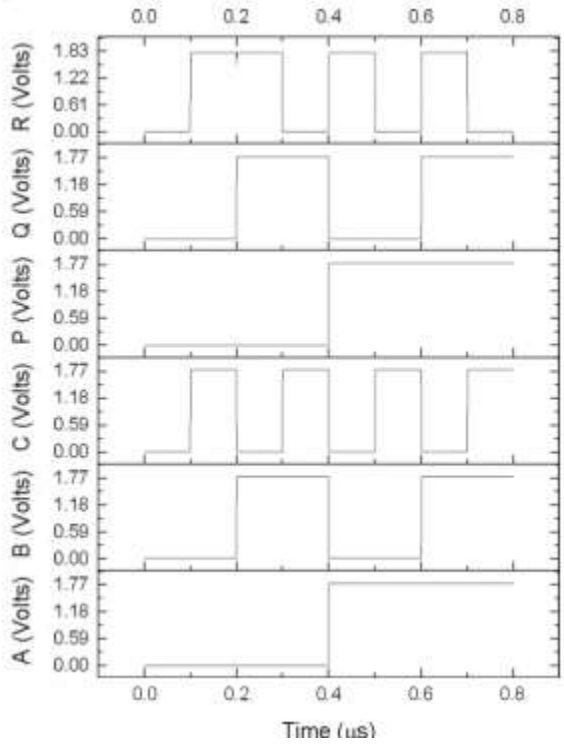


Fig. 11. Simulation input and output wave-form

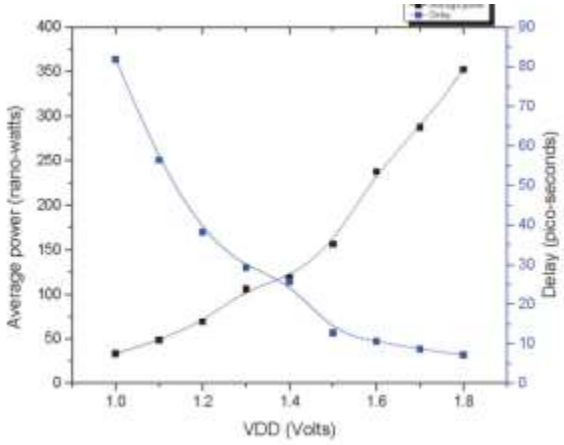


Fig. 12. Average Power Dissipation and Delay Curves

D. Peres Gate

Another important logic gate having reversible property is Peres gate [5] consisting of 3 inputs and 3 outputs. It can be viewed as an amalgamation of Feynman and Toffoli gate. Fig. 13 shows Peres gate.

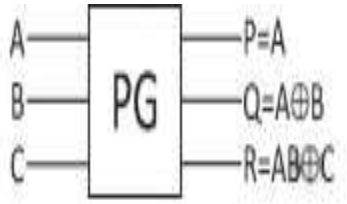


Fig. 13. Block diagram of Peres Gate

a) Schematic of Peres Gate in transistor level

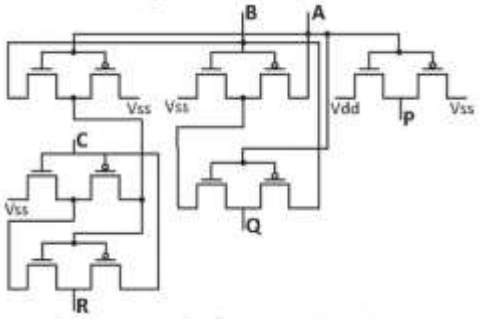


Fig. 14 gives the schematic of Peres Gate [5], which is completely reversible. The first output (P) is a buffer of the first input (A). The said implementation involves the concept of pass transistors using 12 transistors.

Here, while computing in forward direction, it is seen that output P is equivalent to input A. Now, if input A = 0, the output Q = B as well as R = C; or Q = B5and also R = C5when A= 1.

Similarly, A = P during reverse computation. If P is set to 0, then B is found to be equal to Q and C becomes equivalent to R, otherwise terminal B = Q5and terminal C = R.

b) Results ofSimulation.

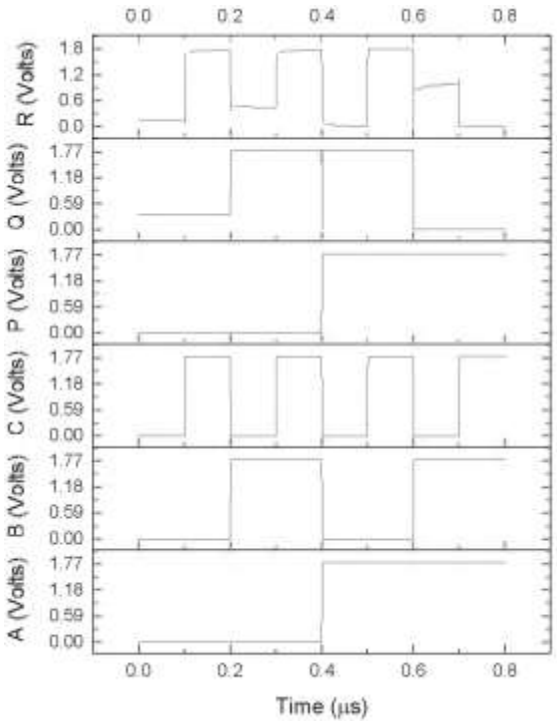


Fig. 15. Simulation input and output wave-form

Results obtained from TSPICE simulations implemented at room temperature in a standard 180nm CMOS are shown here. Initially supply voltage was taken to be 1 V and then increased by 0.2 V in each step, up to 2 V. As a result of those simulations we have provided the simulation input patterns with output wave-forms at a supply voltage of 1.8V in Fig. 15 as well as the average power dissipation and delay curves in Fig. 16 below. The output wave-forms show some degradations in voltage levels. But it does not bring a considerable change in the desired output, and so may be accepted in order to minimise the number of transistors used.

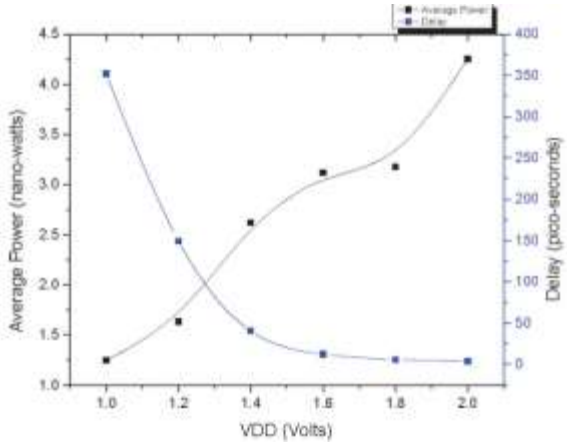


Fig. 16. Average Power Dissipation and Delay Curves

E. TS Gate(TSG)

TS Gate or TSG [6] [7] [8] is a 4*4 reversible one-through gate which is adept at computing Boolean operations. Fig. 17 shows TSG having four inputs and outputs each.

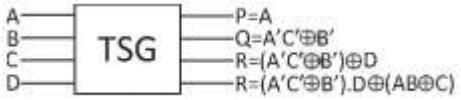


Fig. 17. Block diagram of TSG

a) Schematic of TSG in transistor level

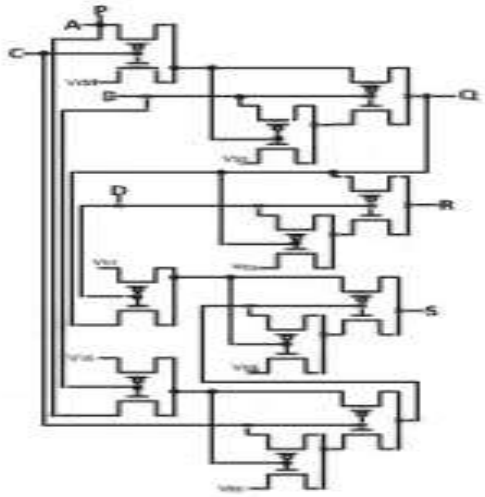


Fig. 18. Schematic of TSG in transistor level

Fig. 18 gives the circuit diagram of TSG. This implementation is fully reversible. Therefore, the output (P) that can be obtained by passing the input (A) is not a garbage output (garbage output refers to an output neither utilized as a primary output nor as any input to other gates), keeping in mind that there is provision for computing the output from input terminal and the converse is also true. The said implementation involves 22 transistors.

b) Results of Simulation

Effective simulations have been carried out using TSPICE at 298K (room temperature) with CMOS of channel length 180nm. Voltage ranging from 1.2 V to 2 V have been supplied, with steps of 0.1 V. As a result of those simulations we have provided the simulation input patterns with output wave-forms at a supply voltage of 1.8V in Fig. 19 as well as the average power dissipation and delay curves in Fig. 20 below.

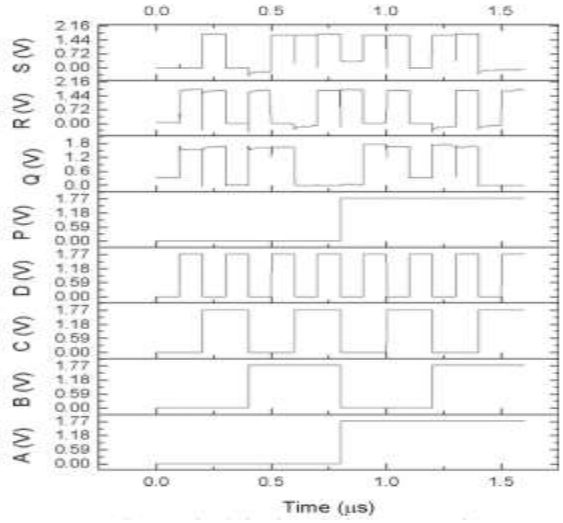


Fig. 19. Simulationinput and output wave-form

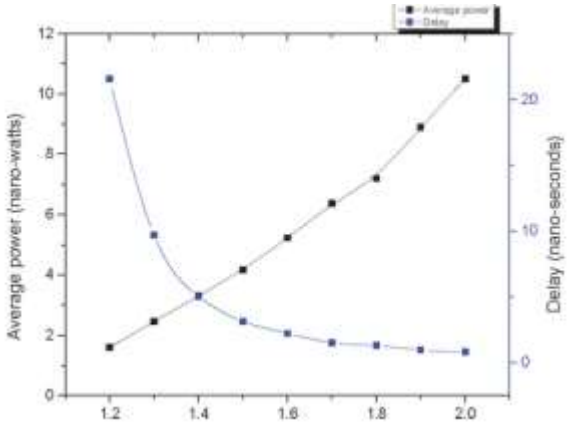


Fig. 20. Average Power Dissipation and Delay Curves

F. Reversible Full Adder using TSG

TSG can be applied to implement a full adder, completely reversible in nature [10], This implementation of full adder involves one reversible TSG and garbage outputs, two in number, are generated. Mentioned full adder is given in Fig. 21.

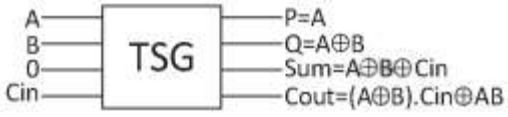


Fig. 21. Block diagram of Full Adder using TSG

a) Schematic ofReversible Full Adder in transistor level Fig. 22 gives the fully reversible transistor-level circuit Of the above-mentioned full adder. This is constructed by modifying the transistor-level schematic of TS Gate by withdrawing unused transistors. Here, the third input of TS Gate gets zero as input. Therefore, the complexity associated with computation of output is decreased, and number of

garbage outputs have been reduced to one during transistor implementation. 18 transistors have been used in the construction.

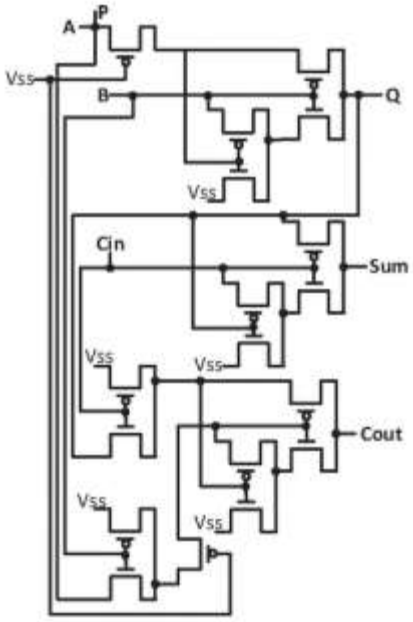


fig 22: schematic of reversible full adder in transistor level

b) Results of Simulation

Effective simulations have been performed using TSPICE with room temperature set to 298K. 180nm CMOS has been used. Voltage ranging from 1.4 V to 2.4 V with intermediate steps of 0.2 V have been provided. As a result of those simulations we have given the simulation input patterns with output wave-forms at a supply voltage of 1.8V in Fig. 23 as well as the average power dissipation and delay curves in Fig. 24 below.

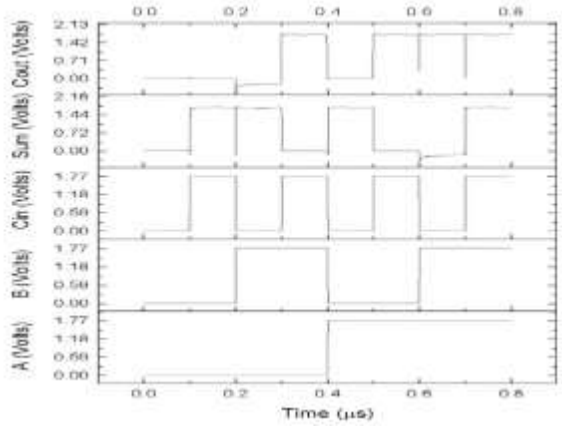


Fig. 23. Simulation input and output wave-form

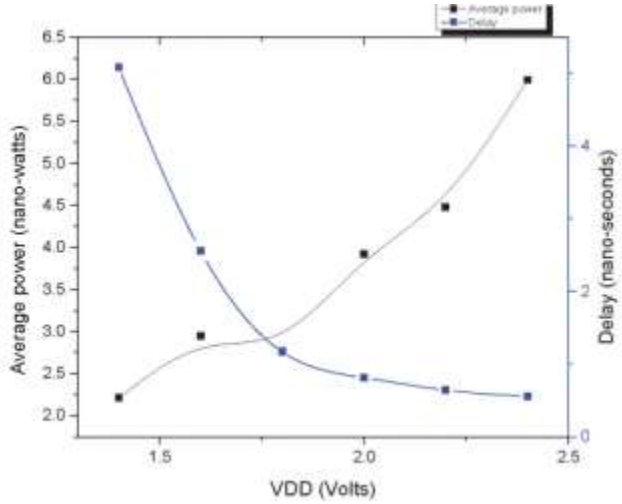


fig 28:average power diddipation and delay curves

CONCLUSION

Reversible logic thus aids in designing circuits with high speed and low power, as no information is lost by them and heat dissipation is minimum. The designs evaluated in this paper are suitable for constructing complex circuits based on reversible logic since they can be conveniently implemented in silicon. However, these reversible circuits can be implemented by multi-gated MOSFETs, Tunnel FETs etc. instead of using planar MOSFET. Due to better electrostatic control, multi-gated MOSFETs can diminish the short channel effects and reduce the power dissipation and delay of the logic circuits significantly. TFET also can be a promising alternative for the design and implementation of the low power reversible logic circuits in subthreshold regime. Authors have left these as future scope of the proposed work.

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