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IMPLEMENTATION OF LOW AREA MULTIPLIERS USING MODIFIED GATE DIFFUSION INPUT TECHNOLOGY

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ABSTRACT:

This project presents a design of 4-bit multiplier using full adder cell based on full swing gate diffusion input technique. The proposed adder design consists of 18 transistors and compared with different logic styles for full adders through cadence virtuoso simulation based on TSMC 25nm models at a supply voltage of 1v and frequency 250MHz. The simulation results showed that the proposed full adder design dissipates low power while improving the area and provides full swing output voltage among all the designs taken for comparison. The proposed full adder used to design Array, Barun and Baugh Wooley multipliers, Energy and Transistor count of these multipliers improved compared to CMOS.

1.0 INTRODUCTION:

Currently, there is a strong need for accelerated development in multimedia and digital communication technologies, real-time signal processing including voice, image and video processing .. Most applications such as processors and processing of digital signals, like filtering, uncertainty transformation, require some kind of integration, such as multiplication, multiplication and accumulation (MAC) and operation and subtraction. subtraction.

ADDERS:

Adders are logic gate combinations which combine binary values to get a number. They are graded by their ability to take and merge the numbers. In this section the fourth source, half adders and full supplements will be discussed. A quarter adder is a circuit which can add two digits, but does not produce a bring.

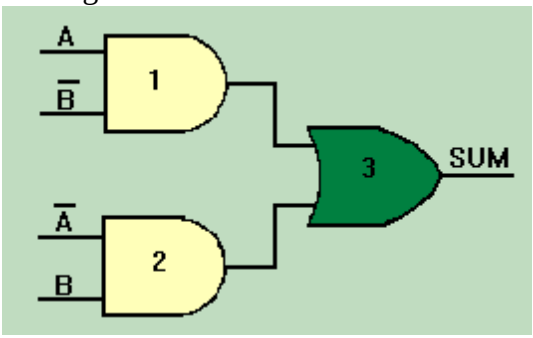

Figure 1. - Quarter adder

HALF ADDER

A half adder is designed to merge two numbers with a carry. Figure 2 shows two ways to construct a half adder. An AND gate to produce the carry is inserted in parallel with the fourth

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adder. The SUM column of the Table of Truth represents the quarter adder output and the CARRY column represents the AND gate output.

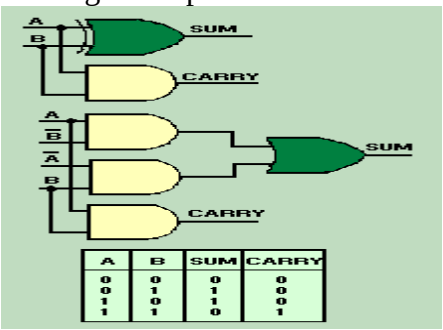

Figure- Half adders and Truth Table.

We found that the value of the adder for the quarter is Low but not Low for any value. The AND gate is triggered and there is a carry only when each of the inputs are HIGH. The highest volume of half adder is 102 (12 + 12).

LITERATURE REVIEW:

[1] Tripti Sharma, K.G.Sharma (2010) Full adder is an important factor in the architecture and construction of all types of manufacturers. Processors for optical signal (DSP), microprocessors, Additions are the central component of complex arithmetic operations, such as addition , multiplication, division, etc. Adder is in the critical line of each of these systems, which influences the average speed of the system. Improving the output of the full one-bit adder cell is therefore an essential goal.

[2] Rajkumar Sarma1 (2012) Adder cells using Gate Diffusion Technique (GDI) & PTL-GDI technique are described in this paper. GDI technique allows reducing power consumption, propagation delay and low PDP (power delay product) whereas Pass Transistor Logic (PTL) reduces the count of transistors used to make different logic gates, by eliminating redundant transistors. Performance comparison with various Hybrid Adder is been presented.

[3] A. Morgenshtein, (2010). The Gate diffusion input (GDI) process, consistent with CMOS, is proposed for this article. The GDI approach allows a wide variety of dynamic logic functions with only two transistors to be introduced. This approach is ideal for developing low-capacity logic gates with much narrower areas than Static CMOS and PTL systems.

INTRODUCTION TO VLSI

- VLSI is an implementation technology for electronic circuitry-analog or digital.
- This involves the creation on the surface of a semiconductor crystal of interconnected switches and gates.
- Microprocessors, HPCs, microcontrollers.
- DRAM / SRAM. For memory.
- ASICS (CD players, DSP applications) for special needs processors.

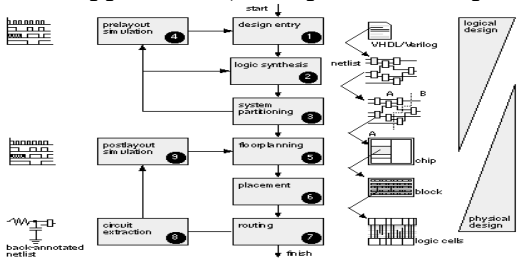

Fig : Typical ASIC Design Flow.

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Study on FPGA (various technologies):

1. Xilinx Series:
   - ❖ XC3000 Series.
   - ❖ XC4000 Series.
   - ❖ Spartan Series.
   - ❖ Vertex Series.
2. **Altera Series:**
   - ❖ System On Chip
3. **Technological Advances:**
   - ❖ Chips containing millions of transistors
   - ❖ Transistors gate lengths are in order of nanometers
4. **Consequences:**

   Components attached to a printed circuit board are only usable on a single chip.

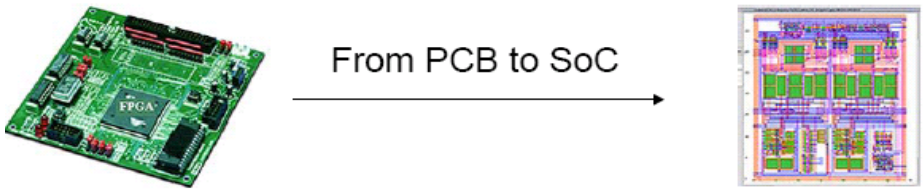


Figure: Altera Series.

A Typical SoC Design flow:

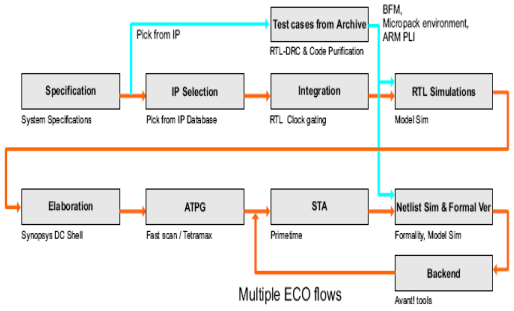


Figure: A Typical SoC Design flow.

Physical design flow in designing System-on-Chip:

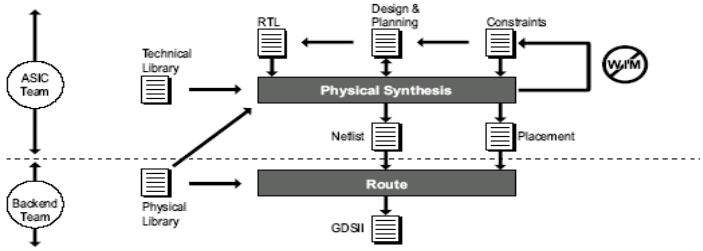


Figure: Physical design flow in designing System-on-Chip.

GATE DIFFUSION INPUT METHOD

In the year 2002 [3] A. A. Fish & A. Morgenshtein As an alternative to CMOS logic architecture the Gate Diffusion Technique (GDI) suggested by Wagner for low power and limited silicone areas of VLSI computer design. Proposed GDI cells shown in Figure 1(a)

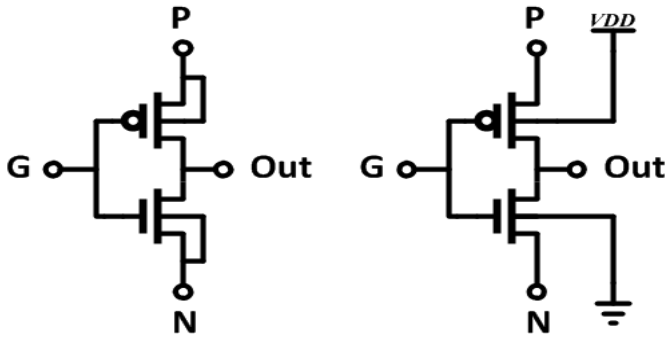


Figure: GDI cell; (a) Primitive Proposed GDI Cell, (b) MOD-GDI

This method is specifically recommended for silicone insulator (SOI) and double-bell CMOS processes manufacturing. This also provides an efficient method for designing fast, low-power designs using fewer transistors than CMOS, PTL and TG techniques. It makes it possible to implement a variety of complex functions with just 2 transistors as seen in Table I.

TABLE I. Different logic functions realization using GDI cell

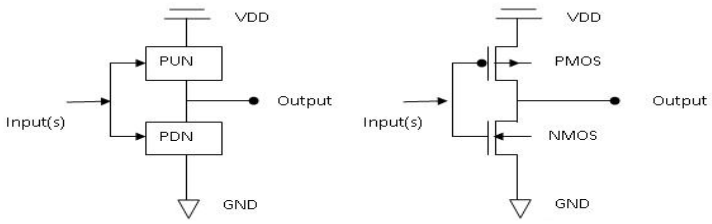
N	P	G	OUT	Function
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{\ }+B$	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}B+AC$	MUX
0	1	A	$\bar{\ }$	NOT

This logic has some limitations, such as the low threshold voltage, that means the high or low voltage is deviated by threshold voltage drop from the VDD or GND, because that threshold drop causes a decrease in efficiency and an increase in power. This logic design is based on a lowered output voltage.

CMOS & its Fabrication

CMOS has characteristics very similar to the perfect family theory. The perfect family of logic does not dissipate any electricity, has no time spread, regulated ups and downs and has a strong tolerance to noise.

The transistors of NMOS and PMOS are not suitable for switching. NMOS pass solid '0' but weak and degraded '1' (pull not above VDD-Vtn), while PMOS pass solid '1' but weak or degraded '0 (pull not below |Vtp|). NMOs are also the best way to take down a network, while PMOS is the best way to bring it up.



CMOS gates generate '0' or '1' at all times. The PMOS transistor should be closed when there is a gate voltage-the output is zero, depending on the correct polarities. The NMOS transistor is closed with gate voltage zero, the PMOS is opened and the output is VDD.

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EXISTING METHOD

Today, omnipresent computer devices are an inseparable part of everyday life. A substantial portion of the computer infrastructure is composed of digital circuitry, such as microprocessors, wireless communication machines and digital signal processors. When the deployment rate rises, the efficiency of the device is constrained by increased power levels [1] and field utilization. The manufacturers are also trying to reduce the energy usage and area of battery powered portable devices such as cell telephones, tablets and laptops while retaining their size, provided that they are increasing in popularity and demand.

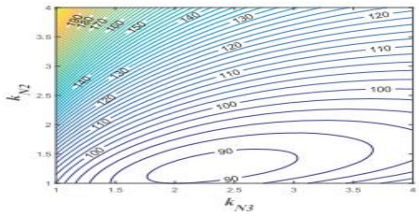

Fig. 3. Normalized PDP with $a = 3$ for $1 \leq k_{N2}, k_{N3} \leq 4$.

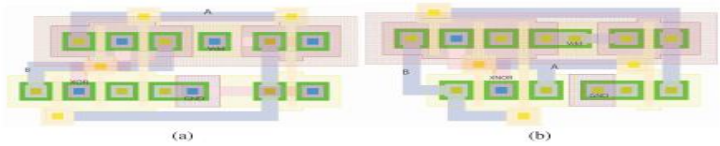

Fig. 4. Circuit layout of proposed XOR/XNOR. (a) Circuit layout of proposed XOR. (b) Circuit layout of proposed XNOR.

Where Cgmin is a transistor 's gate capacitance, and Ctotal's all the conversion capabilities. By taking Cdmin = C and a = 3 (transistor type P2, P3 and N4 relative to Wmin) PAB=10→11 = ((kN2 + kN3)C + (3 + kN2)C + kN3C + 3C)VDD 2 = CVDD 2(2kN2 + 2kN3 + 6). (4) Finally, the PDP of the circuit can be determined by the delay value and power dissipation.

TABLE I
SIMULATION RESULTS (OPTIMUM SIZE OF TRANSISTORS IN nm, POWER IN e-6W, DELAY IN ps, AND PDP IN aJ) FOR XOR/XNOR AND SIMULTANEOUS XOR–XNOR CIRCUITS IN 65-nm TECHNOLOGY WITH 1.2-V POWER SUPPLY VOLTAGE AT 1 GHz

Designs		N1	P1	N2	P2	N3	P3	N4	P4	N5	P5	N6	P6	Delay	Power	PDP
Fig. 1(a) [16]	XOR	130	610	180	130	130	130	130	262					26.1	2.48	64.7
	XNOR	195	130	130	640					130	130	155	240	25.8	2.50	64.5
Fig. 1(b) [11]	XOR	342	130	130	190	166	250							23.6	**2.14**	50.5
	XNOR	130	793					130	130	130	456			25.6	2.47	63.2
Fig. 2(b)*	XOR	130	130	330	245	170	344	130						21.9	2.22	**48.6**
	XNOR	130	130	204	732	130	578		130					**21.5**	2.46	52.9
Fig. 1(a) [16]**		223	588	191	561	130	130	130	130	130	130	130	130	33.6	4.30	144.5
Fig. 1(b) [11]**		514	876	130	130	130	205	130	130	130	527			29	4.50	130.5
Fig. 1(c) [16]		362	720	403	709	249	130	357	130	357		273		39.6	5.43	215.2
Fig. 1(d) [3]		130	483	541	154	130	178	130		430				62.7	5.31	332.9
Fig. 1(e) [13]		190	404	190	404	138	467							157.2	4.89	768.7
Fig. 1(f) [18]		130	273	187	309	130	130	130	677	373	405			38.6	4.71	181.8
Fig. 1(g) [23]		281	999	375	130	130	426	130	130	130	506			36.0	5.25	189.0
Fig. 2(e)*		130	183	144	577	130	373	130	130	130	258	242	232	**26.4**	**4.14**	**109.3**

* Means proposed design.
** This two simultaneous XOR-XNOR gates are achieved by combining of the two XOR and XNOR circuits of Fig. 1(a) and Fig. 1(b).

PROPOSED METHOD

XOR/XNOR based full adder

The complete adder is the 2 standard CMOS logic gate. 2 although a total adder equation is present as an equation

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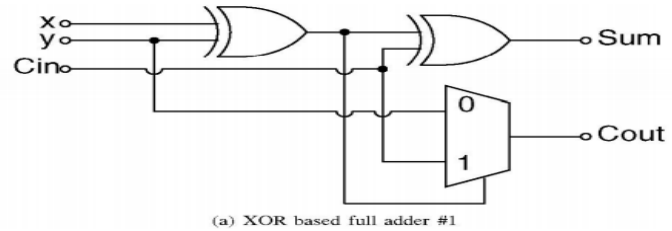
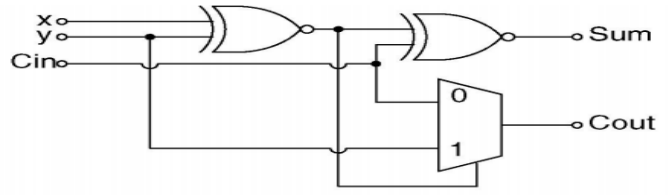
$$x + y + Cin = 2Cout + Sum \quad (1)$$
$$Cout = (y(\overline{x \oplus y})) + (Cin(x \oplus y)) \quad (2)$$
$$Sum = x \oplus y \oplus Cin \quad (3)$$
$$\text{or}$$
$$Sum = \overline{\overline{x \oplus y} \oplus Cin} \quad (4)$$

Two complete y XOR / XNOR based additionals can be updated according to equation (1) to (3) as shown in Fig. Fig. 3. (a) and 3.(b) [7] and / o.



(a) XOR based full adder #1



(b) XNOR based full adder #1

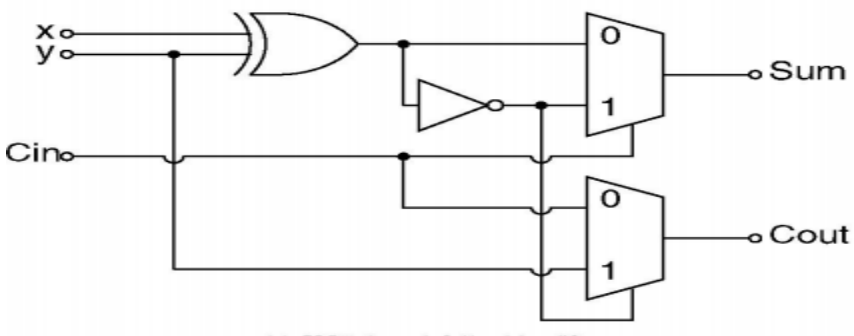
Fig. 3. XOR/XNOR based full adder

Therefore, there will be two more complete adders based on XOR / XNOR. 5. Equation GDI XOR gate (1), (2) and (4) are derived. The graphs are represented as statistics.

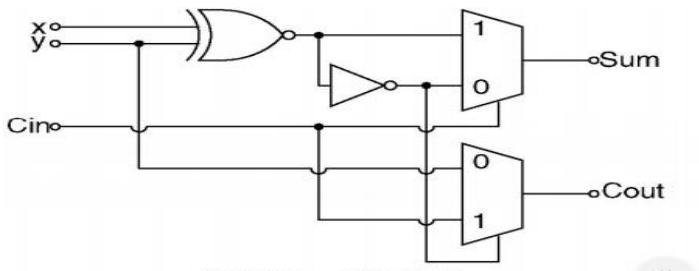
REDESIGNED XOR/XNOR/MUX GATE

A. GDI XOR

The GDI XOR door will be shown as chart. Six of which only four transistors are used. It is obvious that GDI Xor e L R. S l U Sum Gate need less transistor, as compares the GDI Xor to its traditional CMOS equivalent.



(a) XOR based full adder #2



(b) XNOR based full adder #2

Fig. 4. XOR/XNOR based full adder

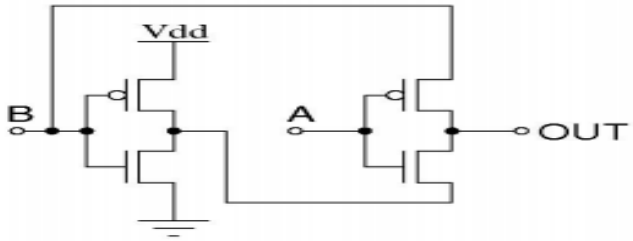


Fig. 5. GDI XOR gate

THE PROPOSED GDI FULL ADDER

We can rebuild four different styles of full GDI adder according to the 4 different complete adder architectures specified. The 4 additional ones are shown in Fig. Eight to eleven respectively. Cout All of the full suppliers proposed should be noted as 10-T. This means that the attempt is being made to create full 10-T adders.

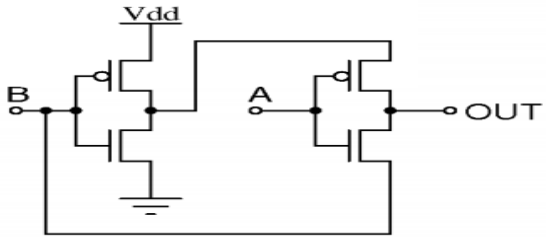


Fig. 6. GDI XNOR gate

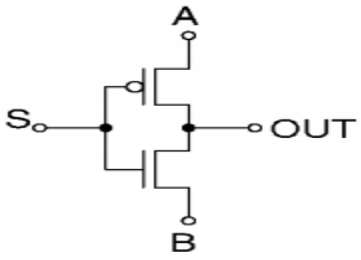


Fig. 7. GDI MUX gate

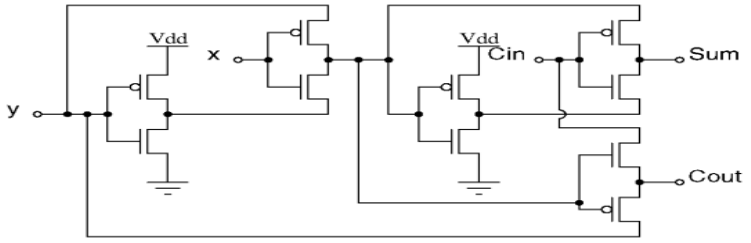


Fig. 8. GDI XOR Full Adder #1 (Based on Fig. 3(a))

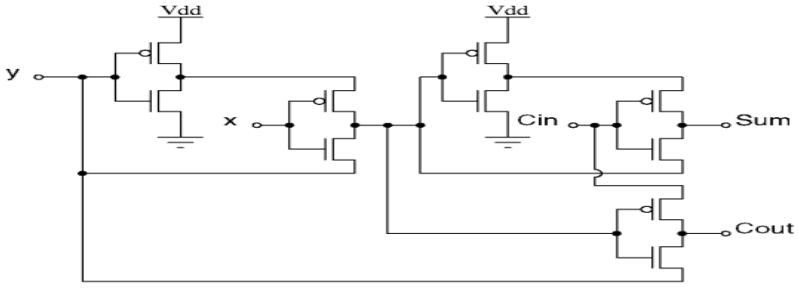


Fig. 9. GDI XNOR Full Adder #1 (Based on Fig. 3(b))

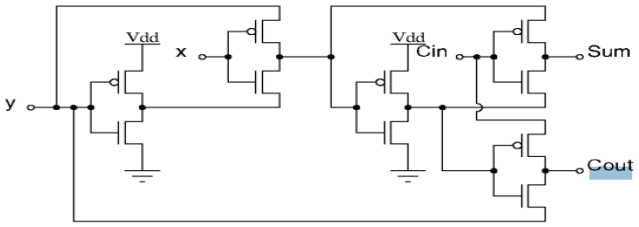


Fig. 10. GDI XOR Full Adder #2 (Based on Fig. 4(a))

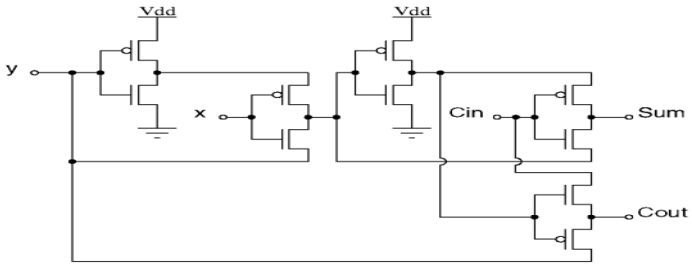
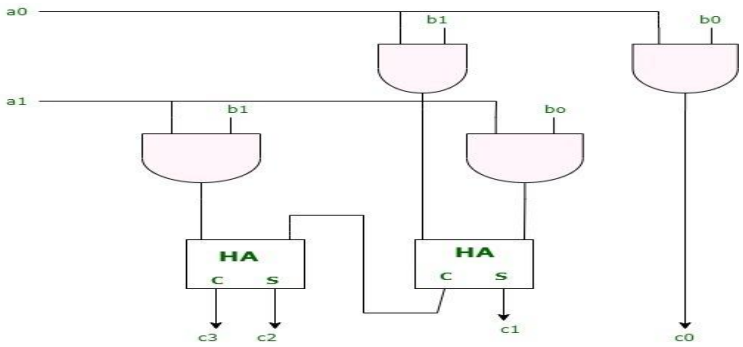


Fig. 11. GDI XNOR Full Adder #2 (Based on Fig. 4(b))

Array Multiplier in Digital Logic

An array multiplier is a digital combination circuit used to multiply two binary numbers with a full and half adders array. This framework is used to incorporate the relevant product words almost simultaneously. A sequence of AND gates is used before the Adder sequence to define the separate component names. A sequence operation which requires a sequence of additional and shift micro-operations is checked at a time by multiplier's bit and part products. With one micro-operation, a combinational circuit that forms the product bits all at once can be carried out to multiply two bi-numbers.



Array is the shortest parallel multiplier form. This multiplier uses the traditional add and move operation based on the algorithm 'load and change' to execute a multiplication operation. The 4-bit multiplier frame structure as seen in fig. 3. The partial product generator consists of n the number of ' AND 'gates to subtract the multiplicand by each multiplier bit and then these partial products can be shifted on a complete adder and a half adder depending on the request. For a 4x4 multiplier, the 4x4 AND gates are used to produce partial products and 4x(4-2) complete adders.

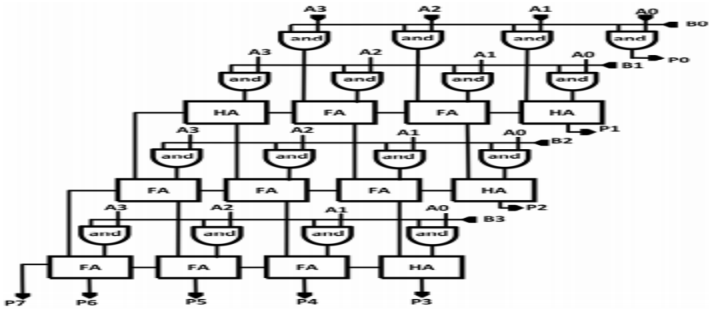


Fig. 3. 4x4 Array Multiplier

Barun Multiplier

Barun multiplier is a linear multiplier, known as a carry-save multiplier with a normal form. The multiplier functions as "carrying bits," which are outputs for the first stage but are reserved for the next stage implementation, are not added automatically. As in the photo. 4. 4x4 Brown multiplier comprising of (4-1) carry-save adders (CSAs) rows and a (4-1) bit ripple-carry adder for the final row of (4-1), total Adder (FAs) for each row. Barun has the key advantage that only one critical path is encountered rather than a variety of paths in the array multiplier and this is the most common in DSP implementations because of its low power consumption.

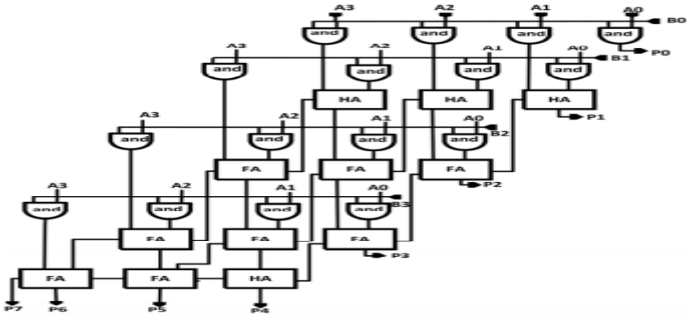


Fig. 4. 4x4 Barun Multiplier

BASEPAPER RESULTS

Design	Power (uW)	Delay (pS)	PDP (e-18J)	No.of Transistors
Array Multiplier-CMOS	53.8	146	7854.8	400
Array Multiplier-GDI	109	159	17331	296
Array Multiplier-FSGDI	44	133	5852	260
Barun Multiplier-CMOS	48.5	133.5	6474.7	400
Barun Multiplier-GDI	78.9	189	14912	296
Barun Multiplier-FSGDI	38.5	230	8855	260
Baugh Wooley Multiplier-CMOS	55	160	8800	532
Baugh Wooley Multiplier-GDI	121	187	22627	382
Baugh Wooley Multiplier-FSGDI	47	145	6815	366

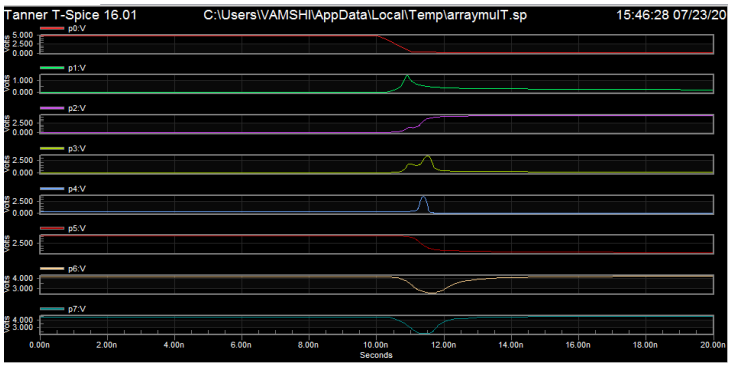


Figure 1: simulation output

```
          MOSFETs -     136
MOSFET geometries -       2
  Voltage sources -       9
       Subcircuits -      28
Model Definitions -       2
  Computed Models -       2
Independent nodes -     204
   Boundary nodes -      10
      Total nodes -     214
```

Figure: transistor count

CONCLUSION:

This work presents a 10 T complete addition, designed with the Full-Swing GDI technique and simulated using the Virtuoso simulator of Cadence in the 65 nm TSMC process. The findings of the numerical simulation showed an increase in power consumption, delay and the count of transistors while maintaining the maximum swing function in contrast to other methods. The proposed array multiplier showed 35% energy improvement, 34% energy improvement for the proposed barn multiplier and 32% power improvement in the proposed Baugh Wooley multiplier, compared with CMOS and reported better energy, delay and energy results as

compared to GDI multipliers. This work will be suitable in the future for designing filters for DSP applications.

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