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HIGH SPEED ROBUST VEDIC MULTIPLIER USING 4-2 AND 5-2 COMPRESSORS

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ABSTRACT:- Now a days the speed of the multipliers is constrained by the speed of the adders used for partial product expansion. In this Project, we proposed a 4-bit multiplier using a Vedic Multiplier. Vedic multiplier estimation is used to enhance the execution sufficiency of the cerebrum boggling tallies. In this project, we proposed a novel dual quality 4:2 compressor and two 5:2 compressors outlining. In this arrangement, we decreased lethargy and area width. In the proposed diagram we have reduced the amount of method of reasoning levels, accordingly diminishing the basis delay. In the proposed plot we have reduced the measure of premise levels, thusly diminishing the strategy for thinking deferral. Redirection of the setup is done utilizing Xilinx ISIM and facilitated utilizing Xilinx XST. Proposed compressor diagrams have demonstrated favored execution over existing Vedic algorithm based algorithm.

I.INTRODUCTION

Arithmetic operation such as addition, subtraction, division and multiplication, among these a multiplier is discussed, which are used in the ALU (Arithmetic Logical Unit) and DSP. There are more multipliers among them the Vedic multiplier also called as Urdhva Triyakbyam Sutra [2] is utilized which reduces power and area efficient multiplier. Compressors are basic components used for propagating and generating operation [5] .Architecture can use the compressor in many ways according to the basic concept. It cannot achieve the three parameters power, delay and area there will be tradeoff or compromising. For the Fast addition processes compressors are used in multiplier architecture. The main aim of compressors is to increase the performance and reduce the cell area. S.F.Hsiao et al proposed 3:2 compressor which is a combination of multiplexer and Exor in which the performance increases and area reduces. Here we are using 4:2 and 5:2 proposed by Sreehari et al [5].

II.BACKGROUND ON COMPRESSORS

Compressor 4:2

The 4-2 Compressor have 5 inputs A, B, C, D and C into give 3 output Sum, Carry and Cout as appeared in Figure 1(a). The 4 inputs A, B, C and D and the output Sum having same piece estimate. The information Cin is the output from a past lower compressor and the Cout output is for the compressor. The ordinary way to deal with actualize 4-2 compressors is with two full adders associated in serially as appeared in Figure 1(b).

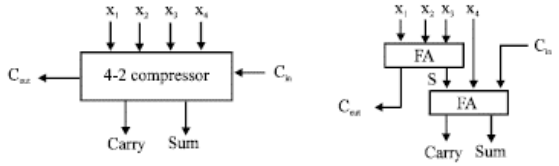


Fig: 1(a) 4-2 adder Compressor.(b) 4-2 adder compressor implemented with full adders.

Exact 4:2 Compressor

To reduce the delay of the partial product summation stage of parallel multipliers, 4:2 and 5:2 compressors are widely employed [18]. Some compressor structures, which have been optimized for one or more design parameters (e.g., delay, area, or power consumption), have been proposed [18], [19]. The focus of this paper is on approximate 4:2 compressors. First, some background on the exact 4:2 compressor is presented. This type of compressor, shown schematically in Fig. 2, has four inputs (x1–x4) along with an input carry (Cin), and two outputs (sum and carry) along with an output Cout. The internal structure of an exact 4:2 compressor is composed of two serially connected full adders, as shown in Fig. 1. In this structure, the weights of all the inputs and the sum output are the same whereas the weights of the carry and Cout outputs are one binary bit position higher. The outputs sum, carry, and Cout are obtained from

$$\text{sum} = x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin \quad (1)$$

$$\text{carry} = (x1 \oplus x2 \oplus x3 \oplus x4)Cin + \overline{(x1 \oplus x2 \oplus x3 \oplus x4)}x4 \quad (2)$$

$$\text{Cout} = (x1 \oplus x2)x3 + \overline{(x1 \oplus x2)}x1. \quad (3)$$

III Proposed Dual-Quality 4:2 Compressors

The proposed DQ4:2Cs operate in two accuracy modes of approximate and exact. The general block diagram of the compressors is shown in Fig. 2. The diagram consists of two main parts of approximate and supplementary. During the approximate mode, only the approximate part is exploited while the supplementary part is power gated. During the exact

operating mode, the supplementary and some parts of the approximate parts are utilized.

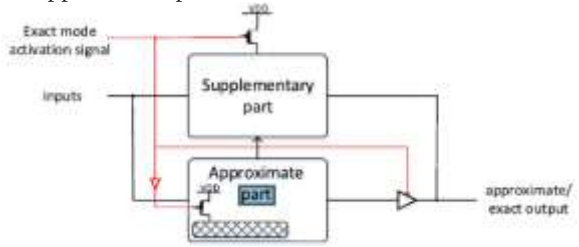


Fig 2. Block diagram of the proposed approximate 4:2 compressors.

In the proposed structure, to reduce the power consumption and area, most of the components of the approximate part are also used during the exact operating mode. We use the power gating technique to turn OFF the unused components of the approximate part. Also note that, as is evident from Fig. 2 in the exact operating mode, tristate buffers are utilized to disconnect the outputs of the approximate part from the primary outputs. In this design, the switching between the approximate and exact operating modes is fast. Thus, it provides us with the opportunity of designing parallel multipliers that are capable of switching between different accuracy levels during the runtime. Next, we discuss the details of our four DQ4:2Cs based on the diagram shown in Fig. 2. The structures have different accuracies, delays, power consumptions, and area usages. Note that the *i* th proposed structure is denoted by DQ4:2C*i*. The basic idea behind suggesting the approximate compressors was to minimize the difference (error) between the outputs of exact and approximate ones. Therefore, in order to choose the proper approximate designs for the compressors, an extensive search was performed. During the search, we used the truth table of the exact 4:2 compressor as the reference.

Structure 1 (DQ4:2C1): For the approximate part of the first proposed DQ4:2C structure, as shown in Fig. 3(a), the approximate output carry (i.e., *carry_*) is directly connected to the input *x*4 (*carry_ = x*4), and also, in a similar approach, the approximate output sum (i.e., *sum_*) is directly connected to input *x*1 (*sum_ = x*1). In the approximate part of this structure, the output *C*out is ignored.

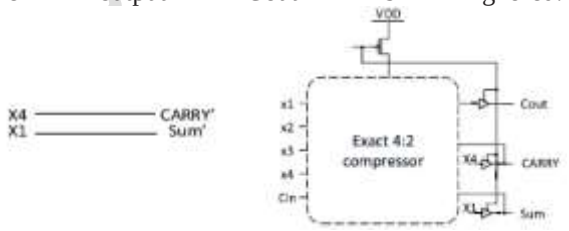


Fig 3. (a) Approximate part and (b) overall structure of DQ4:2C1.

While the approximate part of this structure is considerably fast and low power, its error rate is large (62.5%). The supplementary part of this structure is an exact 4:2 compressor. The overall structure of the proposed structure is shown in Fig. 3(b). In the exact operating mode, the delay of this structure is about the same as that of the exact 4:2 compressor.

Structure 2 *(DQ4:2C2):* In the first structure, while ignoring *C*out simplified the internal structure of the reduction stage of the multiplication, its error was large. In the second structure, compared with the DQ4:2C1, the output *C*out is generated by connecting it directly to the input *x*3 in the approximate part. Fig. 4 shows the internal structure of the approximate part and the overall structure of DQ4:2C2. While the error rate of this structure is the same as that of DQ4:2C1, namely, 62.5%, its relative error is lower.

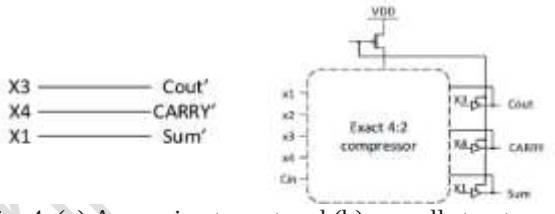
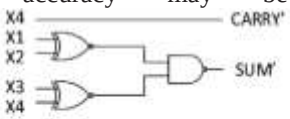


Fig. 4. (a) Approximate part and (b) overall structure of DQ4:2C2.

***Structure* 3** *(DQ4:2C3):* The previous structures, in the approximate operating mode, had maximum power and delay reductions compared with those of the exact compressor. In some applications, however, a higher accuracy may be needed.



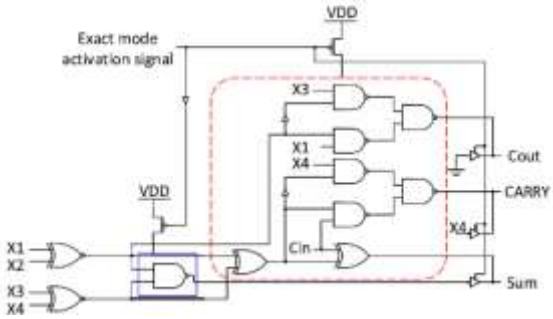


Fig. 5. (a) Approximate part of DQ4:2C3 and (b) overall structure of DQ4:2C3.

In the third structure, the accuracy of the approximate operating mode is improved by increasing the complexity of the approximate part whose internal structure is shown in Fig. 5(a). In this structure, the accuracy of output *sum_* is increased. Similar to DQ4:2C1, the approximate part of this structure does not support output *C*out. The error rate of this structure, however, is reduced to 50%. The overall

structure of DQ4:2C3 is shown in Fig. 5(b) where the supplementary part is enclosed in a red dashed line rectangle. Note that in this structure, the utilized NAND gate of the approximate part (denoted by a blue dotted line rectangle) is not used during the exact operating mode. Hence, during this operating mode, we suggest disconnecting supply voltage of this gate by using the power gating.

***Structure* 4** *(DQ4:2C4):* In this structure, we improve the accuracy of the output *carry_* compared with that of DQ4:2C3 at the cost of larger delay and power consumption where the error rate is reduced to 31.25%. The internal structure of the approximate part and the overall structure of DQ4:2C4 are shown in Fig. 6. The supplementary part is indicated by red dashed line rectangular while the gates of the approximate part, powered OFF during the exact operating mode, are indicated by the blue dotted line. Note that the error rate corresponds to the occurrence of the errors in the output for the complete range of the input.

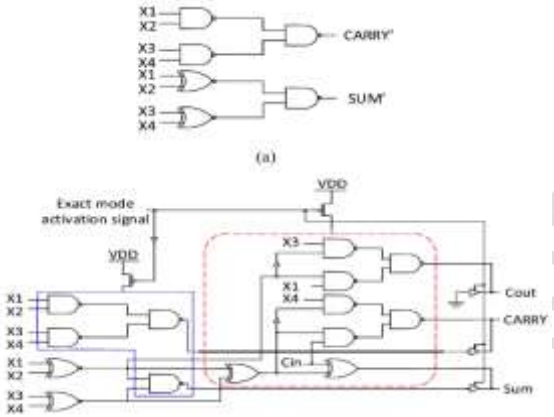


Fig. 6. (a) Approximate part of DQ4:2C4 and (b) overall structure of DQ4:2C4.

IV Compressor 5:2 proposed by Sreehari

When ever these types of full adders are swapped with their constituent blocks of EXOR gates .It can be observed that the overall delay is equal to 6*-EXOR for the propagator or generator output. The models have been proposed by [5] where the postponement has been lessened to 4*-EXOR as appeared in fig.7.

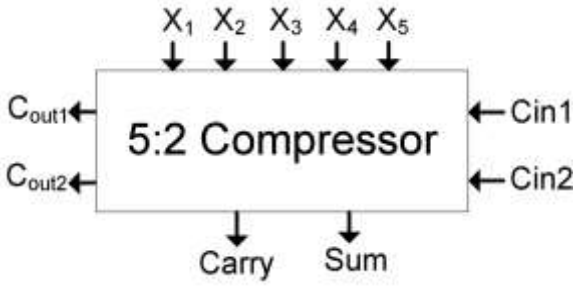


Fig :7.5:2 compressor.

III. BACKGOUND ON MULTIPLIERS

A. Vedic Multiplier

In Vedic mathematics, there are sixteen sutras, which are prepared by the ancient sages of India. It was discovered by the Jagadguru swami Sri Bharatikrishna Tirthaji maharaja during 1911 and 1918 [2]. By using this algorithm, there are many different types of compressors(cm) such as 3:2, 4:2 and 5:2 compressors been proposed. In this work, we used the Vedic algorithm based partial product operation for improving the performance, delay and less area occupancy

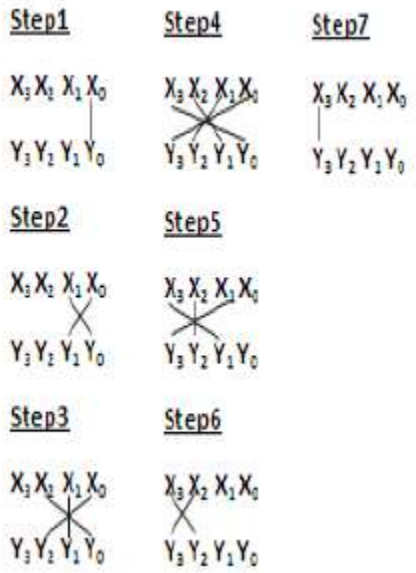


Fig: 8.Basic diagram of Vedic 4x4 multiplication.

In this paper we apply similar musings to the parallel number framework to make the proposed calculation perfect with the advanced gear. It is a general augmentation recipe proper to all cases of duplication. It really implies "Vertically and transversely". The calculation can be summed up for n x n bit number. Since the partial things and their totals are figured in parallel, the multiplier is of the clock repeat of the processor. The Multiplier in light of this sutra has the favorable position that as the quantity of bits builds, gate postponement and territory increments gradually when contrasted with other convolutional multipliers.

To illustrate this plan, let us consider the multiplication of two decimal numbers 252 * 846 by Urdhva Tiryakbhyam strategy as appeared in Figure 5. The digits on the both sides of the line (say, 2 and 6) are multiply by (6 x 2 = 12) and included with the carry from the past stride (at first, carry=0). This

creates one of the bits of the outcome (i.e. 2) and a carry (i.e. 1). This carry (1) is included the following stride and subsequently the procedure goes on. On the off chance that more than one line there in one stage, every one of the outcomes are added to the past carry. In every progression, Least Significant Bit (LSB) goes about as the outcome bit and every other piece go about as carry for the following stride. At first the carry is taken to be zero.

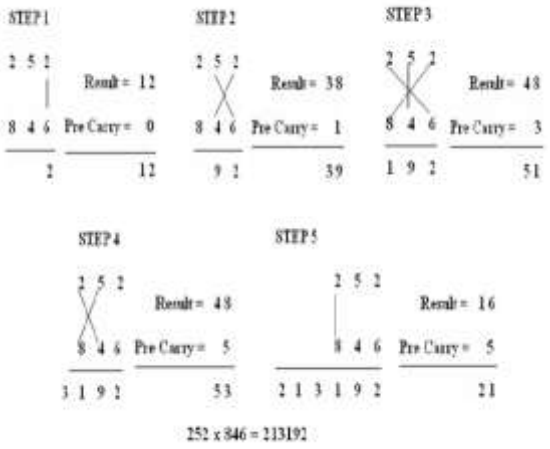


Figure 9: Multiplication of two decimal numbers 252 * 846.

V. SIMULATION RESULT

The result of proposed compressor 5:2 architecture1 is around 5.61 percentage less cell area and 3.32 percentage faster than existing 5:2 compressor(3).

Fig.5.simulation of vedic multiplier.

Fig.7. Area report of vedic multiplier.

The proposed compressor 5:2 architecture2 is around 2.80 percentage less cell area and 0.81 percentage faster than existing 5:2 compressor. The coding is done in Verilog HDL and synthesized on Xilinx 14.6.

VI CONCLUSION

In this project, new engineering compressors are exhibited. These compressors execution is assessed on Vedic Multiplier as far as speed or postpone, Area is thought about utilizing 180nm standard cell innovation of computerized Cadence instruments and orchestrated in Xilinx RTL complier. The outcomes have appeared in this project 6.77 percentage reduces in area and 7.04 percentage quicker than existed compressor when 5:2 compressor architecture1 is utilized. Furthermore around 3.00 percentage lessening in cell area with 5.62 percentage speedier than existed compressor utilizing 5:2 compressor architecture2.

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