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LOW POWER IMPLEMENTATION OF ASK, FSK, PSK DIGITAL MODULATION TECHNIQUES USING VERILOG

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Abstract—This paper presents a general architectural overview regarding elementary method of VERILOG HDL based code simulation for fundamental and widely used digital modulation techniques such as Binary Amplitude-shift keying (BASK), Binary Frequency-shift keying (BFSK), Binary Phase-shift keying (BPSK) and Quadrature Phase Shift Keying(QPSK). In this work the idea of sinusoidal signals that have been generated is plain sailing in nature and based on fundamentals of signal sampling and quantization. Such concept of sinusoidal signals generation is not unfamiliar but somehow simplified using sampling and quantization in time and amplitude domain, respectively. The whole simulation is done on Model Sim and Xilinx-ISE using VERILOG Hardware descriptive language. The work has been accomplished on Thirty two bit serial data transmission with self-adjustable carrier frequency and bit duration length.

Keywords- Orthonormal, Analog, FPGA, BASK, BFSK, BPSK, QPSK, OQPSK, QAM, MSK, CPFSK, PISO

I. INTRODUCTION

Digital bandpass modulations employing amplitude, frequency and phase shift keying techniques have been in use for quite a long time. One of the major emphases behind such designs is to improve the bandwidth efficiency as well as transmission rate. Multi valued logic (MVL) systems are useful in this context. A ternary, three-valued or trivalent logic [1] is one of several multi-valued logic systems [2]. In a ternary based system, three logic levels are used(0,1,2) corresponding to low, middle and high voltage level. The boolean arithmetic using ternary logic [3],[4] had already been established[5].Several research shows that ternary logic or three valued logic provides several advantages over binary logic in the design of digital systems [6],[7],[8]. Such advantages include more information in a given register length and higher speed of operation during arithmetic and logical operations. As the hardware requirement of a ternary circuit is less in comparison to the binary counterpart, ternary circuits can be implemented with reduced complexity of interconnects and less chip area resulting speed enhancement and

significant reduction of static power dissipation. Researchers have also concentrated to design reconfigurable modulators based on binary logic suitable for different modulation and demodulation schemes without changing the underlying hardware [9]. However performance of such designs can be improved using the ternary number system. For example, using the same word length log327 the ternary logic can represent 27 different possible symbols whereas the maximum number of possible combinations using the binary logic is only 23 .

2. Literature survey:

Our project is FPGA implementation of BASK-BPSK-BFSK digital modulators .In this project each of these digital modulation technique was done using a multiplexer using coding. Here we are using minimum number of blocks[1].This section presents a broad overview of digital modulators, applications and commonly used hardware platforms for modulators. Traditional modulators are using large number of building blocks .They are quite inflexible because it is difficult to change the parameters of modulating and carrier signal ,The most commonly used methods for modulator implementation are matlab implementation ,FPGA implementation, generation with self starting optoelectronic oscillator, DSP(Digital Signal Processor), general purpose microprocessors ,graphic processing units (GPU),ASICS(Application Specific Integrated Circuit) and through hardware circuits consiting of resistors ,CD 4016 IC etc. General purpose microprocessors, such as the Intel and AMD devices usually found in personal computers, are not specialized for any particular application[2].Therefore, they are very flexible. However, SDR systems using general purpose processors are often wasteful since these processors are designed for speed and generality rather than power efficiency or mathematical operations[3].

Graphics processing units uses massively parallel architectures that are optimized for vector manipulations and other graphical operations. Such parallel designs are very well suited for signal processing, but general purpose processors are relatively difficult to program and they consume high power. A digital signal processor solve these two problems by fetching instructions and data from memory, does operations, and stores the results back to memory, just like a regular CPU[4]. The difference between a DSP chip and a CPU chip is that a DSP chip usually has a block that does high-speed signa lprocessing, especially a block called MAC (Multiply and Accumulate). By calling different routines in memory, a DSP chip can be reconfigured to perform functions. On the other hand, their narrow focus makes them slow for

other applications. ASIC (Application-specific Integrated Circuit) is an integrated circuit that is used to perform a fixed specific task[5]. Examples of signal-processing specific ASIC's are DDC (digital down converter) chip, and digital filter chips. The disadvantage of ASIC is that its functionalities are fixed and thus cannot be changed by the user according to his interest

Over the previous few decades, there has been occurred a big alteration from simple analog modulation and angle (phase/frequency) modulation methods to latest digital modulation techniques. Such digital modulation techniques have become fundamentals of satellite communication, Wireless networks and Cellular networks. In the field of telecommunication, modulation is an exercise of diverging either amplitude or angle of a periodic waveform, known as the carrier signal using a modulating signal that in general encompass information to be transmitted, called as intelligence signal. The intelligence signal can be analog or digital in nature that very much depends upon message source.

The mechanism of modulation uplifts the frequency band spectrum of transmitted signal to the range, where signals are not much attenuated in the channel. Modulation using a sinusoidal waveform transfigures a baseband electrical signal into a passband signal. The rudimentary goal of the author is to achieve a general and simplified method to simulate above stated modulation techniques to transmit data serially. The algorithm is proposed in VERILOG HDL and output signals have been simulated on Xilinx-ISE and further analyzed using Model Sim(Wave).

3. Proposed Method

The proposed ternary modulator is a multimode one which can be operated in any one of ternary ASK, FSK and PSK mode by applying the proper control signals. The proposed architecture as depicted in Fig.1 consists of multiplexers, decoders, standard ternary inverters, carrier wave generator, up converter, limiter and PMOS (P-type metal-oxide semiconductor) switches. The leftmost part of the depicted modulator is carrier signal generator, which is comprised of phase shifter, up converter, and limiter. There are three control signals A, B and C. The Control signals A and C are connected to the input of the Ternary 1:3 decoders D1 and D2 respectively whereas the third control signal B is connected to the select input line of the ternary multiplexer M4 for switching the final modulated output.

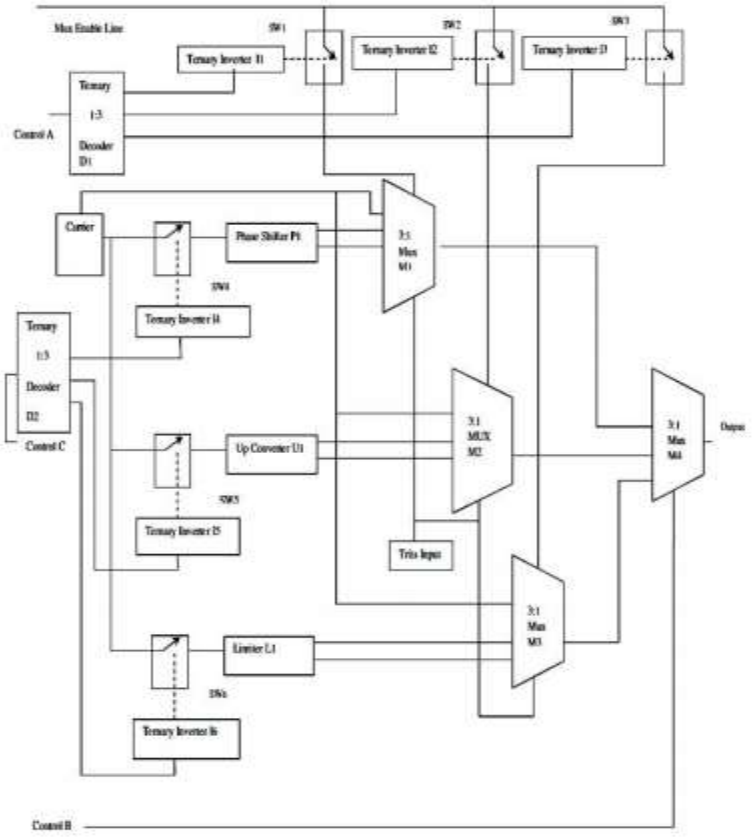
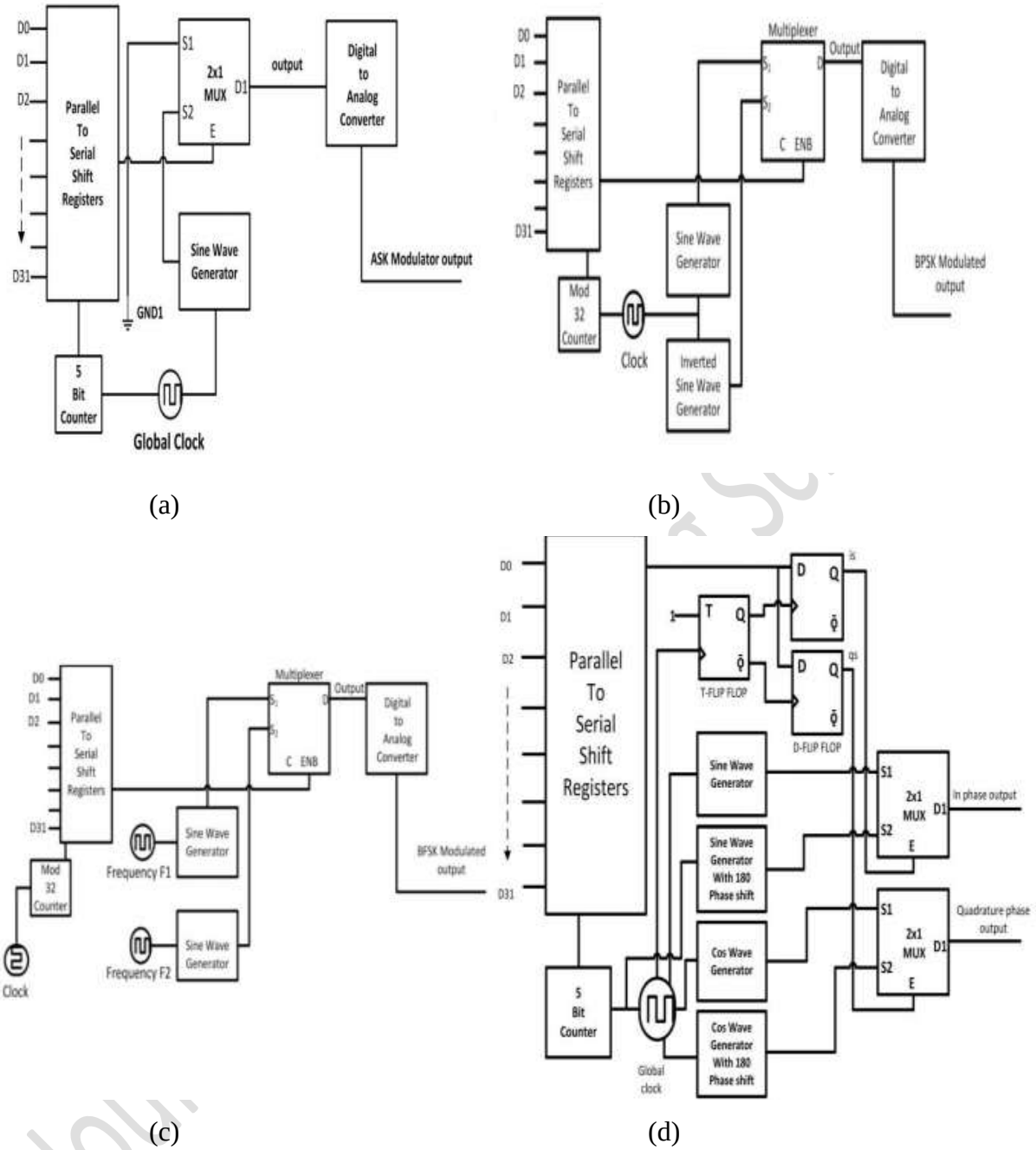


Figure 1. Architecture of the proposed modulator

Architectural overview

All the simulated modulation techniques take 32 bits inputs as the parallel data input which is need to be transmitted and one global system clock which runs every component present in system. The ground level architecture of all modulation techniques are illustrated through block diagram in Figure 2. The primary component of the architecture, the sinusoidal signal generator has been simulated by deviating the register value continuously in periodic manner of deviation. Cosine and inverted sinusoidal signal can be made by adjusting All the four symbols are represented in orthonormal signals 1(t)and2(t) as2Eb π the deviation and varying time period. At the initial stage a parallel input serial output shift register [8] is employed to convert the parallel data bits into serial stream Fig.4. Here the clock retained to the piso is slowed down using a ripple carry counter for achieving desired bit duration length. So variable bit length can be achieved from the method. For an example if global system clock of 50 MHz(For SPARTAN 3AN) [9] and the frequency divider counter is of Mod-32 than the bit duration length will be about0.64 microseconds.



(a) (b)

(c) (d)

Fig. 2. (a) Block Diagram for BASK Implementation (b) Block Diagram for BPSK Implementation (c) Block Diagram for BFSK Implementation (d) Block Diagram for QPSK Implementation

Operation of Ternary Modulator

When the control signal A= 0 the Ternary inverter I1 turns on the PMOS switch SW1 which in turn enables the multiplexer M1. In similar fashion logic 0 at control signal C turns on the PMOS

switch SW4 through the ternary inverter I4. As a result the carrier signal is routed to the multiplexer M1 through the phase shifter P1. The ternary data inputs (TRITS) are applied to the select input of multiplexer M1. According to the value of the TRITS input the carrier signals are switched from input to output of the multiplexer M1.

Now With the value of the control signal B as 0 this output of the multiplexer M1 reaches the final output of the modulator through the multiplexer M4. In this fashion, for the combination 000 of the control signals A, B and C in sequence the configurable modulator operates in Ternary Phase Shift Keying (TPSK) mode. The proposed modulator can be reconfigured [12] to act as a TFSK modulator by applying the combination 111 to the control signal A,B and C respectively. In this mode the carrier signal is fed to the input of the multiplexer M2 in its original form and in up converted form through the operation of ternary inverter I5, PMOS switch SW5 and up converter U1.

The multiplexer M2 is already enabled as the PMOS switch SW2 is turned on through inverter I2. The value of the TRITS input in the select line of multiplexer M2 switches the proper value of the carrier and gets it routed to the 2nd input of the multiplexer M4. This value in the 2nd input of the multiplexer M4 is routed to the final output of the circuit by choosing the value of B as 1 and connecting it to the select line of M4. The whole operation represents the TFSK modulation scheme. The proposed modulator can be configured [13] to operate in TASK mode by applying the logic 2 to all the control signal A.B,C respectively. The switch SW3 is on through ternary inverter I3 which in turn enables the multiplexer M3. The value 2 in control signal C switches on SW6 through inverter I6.As a result the carrier signal is connected to the 2nd and 3rd input of the multiplexer M3 through limiter L1. The carrier signal in its original form is connected to the 1st input of multiplexer M3. Now depending upon the value of the TRITS input the corresponding value from the inputs of M3 is routed to the 3rd input of M4 and that value finally reaches the final output because the value in the control signal B is 2. The whole operation supports the principle of TASK. Table-1 gives the snapshots of different building block units used for various communication schemes and the corresponding value of the control signals.

Table 1. Control signals for the different modulation schemes and the correspondin

Control Logic A	B	C	Modulation Schemes	Basic Building Blocks used
0	0	0	TPSK	D1 ,D2, I1, I4, SW1, SW4, P1, M1, M4
1	1	1	TFSK	D1, D2, I2, I5, SW2, SW5, U1, M2, M4
2	2	2	TASK	D1, D2, I3,I6, SW3, SW6, L1, M3, M4

4. Simulation Results:

Xilinx ISE is a simulation tool. It doesn't create any hardware even on the monitor. ISIM just compiles the code, check syntax of the code, and provides the waveform of the design behavior according to the inputs values defined at the Test Bench file. ISIM is a tool for the functional checking of the design. In ISIM the code is written in Verilog. The sine wave is generated using look up table approach. The values for the look up table are generated using sine function in MATLAB. This project we are using behavioural level approach. Actually in this project the carrier wave reaches a mux module,where the information signal acts like an selection input. The second phase of the project had been done in modelsim for functional verification.

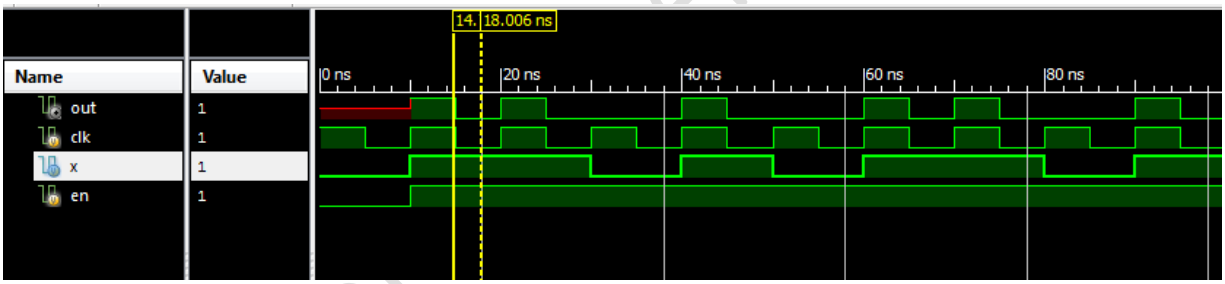


Figure 3: ASK output

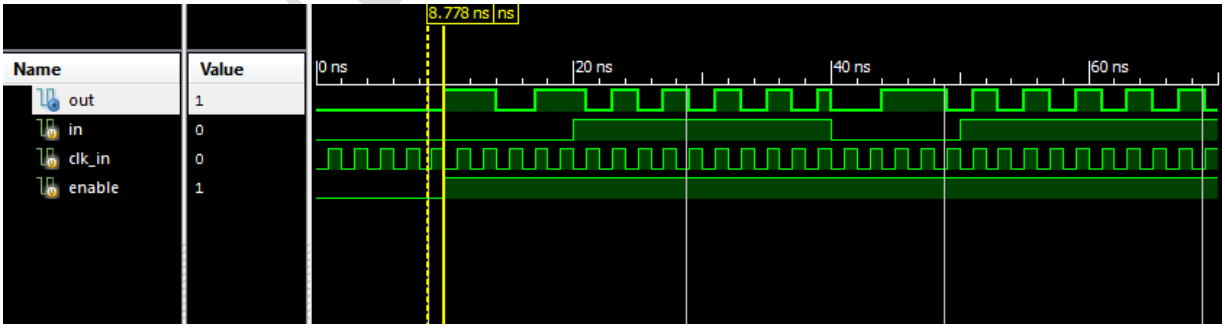


Figure 4: FSK output

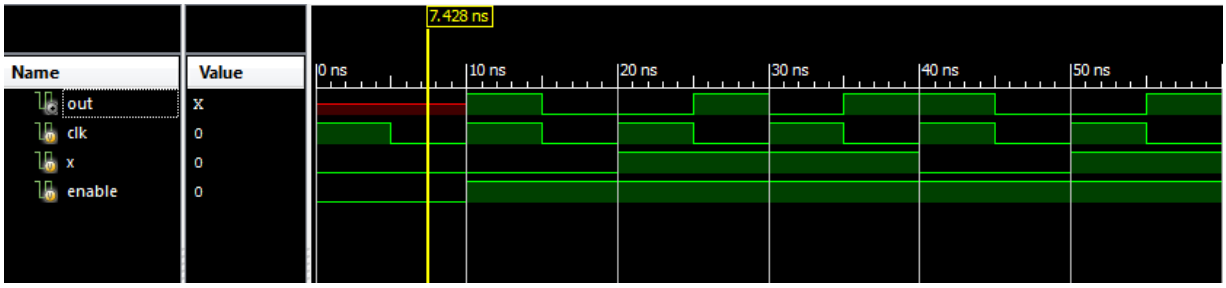


Figure 5: PSK output

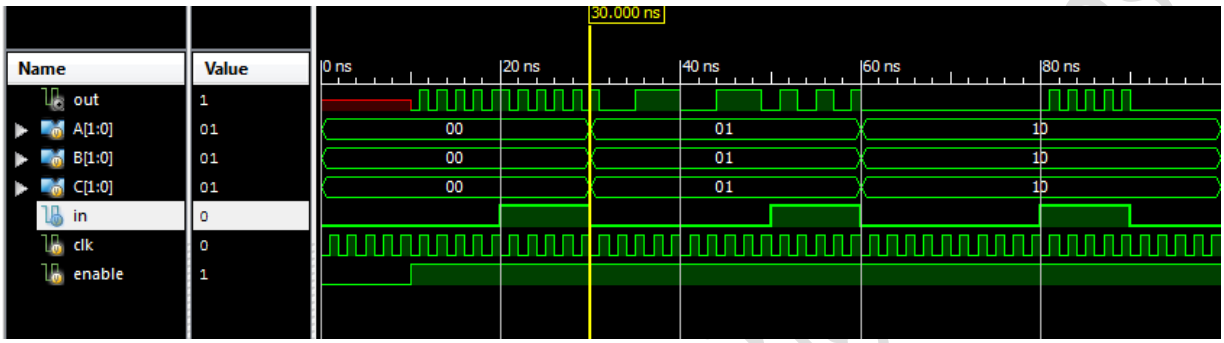


Figure 6: Entire Modulator output

Conclusion: All the above mentioned modulation techniques have been simulated successfully. Proposed method of implementation proved to be very resilient and efficient. The architecture used for the simulation purpose is mainly combinational and therefore do not contribute much propagation delay during simulation. The discussion and tabulation on power consumption, propagation delay(speed) and different area parameters i.e. piece of slice flip-flops, figures of 4 input LUTs, statistics of occupied slices, total number of 4 input LUTs used, number of bonded IOBs etc. have been accomplished. This whole simulation is tested for clock of 50 MHz frequency. Future works includes simulation of more advance modulation techniques such as Offset Quadrature phase shift keying (OQPSK), Quadrature amplitude modulation(QAM), Minimum shift keying(MSK), Continuous phase frequency shift keying(CPFSK) and more.

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