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# LOW POWER DESIGN OF COUNTER USING DIGITAL SWITCHING CIRCUITS FOR COUNTING APPLICATIONS

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*Abstract*

A low-power VLSI circuit is intended to reduce power consumption, increase battery life, and reduce area. The performance of a circuit improves as the circuit's power consumption is reduced. The number of times a procedure or event has occurred in proportion to the clock signal is stored by a scaling circuit or counter. The main issue with scaling circuits is power consumption owing to the power supply. The low power was obtained by employing True Single Phase Clock Logic (TSPCL) and Self Controllable Voltage Level (SVL) Technique to reduce power consumption in flipflops. The number of transistors and leakage power account for the majority of the power usage. By lowering the number of transistor counts, the proposed MGDI uses less power than TSPCL. TANNER EDA software is used to compare the simulation results of both MGDI and TSPCL techniques in terms of transistor count and power usage.

KEY POINTS:TSPCL SVL, TANNER EDA

## I. INTRODUCTION:

In today's world, four elements - area, speed, delay, and power consumption – are critical in driving demand for compact handheld devices such as cell phones, laptops, palmtops, and electronic devices. Area, performance, affordability, and reliability were formerly the primary considerations of VLSI designers. In the past, reliability, cost, and performance were prioritised, and power conservation was a minor consideration. However, in recent years, power has been accorded equal weight to area and speed factors. Because of increased frequencies and chip sizes, power consumption has been a critical concern in recent years. Any VLSI circuit's performance is determined by its design architecture, which optimises power and ensures high reliability. Power optimization of circuits at many levels is required to design any circuit with low power consumption. Power dissipation reduction is a critical design issue in VLSI circuits.

The majority of system-level architectures are made up of sequential circuits, and the design of these circuits has a significant impact on the system's overall power consumption. The clock wastes a lot of electricity in many synchronous applications. The clock is the sole signal that switches continuously, therefore it typically has to drive a vast clock tree. The circuit itself is divided into several blocks. The power dissipation of the clock was lowered in asynchronousapplications. Static and dynamic power dissipation contribute the most power to any circuit. Sub threshold conduction, reverse biassedpn junction conduction, gate tunnelling current, drain source punchthrough, gate induce drain leakage, and other factors cause static power dissipation in the quiescent state of the circuit. When compared to dynamic power, however, static power makes a small contribution. The transition of signal and short circuit current causes dynamic power dissipation. The transient shorting of the power source and ground during signal transition causes short circuit power dissipation. The contribution of short circuit power to dynamic power is roughly 5–10%.

The proposal of an asynchronous counter employing the Modified Gate Diffusion Input (MGDI) design methodology is the paper's key contribution. Counters are circuits that count clock pulses in a sequential order. These are one of the most basic yet crucial building blocks in the construction of very large scale integration systems. It's been utilised in nearly all electronic systems for a long time, including microprocessors, memory, communication devices, scientific apparatus, and measuring systems. It keeps track of and occasionally displays the number of times a specific event or process has occurred, usually in relation to a clock signal. Other devices receive precise timing and control signals from them. It's been utilised in nearly all electronic systems for a long time, including microprocessors, memory, communication devices, scientific apparatus, and measuring systems. It keeps track of and occasionally displays the number of times a specific event or process has occurred, usually in relation to a clock signal. Other devices receive precise timing and control signals from them. In a synchronous counter, the clock pulse is applied to all flipflops at the same time, whereas in an asynchronous counter, the clock pulse is applied to the first flipflops first, and the output of the first flipflop is used as the clock for the remaining flipflops.

Section 2 discusses the various sources of power dissipation in the remainder of this work. The existing Flip-Flop and counter method is discussed in Section 3. The suggested counter method using the Modified Gate diffusion input technology is claimed in Section 4. Section 5 contains the results and analysis of the suggested work, whereas Section 6 contains the conclusion

## II. Sources of power dissipation

The product of the total current provided to the circuit and the total voltage loss or leakage current called power dissipation.Power dissipation is an inescapable barrier when it comes to gadget portability. Costs related with packaging and cooling, standby time and battery life, digital noise tolerance, and environmental considerations are all reasons why power management is vital in System on Chip. The power dissipation is categorised into two types. They are Dynamic Power Dissipation and Static Power Dissipation

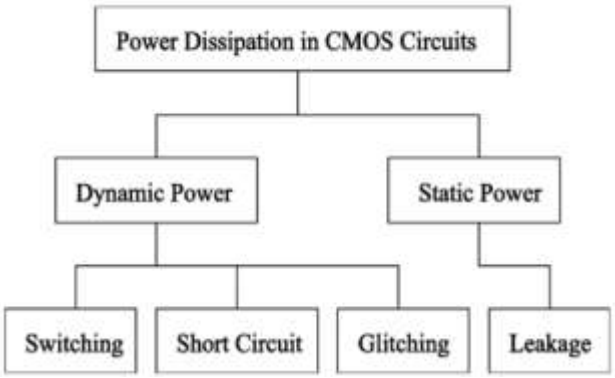


Fig1.Types of Power dissipation

1. **Dynamic power dissipation**:

The power utilised by a circuit when it is actively moving from one state to another is known as dynamic power. Internal power (also known as short circuit power) is consumed internally to the device while it is changing state, and switching power is wasted while charging and discharging the loads on a device. Logic transitions cause logic gates to charge and discharge load capacitance, resulting in dynamic power dissipation. To put it another way, this form of power dissipation is caused by transistor switching.

**a. Switching Power Dissipation**

The power dissipation during a switching event is represented by Switching Power Dissipation. This signifies that a CMOS logic gate's output node voltage undergoes a power-consuming transition. When energy is extracted from the power source to charge up the output node capacitance in digital CMOS circuits, dynamic power is dissipated. The output node voltage normally performs a full transition from 0 to VDD during the charge-up phase, and the energy consumed for the transition is relatively independent of the circuit's function.

**b. Short circuit Power dissipation**

The energy required to charge up the parasitic capacitances in the circuit causes the switching power to dissipate, and the switching power is independent of the rise and fall timings of the input signals. When a CMOS inverter (or a logic gate) is operated with input voltage waveforms with limited rise and fall times, both the NMOS and PMOS transistors in the circuit may conduct for a brief period of time during switching, establishing a direct current path between the power supply and the ground.

**c. Glitch Power Dissipation**

The glitching power dissipation occurs due to the finite latency. This power was used in the intermediate transitions during the logic function assessment of the circuit. The limited propagation time from one logic block to the next can cause erroneous signal transitions or glitches in multi-level logic circuits as a result of crucial races or dynamic hazards. In general, no glitching happens when all of a gate's input signals change at the same time. However, if input signals alter at various times, a dynamic hazard or glitch can emerge. As a result, a node can go through several transitions in a single clock cycle before settling down to the correct logic level. Even if signal glitches are only partial, in the sense that the node voltage does not make a complete transition between the ground and VDD levels, they can contribute significantly to dynamic power dissipation.

2. **Static Power Dissipation**

When the system is not powered or in standby mode, power dissipation takes the form of leakage current. Subthreshold leakage, diode leakages around transistors and n-wells, tunnel currents, gate leakage, and other sources of leakage current exist in circuits.

**Leakage Power Dissipation**

Nonzero reverse leakage and sub threshold currents are common in the NMOS and PMOS transistors utilized in CMOS logic gates. Even when the transistors are not switching, these currents can contribute to the overall

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power dissipation in a CMOS VLSI chip with a large number of transistors. The processing settings mostly impact the size of leakage currents.

## III. Existing System

### *A. True single Phase Clock Technique*

The Flip-Flop is made using the True Single Phase Clock technique. The major goal of employing TSPCL is to do the required Flip-Flop operation with the least amount of power and the fastest speed possible.

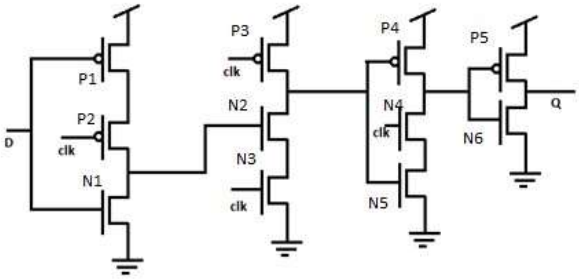


Fig 2. D flipflop Design using TSPCL

When D is 0 and CLK is low, the transistors P1 and P2 are active, which activates the next stage's transistor N2. This stage's P3 is active, and it returns 1 (which is inverted and returns 0). Similarly, D's supplied input is inverted at each level, and the output is the same as the input.

### *B.*

### *C. Selfcontrollable voltage level Technique:*

The SVL approach is used to reduce the circuit's leakage power. Upper SVL, Lower SVL, and a mix of both upper and lower SVL circuits are the three types of self-controllable voltage level circuits.

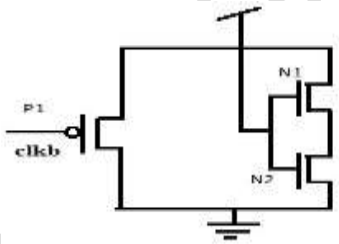


Fig 3. Upper SVL

The two NMOS are connected in series with a parallel PMOS in the upper SVL. PMOS receives the gate of the two NMOS connected to the supply as well as the input clock bar. When the clk is 1, the clkb is 0 and PMOS is enabled. As a result, the PMOS begins to conduct, allowing the supply voltage 1 to pass through. When the clk is 0 and the clkb is 1, the two NMOS begin to conduct and connect to the ground.

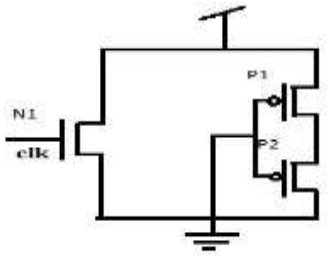


*Fig 4. Lower SVL*

Two PMOS are connected in series with a parallel NMOS in the lower SVL. The input clock is connected to the gate of the two PMOS, while the gate of the NMOS is connected to the ground. When the clk reaches 1 and the NMOS is turned off. As a result, the PMOS begin to conduct and are connected to the earth. When the clk is set to 0, the two NMOS begin to conduct, allowing supply voltage 1 to pass through.When the circuit is turned off, the supply voltage should be decreased to reduce power dissipation and extend battery life. The CMOS D Flip-Flop circuit is modified with the SVL approach, which suppresses signals and minimizes power dissipation due to leakage currents.

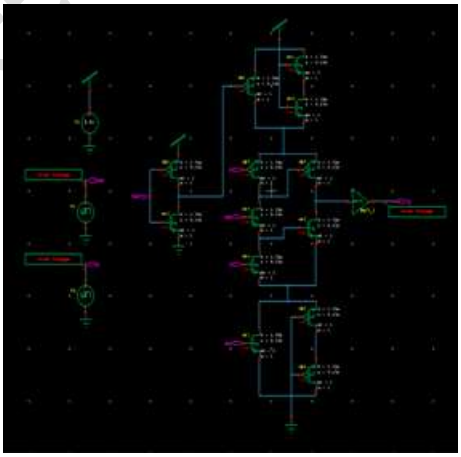

Fig 5. Design of D flipflop with TSPCL and SVL

The D flipflop with combination of both TSPCL and SVL techniques as shown in above figure. From the above figure P1 is active, N2 is active, P2, P3 is inactive, and N1 and N2 are inactive. It is linked to supply and GND in order to perform the standard D Flip-Flop operation. P1, N1, N3 are active when an is inactive, but P2, N2 are inactive, therefore out is inactive. Out becomes one when an is 1, which makes P1, N3 inactive while making N1, N2 and P2 active.P1 and N3 are both turned off, i.e. open circuits. N1, N2 are active, but because they serve as a pull-up network, the supply voltage is Vdd-Vth. The static power is reduced when the

NMOS transistors are coupled in series. P2, P3 are active, however because they serve as a pull down network, they provide a finite positive voltage as a replacement for GND.Because the NMOS transistors are connected in series, the supply voltage is lower and the leakage current is lower during standby mode. Leakage power is related to current and supply voltage, hence lowering it is a major problem. This design also has the benefit of boosting the circuit's operational speed.This TSPCL paired with SVL technology consumes less power than the traditional Flip-Flop.

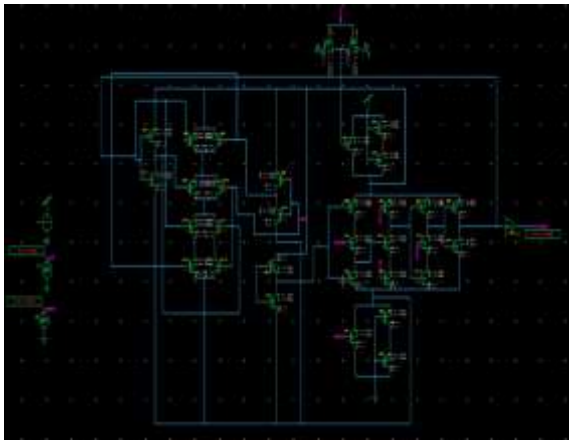

Fig 6. Design of T flipflop using D flipflop

The above figure shows the T flipflop. The T flipflop is formed by placing an XOR gate before the D flipflop. P1 is active, N2 is active, P2, P3 is inactive, and N1 and N2 are inactive. It is linked to supply and GND in order to perform the standard D Flip-Flop operation. P1, N1, N3 are active when an is inactive, but P2, N2 are inactive, therefore out is inactive. Out becomes one when an is 1, which makes P1, N3 inactive while making N1, N2 and P2 active.P1 and N3 are both turned off, i.e. open circuits. N1, N2 are active, but because they serve as a pull-up network, the supply voltage is Vdd-Vth. The static power is reduced when the NMOS transistors are coupled in series. P2, P3 are active, however because they serve as a pull down network, they provide a finite positive voltage as a replacement for GND.Because the NMOS transistors are connected in series, the supply voltage is reduced as well as the leakage current during standby mode.

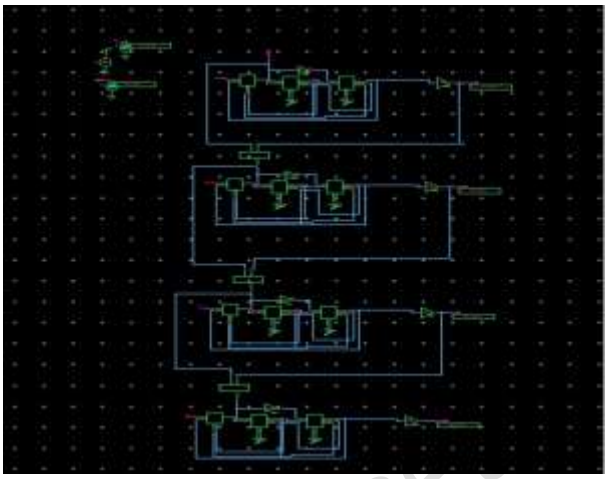

Fig 7. Existing counter Design using TSPCL and SVL

The figure shows 4-bit counter using TSPCL with SVL technique. This system employs a cascade T Flip-Flop structure. The counter is 4-bit so we used four cascaded flipflops. The T Flip-Flop is used because it is concerned with the shifting activity of the following state. When the input of T Flip-Flop is 0, it eliminates the clock transition. When the clock is zero, it has no effect on the circuit's output and so preserves the previous state output, however when the clock is one, the output is toggled.

The Flipflop receives the clock signal from the clock network. The clock is applied at first flipflop it drives the first flipflop and the output of first flipflop is given as clock input for next flipflop. Now the output of flipflop acts as Clock and drives the next flipflop. Similarly next flipflop also activated and produces output.

## IV. Proposed System

MGDI is a brand-new method for creating low-power digital circuits. This method is based on the GDI technology. MGDI is a technique for reducing power dissipation, transistor count, and area in digital circuits. It has three input terminals: G (both PMOS and NMOS input), P (input to PMOS drain/source), and N (input to NMOS drain/source) except for the bulks of PMOS (Sp ) and NMOS (Sn), which are always linked to VDD and GND, respectively.

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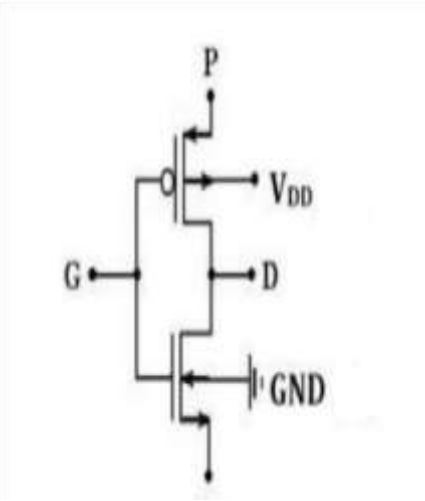


Fig 8. Basic MGDI cell

The disadvantages of the GDI cell are resolved by MGDI. The influence of source body voltage on transistor threshold voltage becomes truncated as technology scales, i.e. the linearized body coefficient ‘' in the equation below. Make MGDI relevant in 65 nm and lower technology.

From the table-1 it has been discovered that a single MGDI cell can be used to create many logic styles. The OR and AND gates are designed with only two transistors, whereas typical CMOS requires six transistors. The fundamental benefit of MGDI is that it reduces transistor counts and chip area, resulting in lower power consumption. As a result, using the MGDI methodology, it is simple to create complex circuits.

| G | P | N | $S_P$ | $S_N$ | OUTPUT | FUNCTION |
|---|---|---|---|---|---|---|
| A | $V_{DD}$ | 0 | $V_{DD}$ | 0 | A' | INVERTER |
| B | 0 | A | $V_{DD}$ | 0 | A.B | AND |
| A | B | $V_{DD}$ | $V_{DD}$ | 0 | A+B | OR |
| B | A | A' | $V_{DD}$ | 0 | A'B+AB' | EX-OR |
| B | A' | A | $V_{DD}$ | 0 | AB+A'B' | EX-NOR |
| S | A | B | $V_{DD}$ | 0 | AS'+BS | 2:1 MUX |

Table-IMiscellaneous functions using MGDI cell

The MGDI cell functions as a 2:1 Mux cell. A multiplexer is a circuit with several data inputs and a single output that is controlled or selected by control or select inputs. The 2:1 mux has two inputs (A and B), as well as one selection line and one output. The selection line input is sorted to both PMOS and NMOS gates and has input A, B, with A being given at the PMOs source and B being given at the NMOS source. We're making a flipflop out of the Mux.

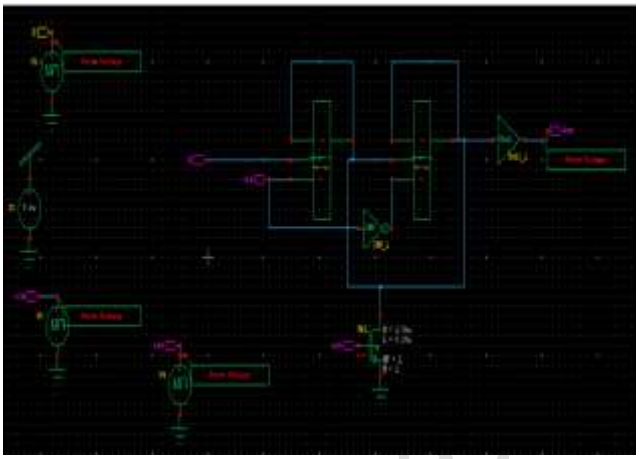

Fig 9. D flipflop using MGDI technique

The D flipflop is built using two multiplexers in this example. The clock is applied to the first block, and D is provided to one of Mux's input terminals. The output of the mux is used as the input for the following Mux, which uses an inverted clock.

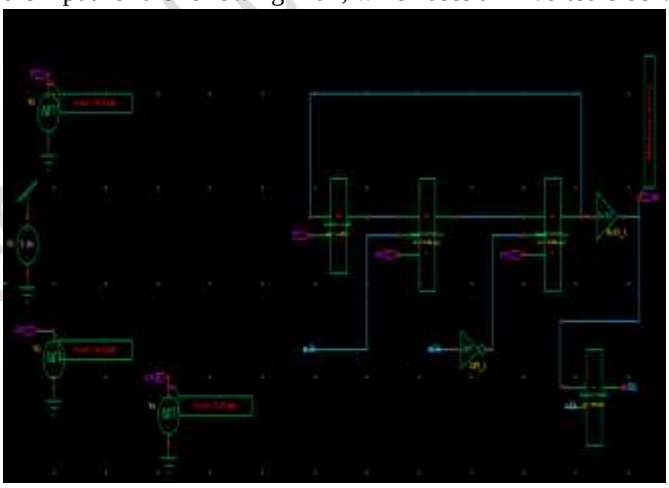

Fig 10. T flipflop Design using MGDI technique

The T flip flop is shown with two D flip flops in the diagram above. The T flipflop is made by attaching an XOR gate to the D flipflopinput. At the initial flipflop, the clock is given. When CLK is 1, the first flipflop is engaged, and the output is D, while the inverted clock is used for the second flipflop. T input is given at input of XOR gate and the feedback is given as another input. The output of XOR isgiven to D flipflop.

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Fig 11. Proposed counter design using Modified GDI Technique

The Proposed counter using 4 T flipflops is shown in figure. Here the T flipflops are connected in cascaded. The CLK signal is applied for first flipflop and the output of first flipflop and CLK signal is given as inputs for AND gate the output of AND gate is acts as CLK for next flipflops.

## V. SIMULATION RESULTS

All the results are simulated using 250nm CMOS technology library in Tanner EDA tool.

a. Simulation results of Existing Method
The simulation results of Existing counter using TSPCl with SVL technique is shown in figure.

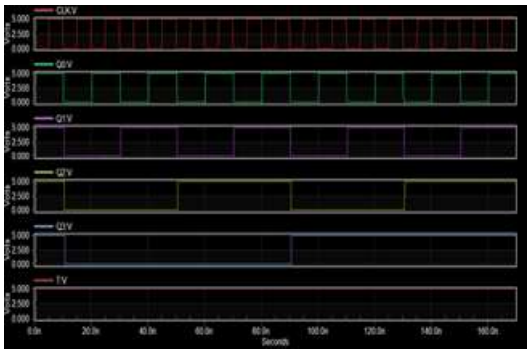
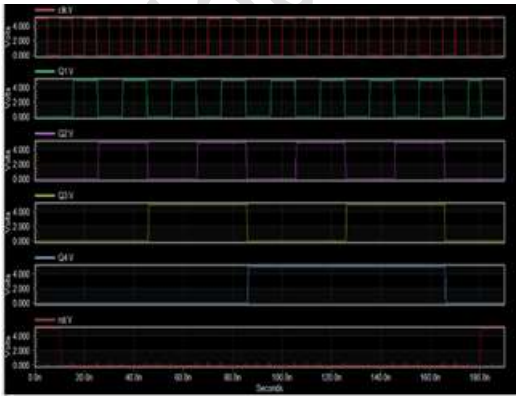


Fig 12.Wave forms of existing counter

The clock input is given as CLK. The Toggle input is denoted by T, and the output is denoted by Q. Because the output changes every clock, the T input is always high.The Q0 indicates the first bit, Q1 indicates the second bit, Q2 indicates the third bit, and Q3 indicates the fourth bit.

b. Simulation results of Proposed method
The simulation results of counter using Modified Gate Diffusion Input is shown below.



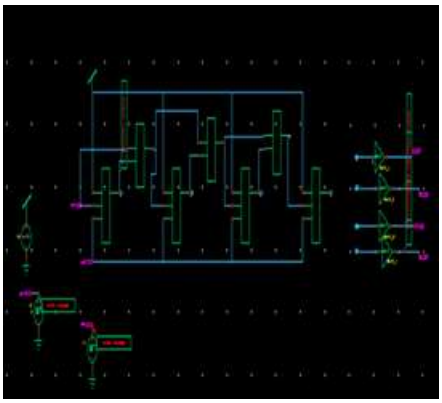


Fig 13. Waveforms of Proposed counter

It's a four-bit up-counter that counts from zero to sixteen on the Negative edge of the clock signal. Q1 indicates the first bit, Q2 indicates the second bit, Q3indicates the third bit, and Q4 indicates the fourth bit.When CLK's negative edge arrives, the output is toggled. The output is initially zero. For Q1 output, the input is 0 during the first negative edge of the clock, and the output is 0 until the next negative edge. The result is toggled from 0 to 1 at the second falling edge. The output toggles from 1 to 0 at the clock's third negative edge, while the output is maintained for the clock's positive edge. Similarly, the output is toggled on every negative edge.The Q1 signal serves as a clock for the output of the second flipflop Q2.

The output is toggled whenever Q1's negative edge occurs. Continue the process for the next two flipflops, counting from zero to fifteen (0-15).

**c. Power comparison results of existing and proposed methods**

The below table compares the power dissipation results of existing and proposed counter for the supply voltage 5.0V.

| | No. of Transistors | Power Consumption | No. of Transistors for each flipflop | Delay |
|---|---|---|---|---|
| Existing Method (TSPCL with SVL) | 234 | 16.67uw | 38 | 266nsec |
| Proposed Method (Modified GDI) | 162 | 13.27uw | 22 | 118nsec |

Table-II Power consumption results of Existing and Proposed counter designs

From the table-II it is shown that the dissipation of power in proposed counter design id reduces by 21% comparing to the Existing counter design.

## Conclusion

The proposed Modified Gate Diffusion Input methodology reduces the power usage in the counter. When compared to the current counter design, the proposed counter uses 21% less energy. The Tanner Tool, which uses 250nm CMOS technology, is used to create and simulate the projected counter. The proposed counter uses less power and chip area, extending the battery life and improving system performance. According to the analysis, it can be stated that using the modified gate diffusion input technique while constructing low-power devices is beneficial. MGDI has been seen to reduce the transistor count by a significant amount in the majority of cases. Another characteristic that is dependent on the number of transistors is delay, which is lowered in comparison to the present method.

# VI. References

[1] Gavaskar, K., Malathi, D., Dhivya, R., Dayana, R. D., &Dharun, I. (2020). Low Power Design of 4-bit Simultaneous Counter using Digital Switching Circuits for Low Range Counting Applications. 2020 5th International Conference on Devices, Circuits and Systems (ICDCS)

[2] Padmanabhan Balasubramanian and Johince John, "Low Power Digital design using modified GDI method",International Conference on Design and Test of Integrated Systems in Nanoscale Technology, IEEE, pp.190-193, September 2006.

[3] C. Christakis, G. Theodoridis and A. Kakarountas, "High speed binary counter based on 1d cellular automata," 5th International conference on modern circuits and systems technologies (MOCAST), Thessaloniki, pp. 1–4, 2016.

[4] Katreepalli, R., &Haniotakis, T. (2018). Power efficient synchronous counter design. Computers & Electrical Engineering.

[5] Rabaey.JM, Chanrakasan A, Nikolic B, Digital integrated circuits; A design perspective, Prentice Hall;2003.

[6] Wu X, Wei J, pedram M, low power design of sequential circuits using quasi-synchronous derived clock.in: Proceedings 2000. Design automation conference. (IEEE Cat, No.00CH37106), Yokohama, Jpan: 2000, P. 345-50

[7] Weste NHE, Harries D, Banerjee A, CMOS VLSI design, 3rd edition, Dorling Kindersley PVT, Ltd,;2006

[8] Hwang YT, Lin Jf, Low Voltage and Low power divide-by=1/3 counter design using pass transistor logic circuit technique, IEEE Trans VERy Large Scale integr VLSI Syst 2012,20(9),1738-42

[9] Madhu Shakya and Shweta Agrawal, "Design of Low Power C-MOS D flip-flop using modified SVL technique," International Journal of Research and Analytical Reviews, Vo. 5, No. 4, pp. 2349-5138, 2018.

[10] E. Ogunt, M. Frank and S. Foo, "Design of a low power binary counter using bi-stable storage element," International conference on electronic design, Penang, pp.1–5, 2008.

[11] Thakur A, Mehra R, Power and speed efficient ripple counter design using 45 nm technology, In;2016 IEEE 1st International Conference on Power electronics, intelligent control and energy systems (ICPEICES, Delhi; 2016.p, 1-4.

[12] Ogunti E, Frank M, Foo S, Design of a low power binary counter using bistable storage element, In: 2008 International conference on Electronic design, Penang; 2008, P. 1-5.

[13] Christakis C, Theodoridis G, Kakarountas A HighSpeed binary counter based on 1d cellular automata. In: 2016 5th International conference on modern circuits and systems technologies (MOCAST), Thessaloniki;2016. P, 1-4.

[14] Hu Jp, Xu Tf, Xia YS. Low power adiabatic sequential circuits with complementary pass-ransistor logic. In; IEEE MWSCASOS5 USA; 2005, P, 1398-401.

[15] Gautham M, Nirmal U, Jain r. Low Power sequential circuits using improved clocked adiabatic lodic in 180nm CMOs Processes, In: 2016 International conference on research advances in integrated navigation systems (RAINS), Bangalore; 2016. P. 1-4.

[16] ASIC primitive cells in Modified Gate Diffusion Input Technoque; R. Uma and Dhavachelvan; pp. 467-474, springer India,2013.