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An Efficient Multi-Layered Full Adder Subtractor In Quantum Dot Cellular Automata

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ABSTRACT

Quantum Dot Cellular Automata (QCA) is one of the efflorescing Nano Technologies and it can be considered as one of the best replacements for the Semiconductor technology which mostly uses the Transistors for the design of circuits. At nanoscale level the transistors don't behave as they really were where QCA does. The major elemental components for designing any circuit in QCA are XOR gate, inverse gate and majority gate and the study consummated in these areas was shortened. The QCA Computational regimens can be abridged with an efficient and effective full adder and subtractor circuits. In this study a new 3 input XOR gate was proposed and with this a novel multi layered full adder-subtractor circuit was designed with a smaller number of quantum dot cells. The Operation of the QCA Circuit is simulated and verified using the Coherence vector simulation. The proposed Design occupies only 0.08 μm² area with 68 Quantum Cells

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KEYWORDS: *Full Adder Subtractor, Quantum Dot Cellular Automata, Multi-Layered Quantum Cells*

I. INTRODUCTION

According to the Moore's law that the number of transistors on the circuit doubles for every 18 months and it implies that the size of the transistors deteriorates, As the size of the transistors diminishes more and more and reach the nanoscale level then they will not work precisely. The predicaments are the more heat dissipation, more energy dissipation, decrease in the efficiency of the circuits, decrease in the performance of the circuits, expensive fabrication and soon...

In order to overcome all these snags QCA is the best alternative for the current CMOS Technology as it was a solid-state nano-electronic technology. The design of the circuits made by using the Quantum Cells. Each Quantum Cell contains of the four quantum dots in which it contains of two electrons and the position of the electrons in these quantum dots adjudicate the polarization. The movement of the electrons in the Quantum dots was only in the vertical direction. The data processing was based on the columbic transcriptions of the similar cells.

In the past years many QCA designs are proposed such as adders, subtractors, multiplexers but, very few designs are proposed based on the full adder-subtractor. In this paper a new full adder-subtractor design was proposed and it contains one XOR gate and two majority gates. At last, QCA Designer-E master was used to analysing the accuracy of the circuit and also the energy dissipation of the circuit.

STRUCTURE OF PAPER

The paper is organized as follows: In Section 1, the introduction of the paper is provided along with the structure, important terms, objectives and overall description. In Section 2 we discussed literature survey. In Section 3 we discussed Basic of QCA. In Section 4 Existing designs is discussed. In Section 5 detailed information of proposed designs is discussed. Section 6 gives the results and comparison. Section 7 gives the conclusion of the entire design.

OBJECTIVES

The main objective of the design of Full adder subtractor was to decrease the size of the full adder subtractor and to decrease the cells used in the design. To increase the efficiency of the output

II. LITERATURE SURVEY

XOR gate is one of the appealing uses of QCA innovation. The proposed plan and recreation of the XOR gate dependent on QCA with least territory and intricacy. This paper introduces the structure and recreation of XOR gate in QCA using the QCA Designer Tool. Most of the circuit designs

utilizes these XOR gates and they play an important role in circuit designing. Many XOR gates (In Ref [3],[4],[5],[6],[7],[8],[9]) have been proposed till now but most of the designs have a greater number of cells and consume more area hence in our paper we proposed an efficient XOR gate with very few numbers of quantum cells and less area occupancy.

By using he proposed XOR gate we constructed the full adder (In Ref [10],[11],[12],[13],[14],[15],[16],[17],[18]), full subtractor (In Ref [3],[24],[30],[31]), full adder-subtractor (In Ref [22],[23],[28],[29],[30]) circuits with a smaller number of areas. Previously, very few numbers of designs are proposed based on the full adder-subtractor and all of these designs occupy a greater number of cells and area. In order to reduce the area in our paper we used the multi-layering concept for constructing the full adder-subtractor with very a smaller number of cells than the previous designs proposed and the area occupancy was also very less and the major advantage of our proposed design was the energy dissipation was very less.

Full adder-subtractor designs are used in most of the arithmetic logic circuits for calculations and the future applications of our proposed design was we can construct the Ripple carry adder using the full adder circuit and Ripple borrow subtractor using the full subtractor circuit. In our proposed design the carry output was collected at the main cell layer and the borrow output was collected at the upper layer hence we can construct the Ripple carry adder at the main cell layer and Ripple borrow subtractor was constructed at the upper layer to collect both the different outputs at the different layers. Hence our proposed design was an efficient and effective approach

.

III. BASIC OF QCA

A) QCA Cell

QCA cell is the basic element for designing any circuit using QCA. The QCA cell consists of four quantum dots they contain only two electrons settled in the diagonal positions of the quantum cell. There was a tunnelling junction in vertical direction between the quantum dots and hence there was movement of electrons but, in the horizontal direction capacitive junction exists hence no movement of electrons in the horizontal direction.

Due to the columbic forces between the electrons they always tend to settle in maximum distance possible and hence the electrons in the Quantum Cell always positioned at the corners in a diagonal position and this applies when two or more quantum cells are connected together. There are different representations of Quantum Dot Cells such as Normal dot cell, Vertical dot cell, Crossover dot cell and four coloured dot cells having colours with respective to their clocks.

B) QCA Wire:

QCA wire is group of the quantum dot cells used for transferring the data from one end to another end. There are two different QCA wire they are normal QCA wire (or) 90^0 wire and another type was 45^0 wire and it is the rotated version of normal QCA wire.

The basic elements in the QCA are the majority gate and the Inverters and these two circuits are used mostly in the designing of the circuits in QCA. The output of inverter was the inverse of the input and the output of the majority gate was the majority of the input values and the output of three input majority gate was given as

Output=MV (A, B, C) =A.B+ A.C+ B.C

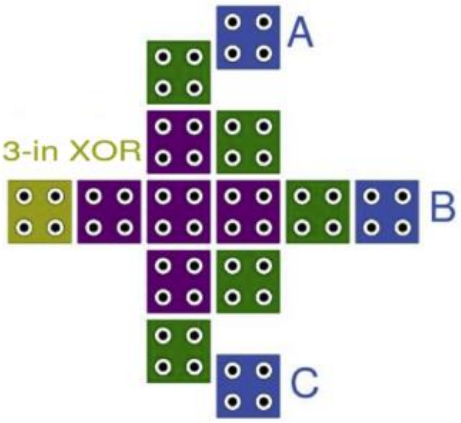
C) Clocking in QCA:

There are four types of clocking's in the QCA as clock 0, clock 1, clock 2, clock 3 and these are applied to the Quantum cells and each clock cycle has their respective own colour representation. Switch, Hold, Release and Relax are the four clock phases of a quantum cell and these have 90^0 Phase shifts from the preceding one. When the clock signal is in a high state, electron tunnel junctions open, allowing electrons to travel between potential wells. The transition from high to low is a switch stage, and as tunnelling energy decreases, the potential barrier rises. The QCA cell achieves a fixed polarised state of electrons at low states. The release stage of the clock signal occurs as tunnelling energy increases, and the potential barrier drops. Finally, the QCA cell is relaxed to an unpolarized state at high state

D) Wire Crossing Techniques:

Wire crossing is the most useful technique in designing the circuits and it was considered as very important technique. Coplanar wire crossing, Multilayer wire crossing and Logical wire crossing are the three different wire crossing techniques, among those Coplanar wire crossing and the Multilayer wire crossing are the Mostly used wire crossing techniques. In coplanar technique, two different QCA wires (90^0 and 45^0 wire) are used for wire crossing. Coming to the multilayer technique three layers Bottom layer, Middle layer and the Upper layer are used for wire crossing technique and both the techniques are shown below

IV



EXISTING DESIGNS

XOR:

A number of XOR gates have been proposed till now and by using those XOR gates full adder, half adder, full subtractor, half subtractor, full adder-subtractor and many more circuits can be constructed. The Existing designs of the XOR gate are shown below

4.1) XOR in Ref [5]
4.2) XOR in Ref [3]
4.3) XOR in Ref [6]

The existing XOR designs in [5],[3],[6] are having of 12, 22, 94 and with a total area occupancy of 0.012,0.017,0.073, respectively and most of the designs existed are single layer designs and in [26] cell transition technique was utilized.

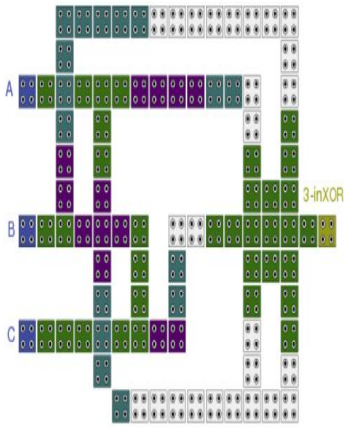


Fig 1

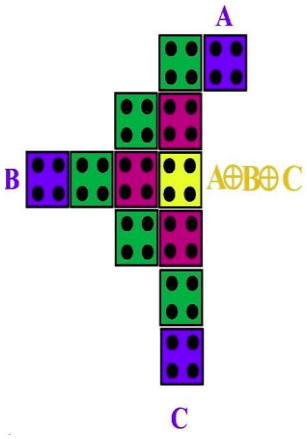


Fig 2

Fig 3

FULL ADDER SUBTRACTORS:

Very few numbers of full adder-subtractor designs are existed till now ([22],[23],[28],[29],[30] ...) and all of these designs requires a greater number of the quantum cells and uses different wire crossing techniques and the area occupied by these full adder-subtractor designs are also more compared to the proposed design.

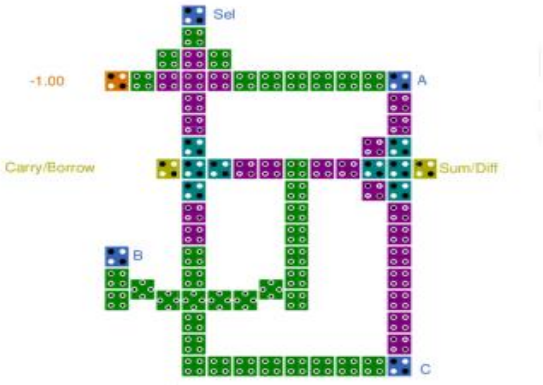


Fig 4

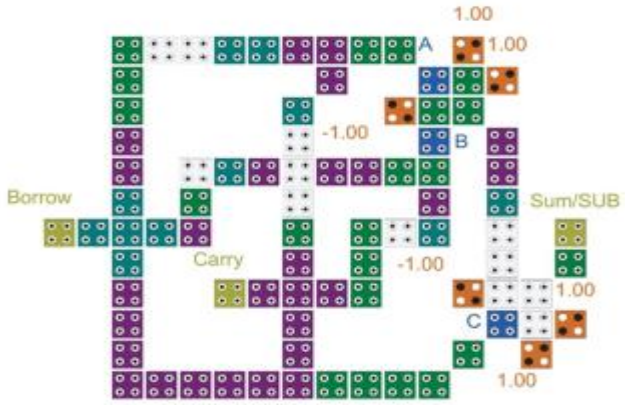


Fig 5

V. PROPOSED DESIGN

Proposed XOR:

In this paper we proposed new XOR gate with 11 cells and with 0.02 µm2 and the proposed XOR gate was a single layer structure.

Total energy dissipation (Sum_Ebath): 2.09e-002 eV (Error: +/- -2.26e-003 eV)

Average energy dissipation per cycle (Avg_Ebath): 1.90e-003 eV (Error: +/- -2.05e-004 eV)

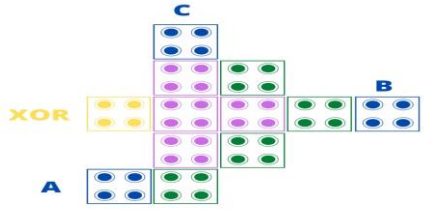


Fig 6 Proposed XOR

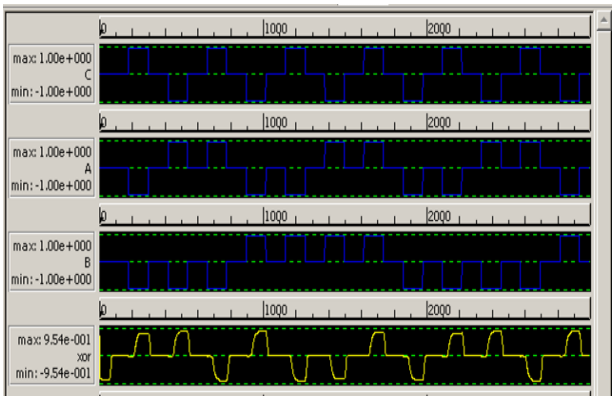


Figure 7: simulation result of proposed XOR

Proposed Full Adder:

Proposed full adder was having of 28 cells with an area of 0.04 µm2 with a single layer structure. Total energy dissipation (Sum_Ebath): 5.54e-002 eV (Error: +/- -5.99e-003 eV)

Average energy dissipation per cycle (Avg_Ebath): 5.04e-003 eV (Error: +/- -5.44e-004 eV)

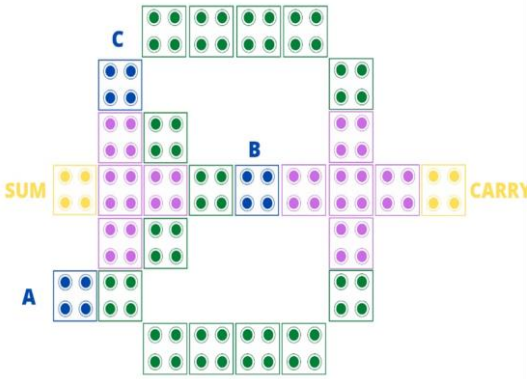


Fig 8 Proposed Full Adder

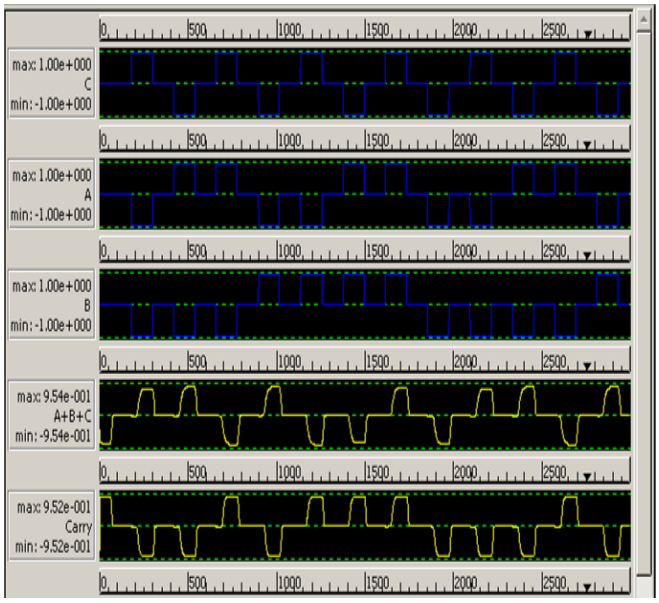


Fig 9 Simulation Result of Full Adder

Proposed FULL Subtractor:

Proposed full subtractor was having 29 cells with an area of 0.04 µm2 with a single layer structure. Total energy dissipation (Sum_Ebath): 6.25e-002 eV (Error: +/- -6.77e-003 eV).

Average energy dissipation per cycle (Avg_Ebath): 5.69e-003 eV (Error: +/- -6.15e-004 eV).

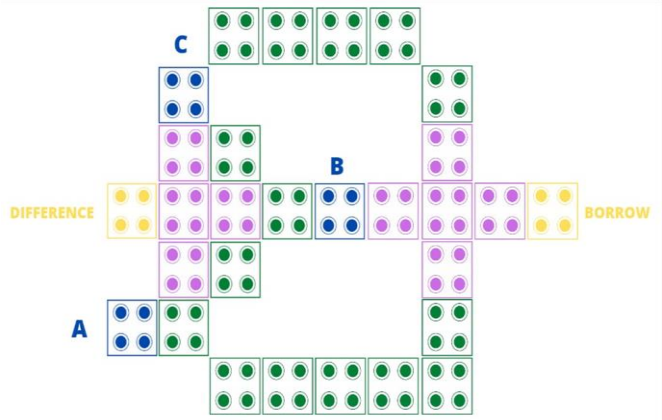


Fig 9 simulation result of proposed Full Subtractor

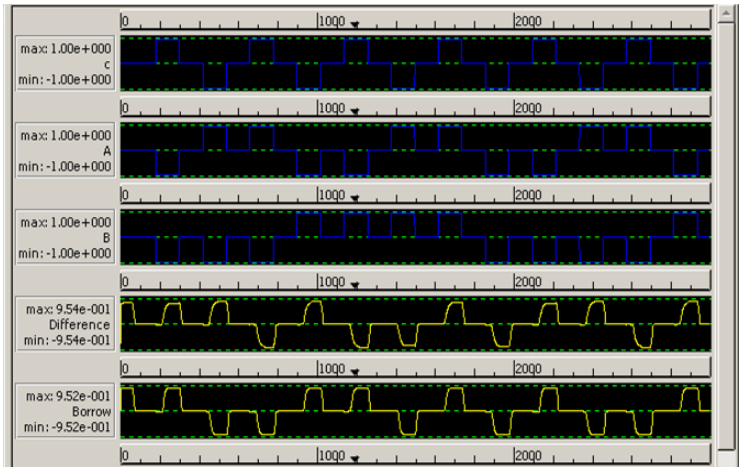


Fig 10 Simulation Result of Full Subtractor

Proposed Full Adder Subtractor:

Proposed full adder-subtractor was with 68 cells and with an area of 0.08 μm2 and it was a multi-layered structure. There are three layers in the proposed full adder-subtractor structure. Multi layered structures are very helpful in future and the main advantage of the multi-layer structured designs are these designs occupies less area than the single layer structures. Total energy dissipation (Sum_Ebath): 1.74e-001 eV (Error: +/- -1.89e-002 eV).

Average energy dissipation per cycle (Avg_Ebath): 1.58e-002 eV (Error: +/- -1.72e-003 eV)

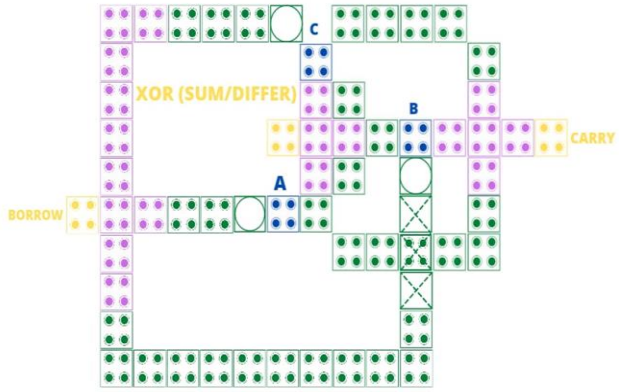


Fig 11 Multi-Layered Full Adder Subtractor

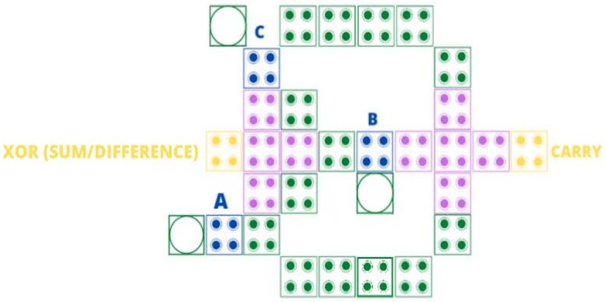


Fig 12 Structure in Lower layer

Fig 13 Structure in Middle layer

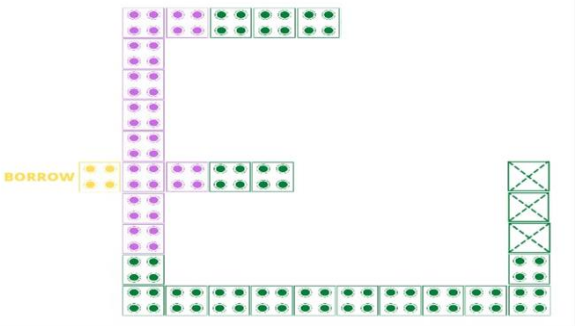


Fig 14 Structure in Upper layer

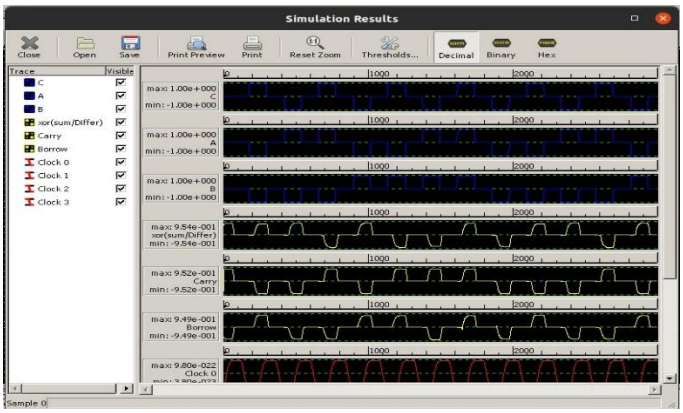


Fig 15 Simulation Result of Full Adder subtractor

VI. RESULTS AND COMPARISION OF DESIGNS

In this section we compare all the previous existing designs and the new proposed design in the form of tables for XOR, full adder, Full subtractor, Full adder Subtractor.

Three input XOR gate	Area (µm 2)	Cell count	Wire crossing Type
Ref [3]	0.012	12	Not Required
Ref [4]	0.017	22	Not Required
Ref [5]	0.073	94	Coplanar
Ref [6]	0.022	14	Not Required
Ref [7]	0.02	28	Not Required
Ref [8]	0.0233	30	Not Required
Ref [9]	0.02	32	Not Required
Proposed XOR	0.02	11	Not Required

TABLE 1

Full Adder	Area (µm 2)	Cell count	Wire crossing Type
Ref [10]	0.2	192	Coplanar
Ref [11]	0.0801	73	Multi-layer
Ref [12]	0.044	73	Multi-layer
Ref [15]	0.07	69	Coplanar
Ref [13]	0.0434	59	Coplanar
Ref [14]	0.034	51	Multi-layer
Ref [17]	0.02	38	Multi-layer
Ref [16]	0.02	33	Multi-layer
Ref [18]	0.02	31	Multi-layer
Proposed Design	0.04	28	Not Required

TABLE 2

Full Subtractor	Area (µm 2)	Cell count	Wire crossing Type
Ref [24]	0.168	136	Multi-Layer
Ref [30]	0.205	178	Multi-Layer
Ref [3]	0.0287	32	Not Required
Ref [31]	0.10	83	Not Required
Proposed Design	0.04	29	Not Required

TABLE 3

Full Adder-Subtractor	Area (µm 2)	Cell count	Wire crossing Type
Ref [30]	0.132	186	Multi-Layer
Ref [29]	0.6	90	Multi-Layer
Ref [28]	0.79	109	NA
Ref [23]	0.09	75	Coplanar
Ref [22]	0.09	83	Coplanar
Proposed Design	0.08	68	Multi-Layer

TABLE 4

Proposed Designs	Cell Count	Area (µm 2)	Wire Crossing Type	Total Energy Dissipation (Sum_Ebath)	Average Energy Dissipation (Avg_Ebath)
XOR gate	11	0.02	Not Required	2.09e-002 eV	1.90e-003 eV
Full Adder	28	0.04	Not Required	5.54e-002 eV	5.04e-003 eV
Full Subtractor	29	0.04	Not Required	6.25e-002 eV	5.69e-003 eV
Full Adder - Subtractor	68	0.08	Multi-Layer	1.74e-001 eV	1.58e-002 eV

TABLE 5

VII. CONCLUSION

As the full adder-subtractor was the very essential component in the Arithmetic computations, in our paper we designed an efficient full adder-subtractor circuit with a very a smaller number of cells and in our design we used the multi-layer approach which is the best way to reduce the total occupancy area of the circuit. Initially proposed an XOR gate design with a smaller number of quantum cells and with this XOR gate we constructed the full adder, full subtractor and full adder-subtractor circuits. The outputs of all the proposed designs are analyzed and verified through the QCA-E master in coherence vector(w/Energy) simulation engine setup with 500000 samples and 3000 samples are recorded for graphing. Our proposed design took only 7 iterations to converge the initial steady state polarization. Finally, we compared the different existed designs with our proposed designs.

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