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IMPACT OF VIA ON SIGNAL INTEGRITY

M. Manjusri[1] | M. Jyothi[2] | M. Narendra Kumar[3]| M. Leela Siva Sai[4]

[1,2,3,4]UG student, Electronics and Communication Engineering, Godavari Institute of Engineering and Technology(Autonomous), Rajahmundry, A.P, India.

ABSTRACT

While designing PCB different types of discontinuities came into picture where designing of Via which is normally used as an interconnect between two different layers is the major drawbacks for providing signal integrity. The study allows high-speed digital designers to possess a more in-depth valuation of via design and its effect on SI performance. In this project we have Designed a four layer Through Hole Via and various parameters like S,Y VSWR have simulated using HFSS. The Designed Via having Higher cut-off Frequency of 6.7 Ghz and Lower cut-off Frequency of 5 Ghz and Produces a wide Band width of 29.05%. The aspect Ratio of Designed Via is less than '8' which indicates it can be used in industrial Sector.

KEYWORDS: Signal Integrity, Via, PCB, HFSS version 15.0(HIGH FREQUENCY STRUCTURE SIMULATOR), FR_4Epoxy, parameters-S,Y,Z

INTRODUCTION

Providing signal integrity or signal quality at high frequency is an important aspect in recent trends in advanced packaging system where one bad bit dramatically affects whole configuration. Signal Integrity refers to a brand set of integrated circuit design issues such as electro-migration, IR drop and antenna effects. A signal that consists of multiple frequency components. A good digital signal typically requires constant amplitude change and constant time shift/delay for all frequency components. If they are not constant, signal distortions may occur. So, the signal integrity is ability of a system to transfer the signal without any excessive distortion. Signal integrity can also reconstruct the signal at the receiver accurately.

Signal integrity becomes more important at higher speeds (as rise time decreases) for high-speed application. So, the signal integrity concern about high-speed digital design. It primarily involves the electrical performance of the wires and other packing structures used to move signal within an electronic product. To ensure signal integrity the design engineer must guarantee that under the condition of system must provide high voltage. In this the high voltage vih and low voltage vil is known as Threshold Voltage between these the receiver is distinguished.

The issues must be resolved during the design the flow. A single data model combined with an integrated design system is necessary to address deep submicron to provide time manner. As, we know the signal integrity existed long before the advent of either technology, and will do as long as electronic communication persist. These effects are typically happening when the system speed exceed a few tons of MHz for the designation of circuit are above >100MHz in the mind of signal integrity. They are many critical aspects while providing signal integrity for high-speed digital design such as signal propagation on transmission lines (loss, termination etc) via, connector and package modeling, non-ideal return paths, power integrity. Here we have designed a via using HFSS and try to figure out its reflection and transmission coefficient, VSWR, parameters etc.,

We proved that the signal integrity can improved by the proper selection of material and we tabulated the values.

II. IMPACT OF VIA ON SIGNAL INTEGRITY

Via is a path way which transmit the signal from source to the receiver. Impact on via on signal integrity which we have shown low capacitance and the inductance effects on via design. We have designed and simulated a four layer single via using HFSS and explained its result output. It'll be shown with careful design of the via environment, this return path can also be controlled, which makes it possible to sort out vias in terms of cable parameters within the certain frequency ranges. This means the via stubs effect and alternatives to mitigate it by shifting unwanted resources beyond the range of interest are addressed. This says that the via impedance can be controlled to match a specific target in order to minimize reflections.

Finally, both via impedance matching and stub length reduction methods were applied to a generic link configuration so on access the impact on signal stability. The most common type of via is called "through hole via" because it is made up of drilling through the board. We can represent via also as a vertical transmission line. It consists of pad, antipad, and barrel.

Barrel: It is a conductive material that fills the hole to allow an electrical connection between layers.

Pad: It is used to connect the barrel to the component or trace.

Antipad: It is clearance hole between the pad and the metal on a layer to which no connection is required.

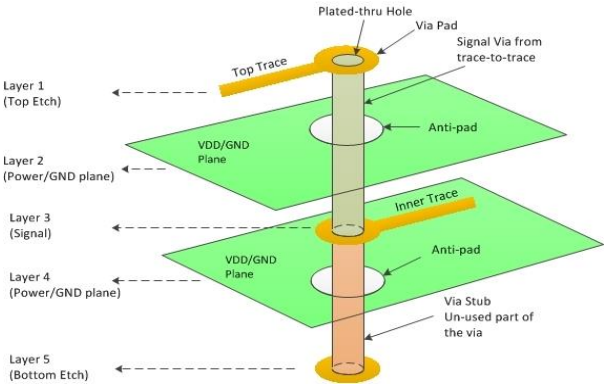


Fig.1 Through hole Via

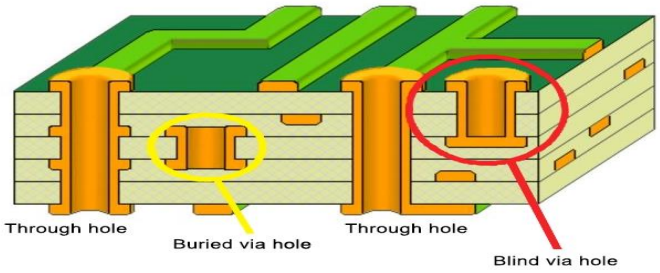


Fig.2 Types of Via used in design

Although the above signal integrity problems have distinct sources, where all of them are impacted by the board traces.

Inductance: A VIA taken in isolation is actually an inductor and thus the inductance of the VIA depends on the VIA ratio.

$$L = 5.08h\ [\ln(4h/d)+1]$$

Capacitance: The presence of the plane around creates some parasitic capacitance between the VIA pads and ground.

The relation between capacitance and VIA can be represented as

$$VIA = \frac{1.41Er\ D1T}{D2-D1}$$

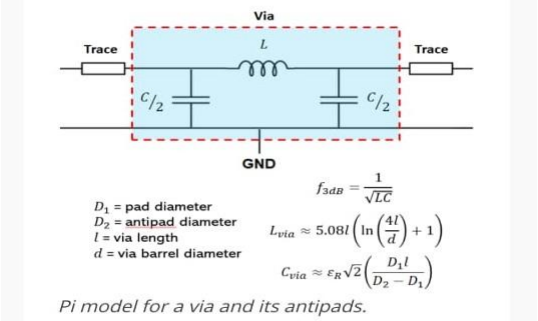
where Er is relative permeability

D1 - diameter of VIA pad

D2 - diameter of VIA antipad

As our project is high frequency structure with multi conductor transmission line ports which are driven by source, the solution type taken as "DRIVEN TERMINAL".

Units of inch and grid size as 0.1 inch starting frequency as 1 GHZ and stop frequency as 10 GHZ and sweep size as 0.5 GHZ.



Pi model for a via and its antipads.

III. VIA DESIGN USING HFSS

The simulation of via on signal integrity can be performed by using the HFSS (High Frequency Structure Simulator) microwave studio's is based on FEM (Finite Element Method)

There are six general steps to simulate in HFSS.

1. Generate a 3D structure.
2. Apply boundary.
3. Set excitation.
4. Solution setup.
5. Simulate & observe the result.

Post process

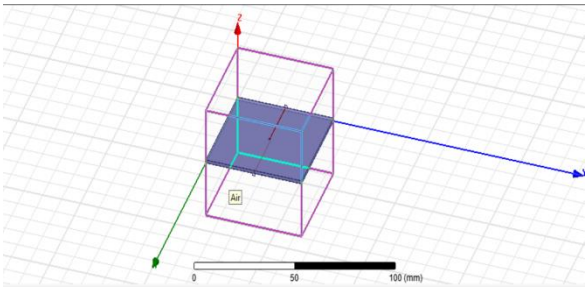


Fig.3 Design of Via using HFSS

In this design we are have the FR4_1, FR4_2, FR4_3, GND_1, GND_2, Trace1, Trace2, Via1, AntiVia1, Air1, Air2, Port 1, Port 2. These parameters having respective size, materials and centre position.

Via Design Considerations:

Draw	**Name**	**Centre position**	**Size**	**Material**
Box 1	FR4_1	(0,0,0)	(2,2,0.005)	FR4_Epoxy
Box 2	FR4_2	(0,0,0.0064)	(2,2,0.047)	FR4_Epoxy
Box 3	FR4_3	(0,0,0.0548)	(2,2,0.005)	FR4_Epoxy
Box 4	GND_1	(0,0,0.005)	(2,2,0.0014)	Copper
Box 5	GND_2	(0,0,0.0534)	(2,2,0.0014)	Copper
Box 6	Trace 1	(0,1,0.0598)	(1.005,0.005,0.0014)	Copper
Box 7	Trace 2	(0.995,1,0)	(1.005,0.005,-0.0014)	Copper
Cylinder 1	Via 1	(1,1.0025,0)	Radius= 12 mil, Height= 0.0598 in	Copper
Cylinder 2	AntiVia 1	(1,1.0025,0)	Radius= 20 mil, Height= 0.0598 in	FR4_Epoxy
Box 8	Air 1	(0,0,0.0598)	(2,2,1)	Air
Box 9	Air 2	(0,0,0)	(2,2,-1)	Air
Rectangle 1	Port 1	YZ-plane	(2,0.978,0.005), Y=0.05, Z= -0.05	Copper
Rectangle 1	Port 2	YZ-plane	(0,0.978,0.005), Y=0.05, Z= 0.05	Copper

Table.1 Via Design Considerations

S-Parameters:

Scattering parameters describe electrical behaviour of transmission line signals. It is much easier to measure power at high frequencies which defines a set of information. It is a simplified interconnect model that simulates faster and easier to correlate with actual hardware.

a1 _____ (S11, S12) _____ a2

b1 _____ (S21, S22) _____ b2

The input power is coupled to other ports if it is a directional coupler. Distribution of power to the ports in the circuits. Hence, the S-parameters is responsible for some losses which are reflection coefficient, return loss.

Return loss: The loss of power which is reinstated or reflected by the transmission line.

RL(dB)= 10 log10 Pi/Pr

Pi = Incident Power

Pr = Reflected Power

Hence, the transmitted power is maximum to the input power and reflection loss is kept ideally zero(minimum).

Y-Parameters:

As we know the high frequency components are attenuated more than the low frequency components that are useful to find the effect of parasite reactance's in signal integrity. These are also called as 'Admittance parameters.

These properties using to describe the electrical behaviour of linear electrical network. These are used to calculate the incoming and outgoing voltages and currents of a network. Y-parameters are also known as "short circuit impedance parameters".

$I_1 = Y_{11}V_1 + Y_{12}V_2$

$$I_2 = Y_{21}V_1 + Y_{22}V_2$$

Z-Parameters:

We first express the channel impedance in terms of a known system reference impedance, Z0 and reflection coefficient.

Zout = Z0((1+Γ)/(1-Γ))

In this the incident wave travel to the channel for reflection.

Γ = Vreflected/Vincident

Unequal impedance of the source output(Zs), line(Z0) and receiver(ZL) cause Impedance Mismatch.

1. Impedance Mismatch
2. Frequency Response
3. Noise

These are the most important forms in the transmission.

VSWR:

VSWR is a function of reflection coefficient, which describes the power that reflected from the antenna. If the reflection coefficient is denoted by □, then the VSWR is defined by the following formula:

$$VSWR=\frac{1+|\square|}{1-|\square|}$$

It is a key parameter to measure when using a radio transmitter. VSWR is a key value for any system using transmission lines/feeders.

It can also be expressed as the source impedance and load impedance terms.

Sij = τ = ((ZL/Z0)-1)/((ZL/Z0)+1)

When Z0 perfectly matches to ZL, the system turns "lossless" and VSWR takes unity value.

VSWR values goes to infinity in a circular where power reflected is 100%.

E-Field:

Electromagnetic waves are made of electric field. They are also called E-field. This field that surrounds electrically-charged particles and apply force on all other charged particles in the field, either attracting or repelling them. If more lines of fields are entering a closed region, there must be a source for the lines inside that region.

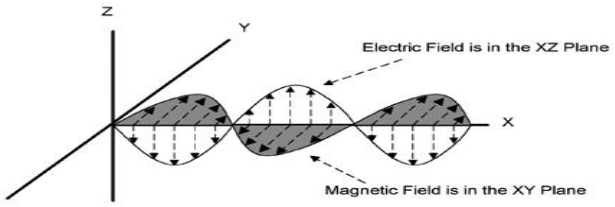
$$D = \varepsilon_0 E$$

H-field:

Electromagnetic waves are made of magnetic fields. They are also called H-field. This field that surrounds magnetically charged particles and apply force on all other charged particles in the field. Magnetic field is a vector field that describes the magnetic on moving electric charges, electric currents and magnetic materials.

$$B = \mu_0 H$$

A magnetic field and an electric field are Current and Voltage respectively that are both needed to transmit power (Watts= Volts * Amps) including in the form of radio which is a magnetic plane wave (B:H) perpendicular to an electric plane wave (E:D) of the same frequency and phased to travel along the axis of perpendicularity.



IV. SIMULATIONS & RESULTS

A. S-Parameters:

Figure (4) shows the S-parameters (S11, S12, S21, S22) of the proposed design in dB.

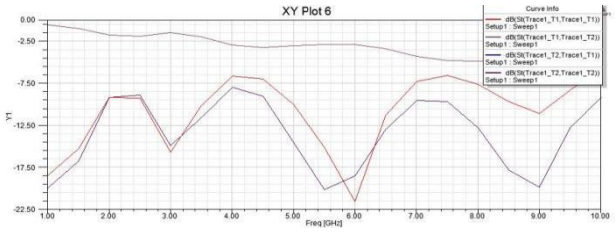


Fig.4 Terminal S-parameters

By considering -10dB cut-off gain Resonant Frequency of designed Via is

Fr= 6Ghz

F_H= 6.7Ghz

F_L= 5Ghz

%BW=[2*(fH-fL)/(fH+fL)]*100

=[2*(6.7-5)/6.7+5)]*100

=3.4/11.7*100

=29.05%

Bandwidth Utilization is 29.05

B. Y-Parameter:

Figure (5) shows the terminal Y-parameter of the proposed design in dB.

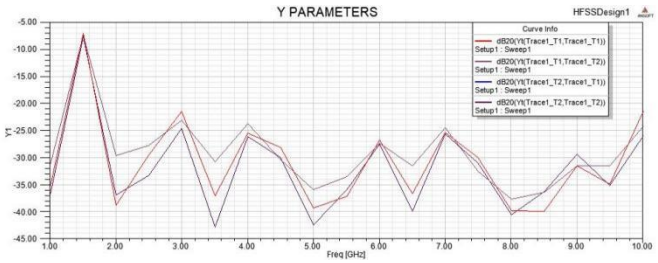


Fig.5 Terminal Y-parameter

Resonant Frequency Fr= 3Ghz

fH= 3.5Ghz

fL= 2.5Ghz

%BW=[2*(fH-fL)/(fH+fL)]*100

=[2*(3.5-2.5)/3.5+2.5)]*100

=1/3*100

=33.3%

Bandwidth Utilization is 33.3

C. VSWR Plot:

Figure (6) shows the terminal VSWR of the proposed design in dB.

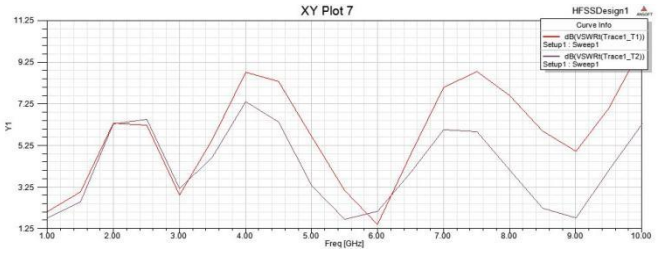


Fig . 6 Terminal VSWR

Resonant Frequency Fr= 6Ghz

fH= 6.4Ghz

fL= 5.2Ghz

%BW=[2*(fH-fL)/(fH+fL)]*100

=[2*(6.4-5.2)/6.4+5.2)]*100

=2.4/11.6*100

=20.6%

Bandwidth Utilization is 20.6

D. E-field:

Figure (7.1&7.2) shows the Mag_E of port fields of the field overlays of the proposed design.

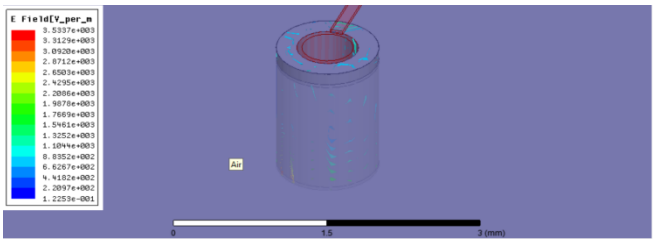


Fig.7.1

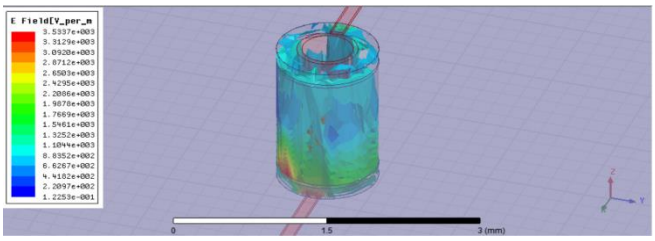


Fig. 7.2

E. H-field:

Figure (8.1&8.2) shows the Mag_H of the field overlays of the proposed design.

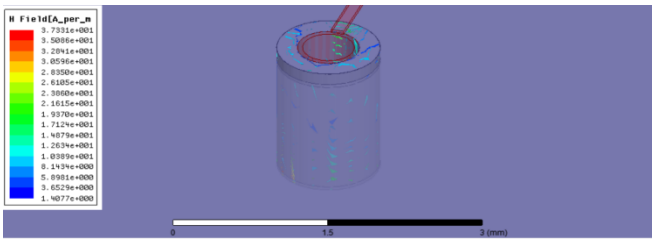


Fig.8.1

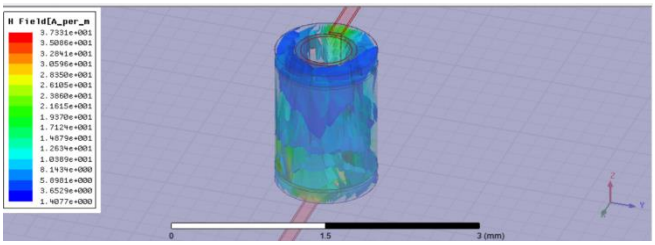


Fig.8.2

V.CONCLUSION

In this project we have designed four Layer Through Hole Via with Ground and Anti-Pad. Different Parameters like S, Y, VSWR, E-field and H-field plots have been carried out using HFSS. The Via produces a wide bandwidth of 29.05% and aspect ratio less than '8' which

proves that it can be useful for industrial application at 6 GHz Resonant frequency

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